Data sheet acquired from Cypress Semiconductor Corporation.
Data sheet modified to remove devices not offered.

TEXAS INSTRUMENTS

CY74FCT257T

SCCS019 - May 1994 - Revised February 2000

Quad 2-Input Multiplexer

Features

- **Function, pinout, and drive compatible with FCT and F logic**
- **FCT-C speed at 4.3 ns max. FCT-A speed at 5.0 ns max.**
- **Reduced V_{OH} (typically = 3.3V) versions of equivalent FCT functions**
- **Edge-rate control circuitry for significantly improved noise characteristics**
- **Power-off disable feature**
- **Matched rise and fall times**
- **Fully compatible with TTL input and output logic levels**
- **ESD > 2000V**
- **Extended commercial range of –40˚C to +85˚C**
- **Sink current 64 mA**
  Source current 32 mA

Functional Description

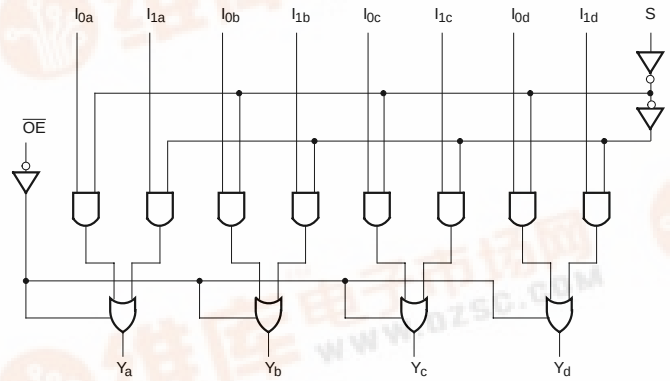
The FCT257T has four identical two-input multiplexers which select four bits of data from two sources under the control of a common data Select input (S). The I_0 inputs are selected when the Select input is LOW and the I_1 inputs are selected when the Select input is HIGH. Data appears at the output in true non-inverted form for the FCT257T.

The FCT257T is a logic implementation of a four-pole, two position switch where the position of the switch is determined by the logic levels supplied to the select input. Outputs are forced to a high-impedance “OFF” state when the Output Enable input ($\overline{OE}$) is HIGH.

All but one device must be in the high-impedance state to avoid currents exceeding the maximum ratings if outputs are tied together. Design of the Output Enable signals must ensure that there is no overlap when outputs of three-state devices are tied together.

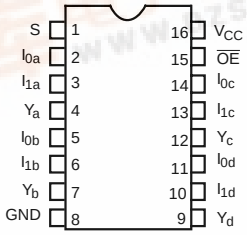
The outputs are designed with a power-off disable feature to allow for live insertion of boards.

Logic Block Diagram

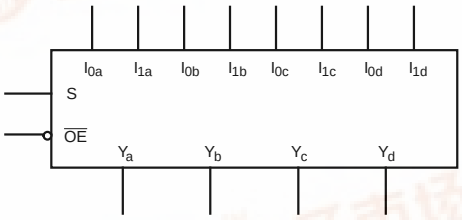


Pin Configurations

SOIC/QSOP
Top View



Logic Symbol



Pin Description

Name	Description
I	Data Inputs
S	Common Select Input
$\overline{OE}$	Enable Inputs (Active LOW)
Y	Data Outputs

Function Table[1]

Inputs				Outputs
$\overline{OE}$	S	I_0	I_1	Y
H	X	X	X	H
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

Note:

1. H = HIGH Voltage Level, L = LOW Voltage Level, X = Don’t Care, Z = High impedance (OFF) state.

Maximum Ratings[2,3]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....–65°C to +150°C

Ambient Temperature with Power Applied.....–65°C to +135°C

Supply Voltage to Ground Potential.....–0.5V to +7.0V

DC Input Voltage .....–0.5V to +7.0V

DC Output Voltage .....–0.5V to +7.0V

DC Output Current (Maximum Sink Current/Pin) .....120 mA

Power Dissipation 0.5W

Static Discharge Voltage.....>2001V (per MIL-STD-883, Method 3015)

Operating Range

Range	Range	Ambient Temperature	V_{CC}
Commercial	All	–40°C to +85°C	5V ± 5%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Typ.[4]	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC}=Min., I_{OH}=–32 mA	2.0			V
V_{OL}	Output LOW Voltage	V_{CC}=Min., I_{OL}=64 mA		0.3	0.55	V
V_{IH}	Input HIGH Voltage		2.0			V
V_{IL}	Input LOW Voltage				0.8	V
V_H	Hysteresis[5]	All inputs		0.2		V
V_{IK}	Input Clamp Diode Voltage	V_{CC}=Min., I_{IN}=–18 mA		–0.7	–1.2	V
I_I	Input HIGH Current	V_{CC}=Max., V_{IN}=V_{CC}			5	µA
I_{IH}	Input HIGH Current	V_{CC}=Max., V_{IN}=2.7V			±1	µA
I_{IL}	Input LOW Current	V_{CC}=Max., V_{IN}=0.5V			±1	µA
I_{OZH}	Off State HIGH-Level Output Current	V_{CC} = Max., V_{OUT} = 2.7V			10	µA
I_{OZL}	Off State LOW-Level Output Current	V_{CC} = Max., V_{OUT} = 0.5V			–10	µA
I_{OS}	Output Short Circuit Current[6]	V_{CC}=Max., V_{OUT}=0.0V	–60	–120	–225	mA
I_{OFF}	Power-Off Disable	V_{CC}=0V, V_{OUT}=4.5V			±1	µA

Capacitance[5]

Parameter	Description	Typ.[4]	Max.	Unit
C_{IN}	Input Capacitance	5	10	pF
C_{OUT}	Output Capacitance	9	12	pF

Notes:

2. Unless otherwise noted, these limits are over the operating free-air temperature range.
3. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.
4. Typical values are at V_{CC}=5.0V, T_A=+25°C ambient.
5. This parameter is specified but not tested.
6. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

Power Supply Characteristics

Parameter	Description	Test Conditions	Typ.[4]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC}=Max., $V_{IN}\leq$0.2V, $V_{IN}\geq V_{CC}$–0.2V	0.1	0.2	mA
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs HIGH)	V_{CC}=Max., V_{IN}=3.4V, f_1=0, Outputs Open[7]	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[8]	V_{CC}=Max., One Input Toggling, 50% Duty Cycle, Outputs Open, $\overline{OE}$=GND, $V_{IN}\leq$0.2V or $V_{IN}\geq V_{CC}$–0.2V	0.06	0.12	mA/MHz
I_C	Total Power Supply Current[9]	V_{CC}=Max., 50% Duty Cycle, Outputs Open, One Inputt Toggling at f_1=10 MHz, $\overline{OE}$=GND, $V_{IN}\leq$0.2V or $V_{IN}\geq V_{CC}$–0.2V	0.7	1.4	mA
		V_{CC}=Max.,50% Duty Cycle, Outputs Open, One Input Toggling at f_1=10 MHz, $\overline{OE}$=GND, V_{IN}=3.4V or V_{IN}=GND	1.0	2.4	mA
		V_{CC}=Max., 50% Duty Cycle, Outputs Open, Four Bits Toggling at f_1=2.5 MHz, $\overline{OE}$=GND, $V_{IN}\leq$0.2V or $V_{IN}\geq V_{CC}$–0.2V	0.7	1.4[10]	mA
		V_{CC}=Max., 50% Duty Cycle, Outputs Open, Four Bits Toggling at f_1=2.5 MHz, $\overline{OE}$=GND, V_{IN}=3.4V or V_{IN}=GND	1.7	5.4[10]	mA

Switching Characteristics Over the Operating Range

Parameter	Description	CY74FCT257T		CY74FCT257AT		CY74FCT257CT		Unit	Fig. No.[12]
		Min.[11]	Max.	Min.[11]	Max.	Min.[11]	Max.		
t_{PLH} t_{PHL}	Propagation Delay I to Y	1.5	6.0	1.5	5.0	1.5	4.3	ns	1, 3
t_{PLH} t_{PHL}	Propagation Delay S to O	1.5	10.5	1.5	7.0	1.5	5.2	ns	1, 3
t_{PZH} t_{PZL}	Output Enable Time	1.5	8.5	1.5	7.0	1.5	6.0	ns	1, 7, 8
t_{PHZ} t_{PLZ}	Output Disable Time	1.5	6.0	1.5	5.5	1.5	5.0	ns	1, 7, 8

Ordering Information

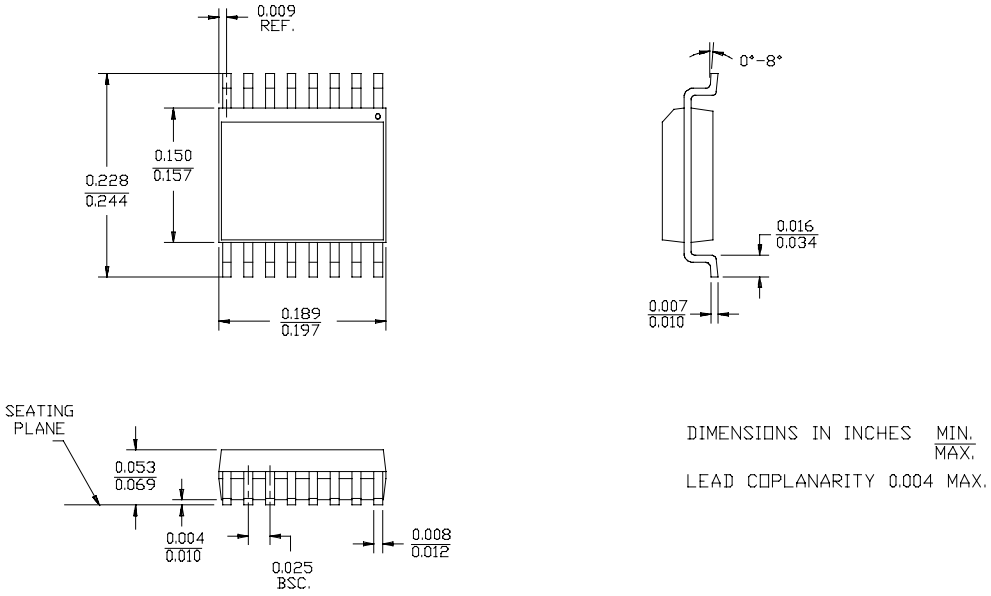
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
4.3	CY74FCT257CTQCT	Q1	16-Lead (150-Mil) QSOP	Commercial
	CY74FCT257CTSOC/SOCT	S1	16-Lead (300-Mil) Molded SOIC	
5.0	CY74FCT257ATQCT	Q1	16-Lead (150-Mil) QSOP	Commercial
6.0	CY74FCT257TQCT	Q1	16-Lead (150-Mil) QSOP	Commercial

Notes:

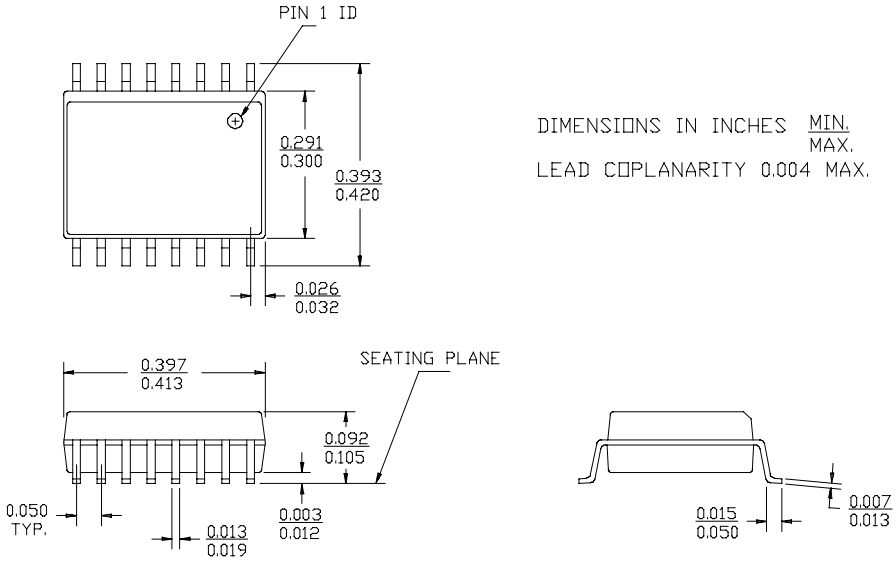
7. Per TTL driven input (V_{IN}=3.4V); all other inputs at V_{CC} or GND.
8. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
9. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC}+\Delta I_{CC}D_HN_T+I_{CCD}(f_0/2 + f_1N_1)$
   I_{CC} = Quiescent Current with CMOS input levels
   ΔI_{CC} = Power Supply Current for a TTL HIGH input (V_{IN}=3.4V)
   D_H = Duty Cycle for TTL inputs HIGH
   N_T = Number of TTL inputs at D_H
   I_{CCD} = Dynamic Current caused by an input transition pair (HLH or LHL)
   f_0 = Clock frequency for registered devices, otherwise zero
   f_1 = Input signal frequency
   N_1 = Number of inputs changing at f_1
   All currents are in milliamps and all frequencies are in megahertz.
10. Values for these conditions are examples of the I_{CC} formula. These limits are specified but not tested.
11. Minimum limits are specified but not tested on Propagation Delays.
12. See “Parameter Measurement Information” in the General Information section.

Package Diagrams

16-Lead Quarter Size Outline Q1



16-Lead Molded SOIC S1



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