

- Member of the Texas Instruments **Widebus+™** Family
- **EPIC™** (Enhanced-Performance Implanted CMOS) Submicron Process
- B-Port Outputs Have Equivalent 26-Ω Series Resistors, So No External Resistors Are Required
- **UBE™** (Universal Bus Exchanger) Allows Synchronous Data Exchange
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

NOTE: For tape and reel order entry:  
 The DGG package is abbreviated to GR, and  
 the DLR package is abbreviated to LR.

### description

This 9-bit, 4-port universal bus exchanger is designed for 1.65-V to 3.6-V  $V_{CC}$  operation.

The SN74ALVCHR16409 allows synchronous data exchange between four different buses. Data flow is controlled by the select (SEL0–SEL4) inputs. A data-flow state is stored on the rising edge of the clock (CLK) input if the select-enable (SELEN) input is low. Once a data-flow state has been established, data is stored in the flip-flop on the rising edge of CLK if SELEN is high.

The data-flow control logic is designed to allow glitch-free data transmission.

The B outputs, which are designed to sink up to 12 mA, include equivalent 26-Ω series resistors to reduce overshoot and undershoot.

When preset ( $\overline{PRE}$ ) transitions high, the outputs are disabled immediately, without waiting for a clock pulse. To leave the high-impedance state, both  $\overline{PRE}$  and SELEN must be low and a clock pulse must be applied.

To ensure the high-impedance state during power up or power down,  $\overline{PRE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

### DGG OR DL PACKAGE (TOP VIEW)

PRE	1	56	CLK
SEL0	2	55	SELEN
1A1	3	54	1B1
GND	4	53	GND
1A2	5	52	1B2
1A3	6	51	1B3
$V_{CC}$	7	50	$V_{CC}$
1A4	8	49	1B4
1A5	9	48	1B5
1A6	10	47	1B6
GND	11	46	GND
1A7	12	45	1B7
1A8	13	44	1B8
1A9	14	43	1B9
2A1	15	42	2B1
2A2	16	41	2B2
2A3	17	40	2B3
GND	18	39	GND
2A4	19	38	2B4
2A5	20	37	2B5
2A6	21	36	2B6
$V_{CC}$	22	35	$V_{CC}$
2A7	23	34	2B7
2A8	24	33	2B8
GND	25	32	GND
2A9	26	31	2B9
SEL1	27	30	SEL4
SEL2	28	29	SEL3

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

# SN74ALVCHR16409

## 9-BIT, 4-PORT UNIVERSAL BUS EXCHANGER WITH 3-STATE OUTPUTS

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### description (continued)

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCHR16409 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

Function Tables

INPUTS		OUTPUT
CLK	SEND PORT	RECEIVE PORT
X	X	$B_0^{\dagger}$
X	L	L
X	H	H
$\uparrow$	L	L
$\uparrow$	H	H
H	X	$B_0^{\dagger}$
L	X	$B_0^{\dagger}$

$\dagger$  Output level before the indicated steady-state input conditions were established

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**DATA-FLOW CONTROL**

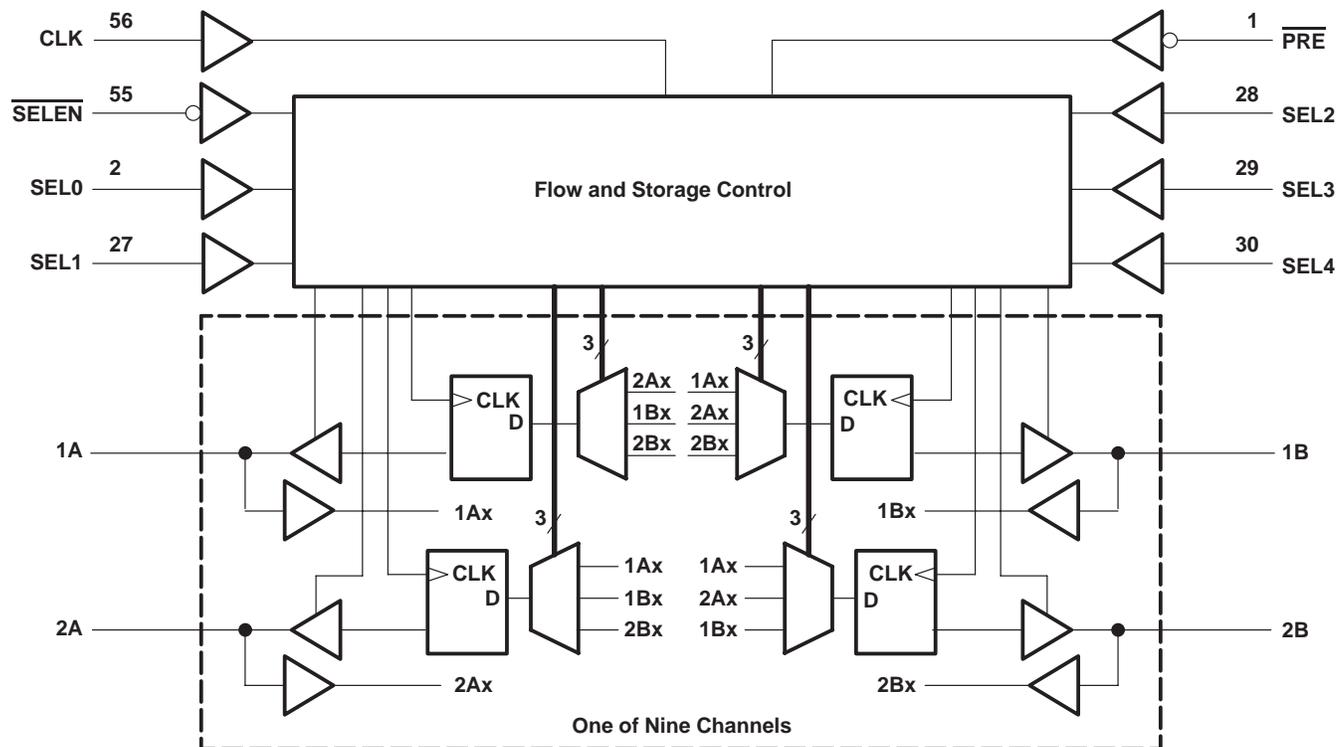
INPUTS								DATA FLOW
PRE	SELEN	CLK	SEL0	SEL1	SEL2	SEL3	SEL4	
H	X	X	X	X	X	X	X	All outputs disabled
L	H	↑	X	X	X	X	X	No change
L	L	↑	0	0	0	0	0	None, all I/Os off
L	L	↑	0	0	0	0	1	Not used
L	L	↑	0	0	0	1	0	Not used
L	L	↑	0	0	0	1	1	Not used
L	L	↑	0	0	1	0	0	Not used
L	L	↑	0	0	1	0	1	Not used
L	L	↑	0	0	1	1	0	Not used
L	L	↑	0	0	1	1	1	Not used
L	L	↑	0	1	0	0	0	2A to 1A and 1B to 2B
L	L	↑	0	1	0	0	1	2A to 1A
L	L	↑	0	1	0	1	0	2B to 1B
L	L	↑	0	1	0	1	1	2A to 1A and 2B to 1B
L	L	↑	0	1	1	0	0	1A to 2A and 1B to 2B
L	L	↑	0	1	1	0	1	1A to 2A
L	L	↑	0	1	1	1	0	1B to 2B
L	L	↑	0	1	1	1	1	1A to 2A and 2B to 1B
L	L	↑	1	0	0	0	0	1A to 1B and 2B to 2A
L	L	↑	1	0	0	0	1	1A to 1B
L	L	↑	1	0	0	1	0	2A to 2B
L	L	↑	1	0	0	1	1	1A to 1B and 2A to 2B
L	L	↑	1	0	1	0	0	1B to 1A and 2A to 2B
L	L	↑	1	0	1	0	1	1B to 1A
L	L	↑	1	0	1	1	0	2B to 2A
L	L	↑	1	0	1	1	1	1B to 1A and 2B to 2A
L	L	↑	1	1	0	0	0	2B to 1A and 2A to 1B
L	L	↑	1	1	0	0	1	1B to 2A
L	L	↑	1	1	0	1	0	2B to 1A
L	L	↑	1	1	0	1	1	2B to 1A and 1B to 2A
L	L	↑	1	1	1	0	0	1A to 2B and 1B to 2A
L	L	↑	1	1	1	0	1	1A to 2B
L	L	↑	1	1	1	1	0	2A to 1B
L	L	↑	1	1	1	1	1	1A to 2B and 2A to 1B

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## 9-BIT, 4-PORT UNIVERSAL BUS EXCHANGER WITH 3-STATE OUTPUTS

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### logic diagram (positive logic)



### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ .....	-0.5 V to 4.6 V
Input voltage range, $V_I$ : Except I/O ports (see Note 1) .....	-0.5 V to 4.6 V
I/O ports (see Notes 1 and 2) .....	-0.5 V to $V_{CC} + 0.5$ V
Output voltage range, $V_O$ (see Notes 1 and 2) .....	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ ) .....	-50 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ ) .....	-50 mA
Continuous output current, $I_O$ .....	$\pm 50$ mA
Continuous current through each $V_{CC}$ or GND .....	$\pm 100$ mA
Package thermal impedance, $\theta_{JA}$ (see Note 3): DGG package .....	81°C/W
DL package .....	74°C/W
Storage temperature range, $T_{stg}$ .....	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.  
 2. This value is limited to 4.6 V maximum.  
 3. The package thermal impedance is calculated in accordance with JESD 51.

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**recommended operating conditions (see Note 4)**

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	1.65	3.6	V
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 1.65 V to 1.95 V	0.65 × V <sub>CC</sub>	V
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.7	
		V <sub>CC</sub> = 2.7 V to 3.6 V	2	
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 1.65 V to 1.95 V	0.35 × V <sub>CC</sub>	V
		V <sub>CC</sub> = 2.3 V to 2.7 V	0.7	
		V <sub>CC</sub> = 2.7 V to 3.6 V	0.8	
V <sub>I</sub>	Input voltage	0	V <sub>CC</sub>	V
V <sub>O</sub>	Output voltage	0	V <sub>CC</sub>	V
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 1.65 V	-2	mA
		V <sub>CC</sub> = 2.3 V	-6	
		V <sub>CC</sub> = 2.7 V	-8	
		V <sub>CC</sub> = 3 V	-12	
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 1.65 V	2	mA
		V <sub>CC</sub> = 2.3 V	6	
		V <sub>CC</sub> = 2.7 V	8	
		V <sub>CC</sub> = 3 V	12	
Δt/Δv	Input transition rise or fall rate		10	ns/V
T <sub>A</sub>	Operating free-air temperature	-40	85	°C

NOTE 4: All unused control inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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**9-BIT, 4-PORT UNIVERSAL BUS EXCHANGER**  
**WITH 3-STATE OUTPUTS**

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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	MIN	TYP†	MAX	UNIT
V <sub>OH</sub>	I <sub>OH</sub> = -100 μA	1.65 V to 3.6 V	V <sub>CC</sub> -0.2			V
	I <sub>OH</sub> = -2 mA	1.65 V	1.2			
	I <sub>OH</sub> = -4 mA	2.3 V	1.9			
	I <sub>OH</sub> = -6 mA	2.3 V	1.7			
		3 V	2.4			
	I <sub>OH</sub> = -8 mA	2.7 V	2			
I <sub>OH</sub> = -12 mA	3 V	2				
V <sub>OL</sub>	I <sub>OL</sub> = 100 μA	1.65 V to 3.6 V			0.2	V
	I <sub>OL</sub> = 2 mA	1.65 V			0.45	
	I <sub>OL</sub> = 4 mA	2.3 V			0.4	
	I <sub>OL</sub> = 6 mA	2.3 V			0.55	
		3 V			0.55	
	I <sub>OL</sub> = 8 mA	2.7 V			0.6	
I <sub>OL</sub> = 12 mA	3 V			0.8		
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	3.6 V			±5	μA
I <sub>I</sub> (hold)	V <sub>I</sub> = 0.58 V	1.65 V	25			μA
	V <sub>I</sub> = 1.07 V		-25			
	V <sub>I</sub> = 0.7 V	2.3 V	45			
	V <sub>I</sub> = 1.7 V		-45			
	V <sub>I</sub> = 0.8 V	3 V	75			
	V <sub>I</sub> = 2 V		-75			
V <sub>I</sub> = 0 to 3.6 V‡	3.6 V			±500		
I <sub>OZ</sub> §	V <sub>O</sub> = V <sub>CC</sub> or GND	3.6 V			±10	μA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	3.6 V			40	μA
ΔI <sub>CC</sub>	One input at V <sub>CC</sub> - 0.6 V, Other inputs at V <sub>CC</sub> or GND	3 V to 3.6 V			750	μA
C <sub>i</sub>	Control inputs	V <sub>I</sub> = V <sub>CC</sub> or GND	3.3 V		4	pF
C <sub>io</sub>	A or B ports	V <sub>O</sub> = V <sub>CC</sub> or GND	3.3 V		8	pF

† All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

‡ This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

§ For I/O ports, the parameter I<sub>OZ</sub> includes the input leakage current.

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## 9-BIT, 4-PORT UNIVERSAL BUS EXCHANGER WITH 3-STATE OUTPUTS

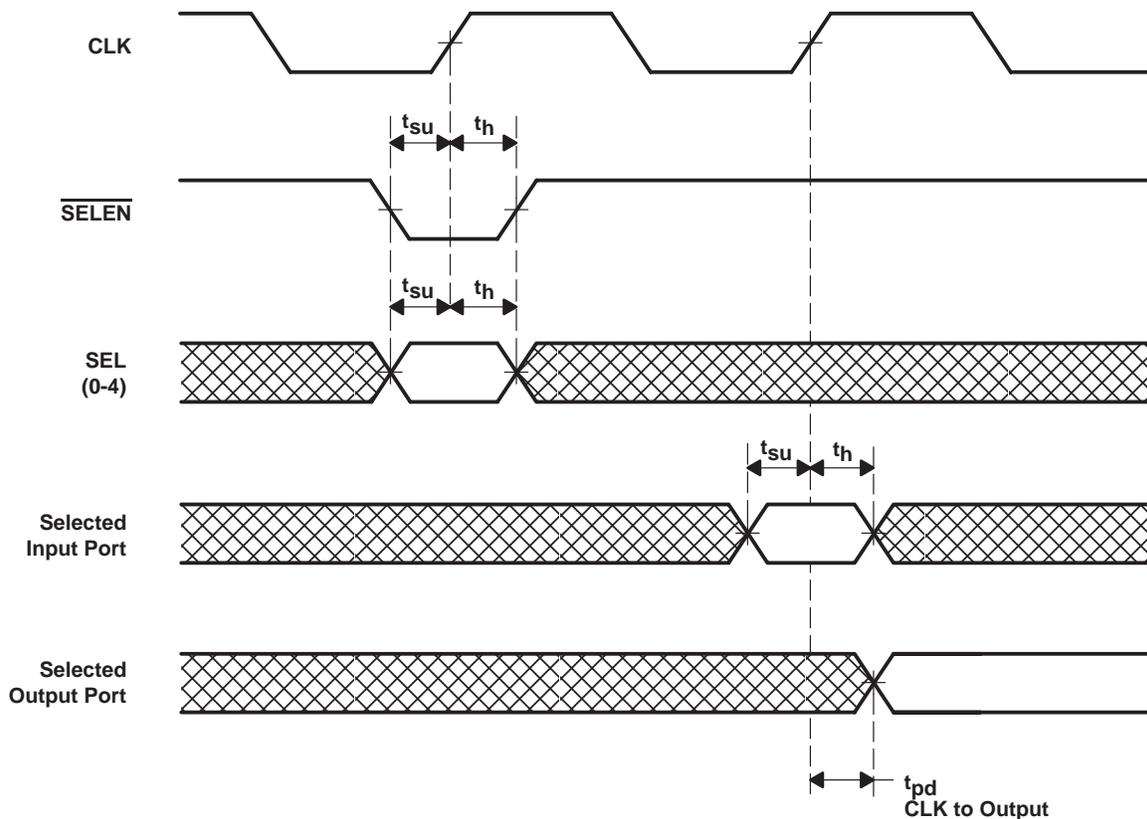
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timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

		$V_{CC} = 1.8\text{ V}$		$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$f_{\text{clock}}$	Clock frequency		†		120		120		120	MHz
$t_w$	Pulse duration, CLK high or low		†		4.2		4.2		3	ns
$t_{\text{su}}$	Setup time	A or B before CLK↑	†		1.9		1.9		1.4	ns
		SEL before CLK↑	†		5.1		4.2		3.5	
		$\overline{\text{SELEN}}$ before CLK↑	†		2.5		2.5		1.8	
		$\overline{\text{PRE}}$ before CLK↑	†		1		1		0.7	
$t_{\text{h}}$	Hold time	A or B after CLK↑	†		0.8		0.8		1	ns
		SEL after CLK↑	†		0		0		0	
		$\overline{\text{SELEN}}$ after CLK↑	†		0.5		0.5		0.8	

† This information was not available at the time of publication.

### timing diagram



**SN74ALVCHR16409**  
**9-BIT, 4-PORT UNIVERSAL BUS EXCHANGER**  
**WITH 3-STATE OUTPUTS**

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**switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 1.8 V		V <sub>CC</sub> = 2.5 V ± 0.2 V		V <sub>CC</sub> = 2.7 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		UNIT
			MIN	TYP	MIN	MAX	MIN	MAX	MIN	MAX	
f <sub>max</sub>			†		120		120		120		MHz
t <sub>pd</sub>	CLK	A or B		†	1.5	6.9		7	1.5	6.2	ns
t <sub>en</sub>	CLK	A or B		†	2.4	7.8		7.6	2	6.8	ns
t <sub>dis</sub>	CLK	A or B		†	2.3	7.1		6.4	2	6.1	ns
	$\overline{\text{PRE}}$			†	2.8	7.7		7	2.5	6.4	

† This information was not available at the time of publication.

**operating characteristics, T<sub>A</sub> = 25°C**

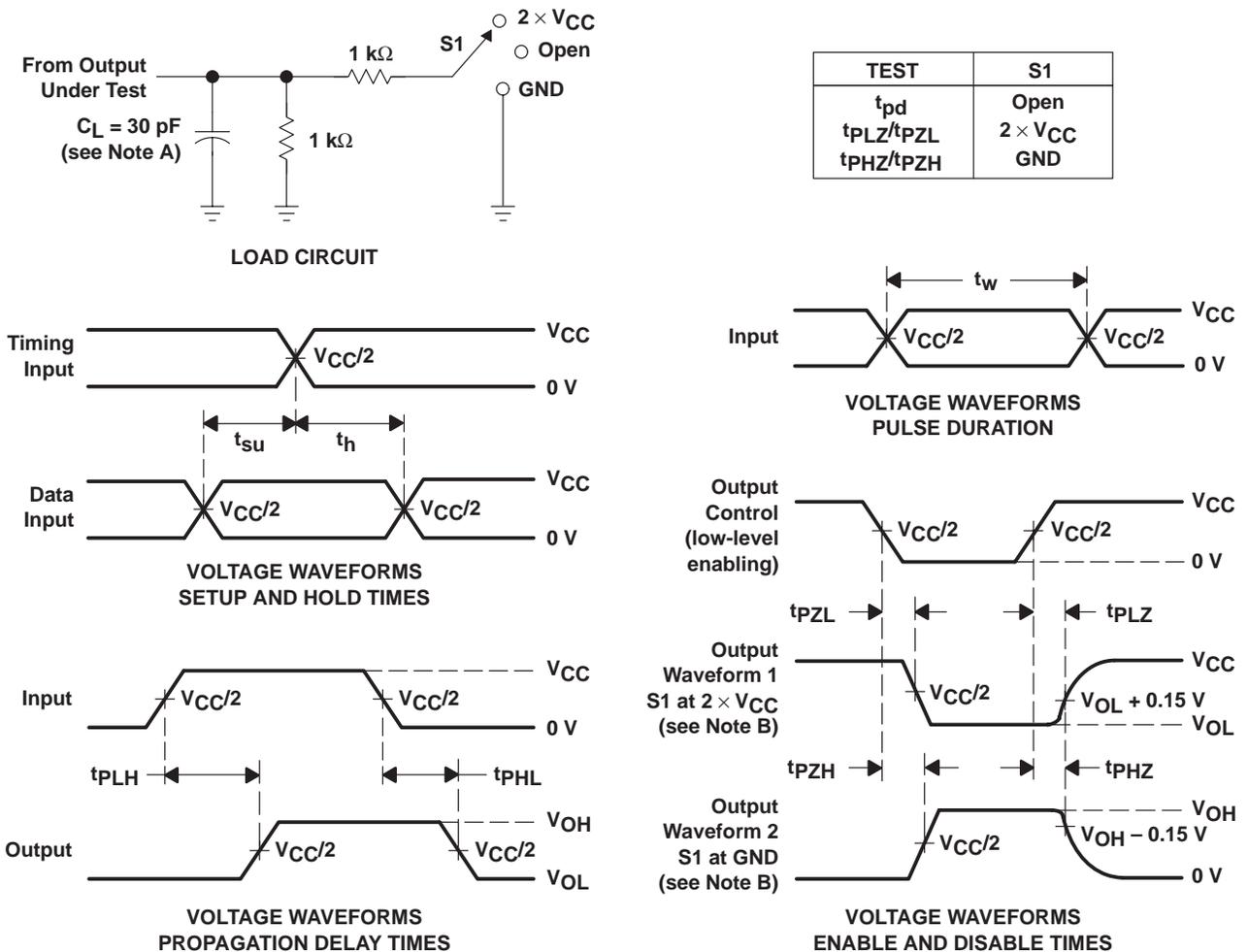
PARAMETER		TEST CONDITIONS	V <sub>CC</sub> = 1.8 V	V <sub>CC</sub> = 2.5 V	V <sub>CC</sub> = 3.3 V	UNIT
			TYP	TYP	TYP	
C <sub>pd</sub>	Power dissipation	All outputs enabled	†	60	60	pF
	capacitance	All outputs disabled	†	60	60	

† This information was not available at the time of publication.

# SN74ALVCHR16409 9-BIT, 4-PORT UNIVERSAL BUS EXCHANGER WITH 3-STATE OUTPUTS

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## PARAMETER MEASUREMENT INFORMATION $V_{CC} = 1.8\text{ V}$



- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_O = 50\ \Omega$ ,  $t_r \leq 2\text{ ns}$ ,  $t_f \leq 2\text{ ns}$ .
  - D. The outputs are measured one at a time with one transition per measurement.
  - E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

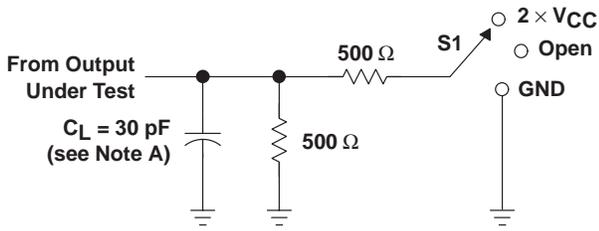
**Figure 1. Load Circuit and Voltage Waveforms**

**SN74ALVCHR16409**  
**9-BIT, 4-PORT UNIVERSAL BUS EXCHANGER**  
**WITH 3-STATE OUTPUTS**

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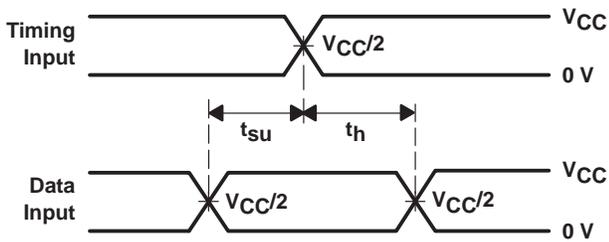
**PARAMETER MEASUREMENT INFORMATION**

$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$

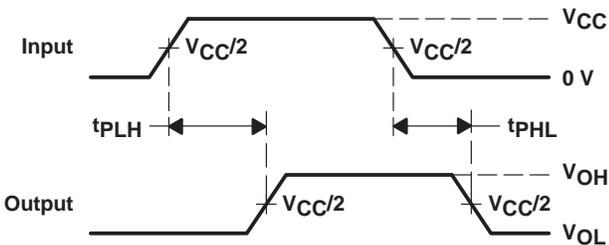


**LOAD CIRCUIT**

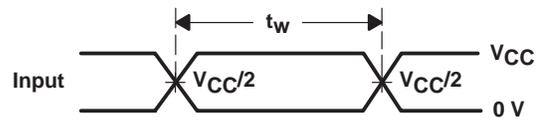
TEST	S1
$t_{pd}$	Open
$t_{PLZ}/t_{PZL}$	$2 \times V_{CC}$
$t_{PHZ}/t_{PZH}$	GND



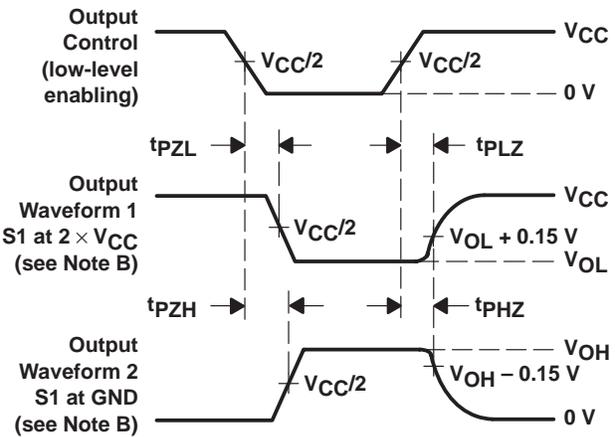
**VOLTAGE WAVEFORMS  
 SETUP AND HOLD TIMES**



**VOLTAGE WAVEFORMS  
 PROPAGATION DELAY TIMES**



**VOLTAGE WAVEFORMS  
 PULSE DURATION**



**VOLTAGE WAVEFORMS  
 ENABLE AND DISABLE TIMES**

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 2\text{ ns}$ ,  $t_f \leq 2\text{ ns}$ .  
 D. The outputs are measured one at a time with one transition per measurement.  
 E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .  
 F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .  
 G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

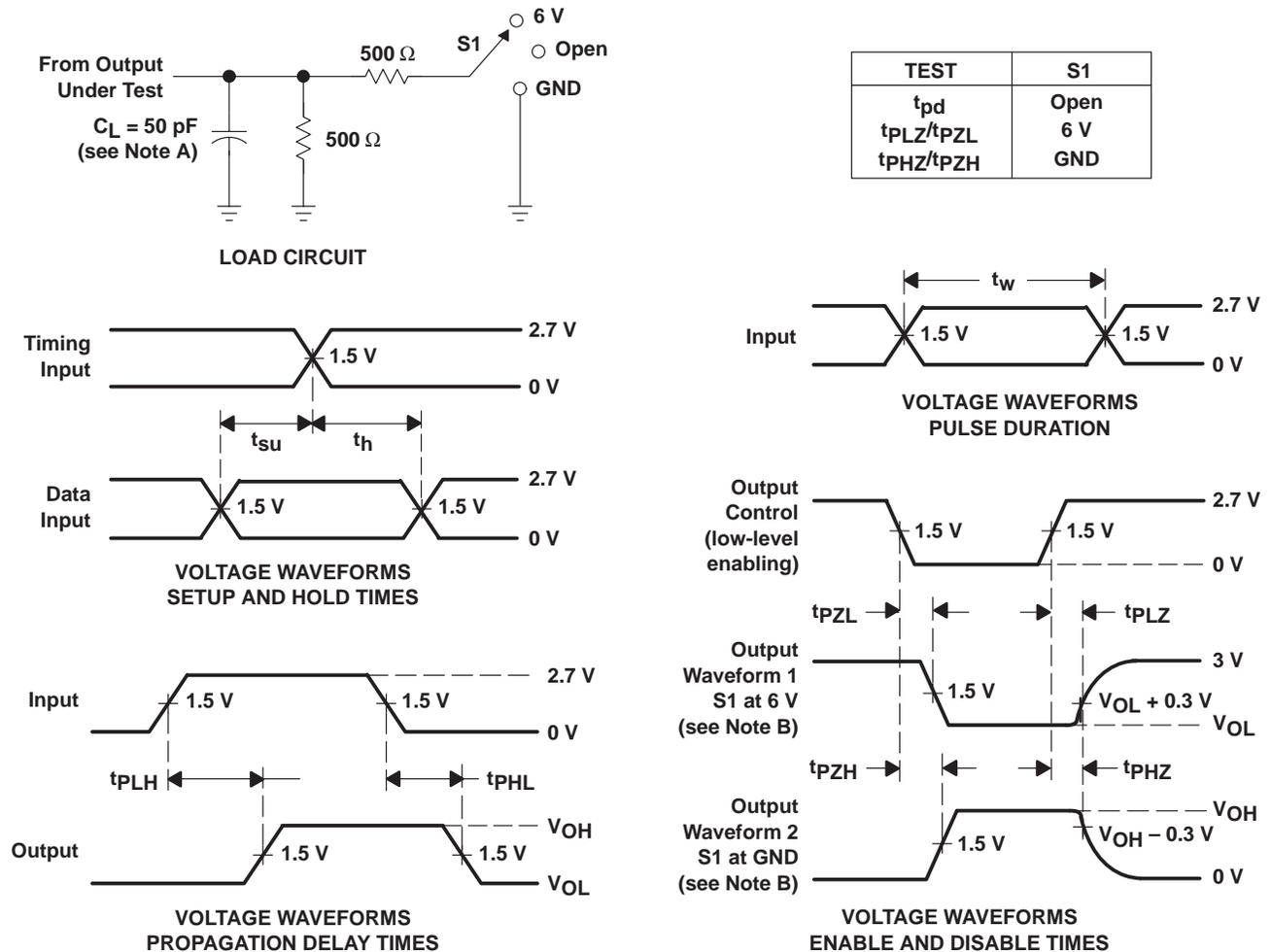
**Figure 2. Load Circuit and Voltage Waveforms**

# SN74ALVCHR16409 9-BIT, 4-PORT UNIVERSAL BUS EXCHANGER WITH 3-STATE OUTPUTS

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## PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 2.7\text{ V AND } 3.3\text{ V} \pm 0.3\text{ V}$



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 2.5\text{ ns}$ ,  $t_f \leq 2.5\text{ ns}$ .  
 D. The outputs are measured one at a time with one transition per measurement.  
 E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .  
 F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .  
 G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

**Figure 3. Load Circuit and Voltage Waveforms**

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