

18-BIT UNIVERSAL BUS DRIVER WITH 3-STATE OUTPUTS

SCES126E – FEBRUARY 1998 – REVISED FEBRUARY 1999

- **Member of the Texas Instruments Widebus™ Family**
- **EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Ideal for Use in PC100 Register DIMM Revision 1.1**
- **Output Port Has Equivalent 26-Ω Series Resistors, So No External Resistors Are Required**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **Package Options Include Plastic Shrink Small-Outline (DL), Thin Shrink Small-Outline (DGG), and Thin Very Small-Outline (DGV) Packages**

description

This 18-bit universal bus driver is designed for 1.65-V to 3.6-V V_{CC} operation.

Data flow from A to Y is controlled by the output-enable (\overline{OE}) input. The device operates in the transparent mode when the latch-enable (LE) input is high. When LE is low, the A data is latched if the clock (CLK) input is held at a high or low logic level. If LE is low, the A data is stored in the latch/flip-flop on the low-to-high transition of CLK. When \overline{OE} is high, the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The output port includes equivalent 26-Ω series resistors to reduce overshoot and undershoot.

The SN74ALVC162835 is characterized for operation from -40°C to 85°C.

DGG, DGV, OR DL PACKAGE (TOP VIEW)

NC	1	56	GND
NC	2	55	NC
Y1	3	54	A1
GND	4	53	GND
Y2	5	52	A2
Y3	6	51	A3
V_{CC}	7	50	V_{CC}
Y4	8	49	A4
Y5	9	48	A5
Y6	10	47	A6
GND	11	46	GND
Y7	12	45	A7
Y8	13	44	A8
Y9	14	43	A9
Y10	15	42	A10
Y11	16	41	A11
Y12	17	40	A12
GND	18	39	GND
Y13	19	38	A13
Y14	20	37	A14
Y15	21	36	A15
V_{CC}	22	35	V_{CC}
Y16	23	34	A16
Y17	24	33	A17
GND	25	32	GND
Y18	26	31	A18
\overline{OE}	27	30	CLK
LE	28	29	GND

NC – No internal connection

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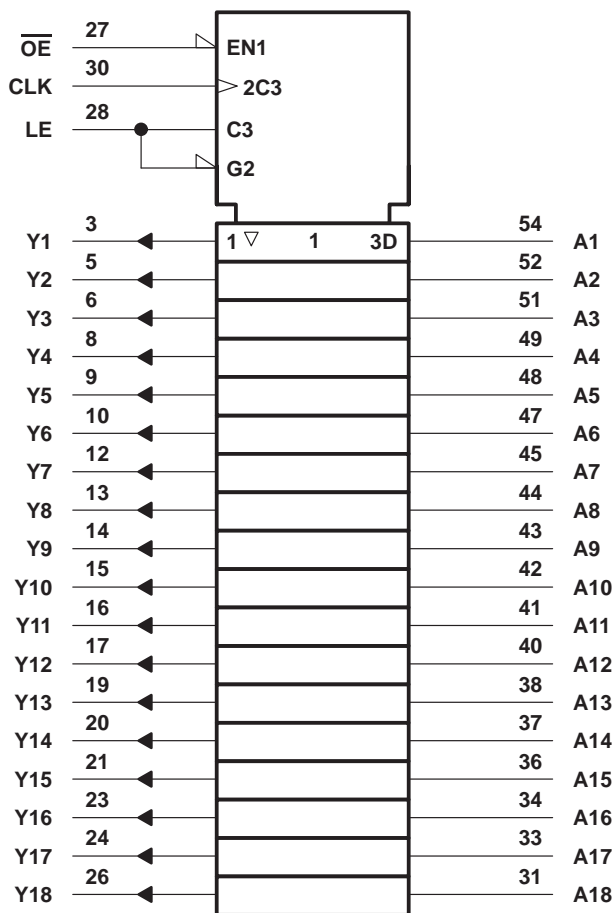
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FUNCTION TABLE

INPUTS				OUTPUT
\overline{OE}	LE	CLK	A	Y
H	X	X	X	Z
L	H	X	L	L
L	H	X	H	H
L	L	↑	L	L
L	L	↑	H	H
L	L	L or H	X	Y_0^\dagger

† Output level before the indicated steady-state input conditions were established

logic symbol‡



‡ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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recommended operating conditions (see Note 4)

		MIN	MAX	UNIT
V _{CC}	Supply voltage	1.65	3.6	V
V _{IH}	High-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}	V
		V _{CC} = 2.3 V to 2.7 V	1.7	
		V _{CC} = 2.7 V to 3.6 V	2	
V _{IL}	Low-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.35 × V _{CC}	V
		V _{CC} = 2.3 V to 2.7 V	0.7	
		V _{CC} = 2.7 V to 3.6 V	0.8	
V _I	Input voltage	0	V _{CC}	V
V _O	Output voltage	0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 1.65 V	-2	mA
		V _{CC} = 2.3 V	-6	
		V _{CC} = 2.7 V	-8	
		V _{CC} = 3 V	-12	
I _{OL}	Low-level output current	V _{CC} = 1.65 V	2	mA
		V _{CC} = 2.3 V	6	
		V _{CC} = 2.7 V	8	
		V _{CC} = 3 V	12	
Δt/Δv	Input transition rise or fall rate		10	ns/V
T _A	Operating free-air temperature	-40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	TYP†	MAX	UNIT
V _{OH}		I _{OH} = -100 μA	1.65 V to 3.6 V	V _{CC} -0.2			V
		I _{OH} = -2 mA	1.65 V	1.2			
		I _{OH} = -4 mA	2.3 V	1.9			
		I _{OH} = -6 mA	2.3 V	1.7			
			3 V	2.4			
		I _{OH} = -8 mA	2.7 V	2			
	I _{OH} = -12 mA	3 V	2				
V _{OL}		I _{OL} = 100 μA	1.65 V to 3.6 V			0.2	V
		I _{OL} = 2 mA	1.65 V			0.45	
		I _{OL} = 4 mA	2.3 V			0.4	
		I _{OL} = 6 mA	2.3 V			0.55	
			3 V			0.55	
		I _{OL} = 8 mA	2.7 V			0.6	
	I _{OL} = 12 mA	3 V			0.8		
I _I		V _I = V _{CC} or GND	3.6 V			±5	μA
I _{OZ}		V _O = V _{CC} or GND	3.6 V			±10	μA
I _{CC}		V _I = V _{CC} or GND, I _O = 0	3.6 V			40	μA
ΔI _{CC}		One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND	3 V to 3.6 V			750	μA
C _i	Control inputs	V _I = V _{CC} or GND	3.3 V	3.5			pF
	Data inputs			5			
C _o	Outputs	V _O = V _{CC} or GND	3.3 V	7			pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

		V _{CC} = 1.8 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency	‡		150		150		150		MHz
t _w	Pulse duration	LE high		3.3		3.3		3.3		ns
		CLK high or low		3.3		3.3		3.3		
t _{su}	Setup time	Data before CLK↑		‡		2.2		2.1		ns
		Data before LE↓	CLK high	‡		1.9		1.6		
			CLK low	‡		1.3		1.1		
t _h	Hold time	Data after CLK↑		‡		0.6		0.6		ns
		Data after LE↓	CLK high or low	‡		1.4		1.7		

‡ This information was not available at the time of publication.

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switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 1.8 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	TYP	MIN	MAX	MIN	MAX	MIN	MAX	
f _{max}			†		150		150		150		MHz
t _{pd}	A	Y	†		1	5	5		1	4.2	ns
	LE		†		1.3	5.9	5.8		1.3	5.1	
	CLK		†		1.4	6.3	6.1		1.4	5.4	
t _{en}	$\overline{\text{OE}}$	Y	†		1.4	6.3	6.5		1.1	5.5	ns
t _{dis}	$\overline{\text{OE}}$	Y	†		1	4.9	4.9		1.3	4.5	ns

† This information was not available at the time of publication.

switching characteristics from 0°C to 85°C, C_L = 0 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 3.3 V ± 0.15 V		UNIT
			MIN	MAX	
t _{pd} †	A	Y	0.9	2	ns
	CLK	Y	1.4	2.9	ns

† Texas Instruments SPICE simulation data

switching characteristics from 0°C to 65°C, C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 3.3 V ± 0.15 V		UNIT
			MIN	MAX	
t _{pd}	A	Y	1	4	ns
	CLK	Y	1.9	5	ns

operating characteristics, T_A = 25°C

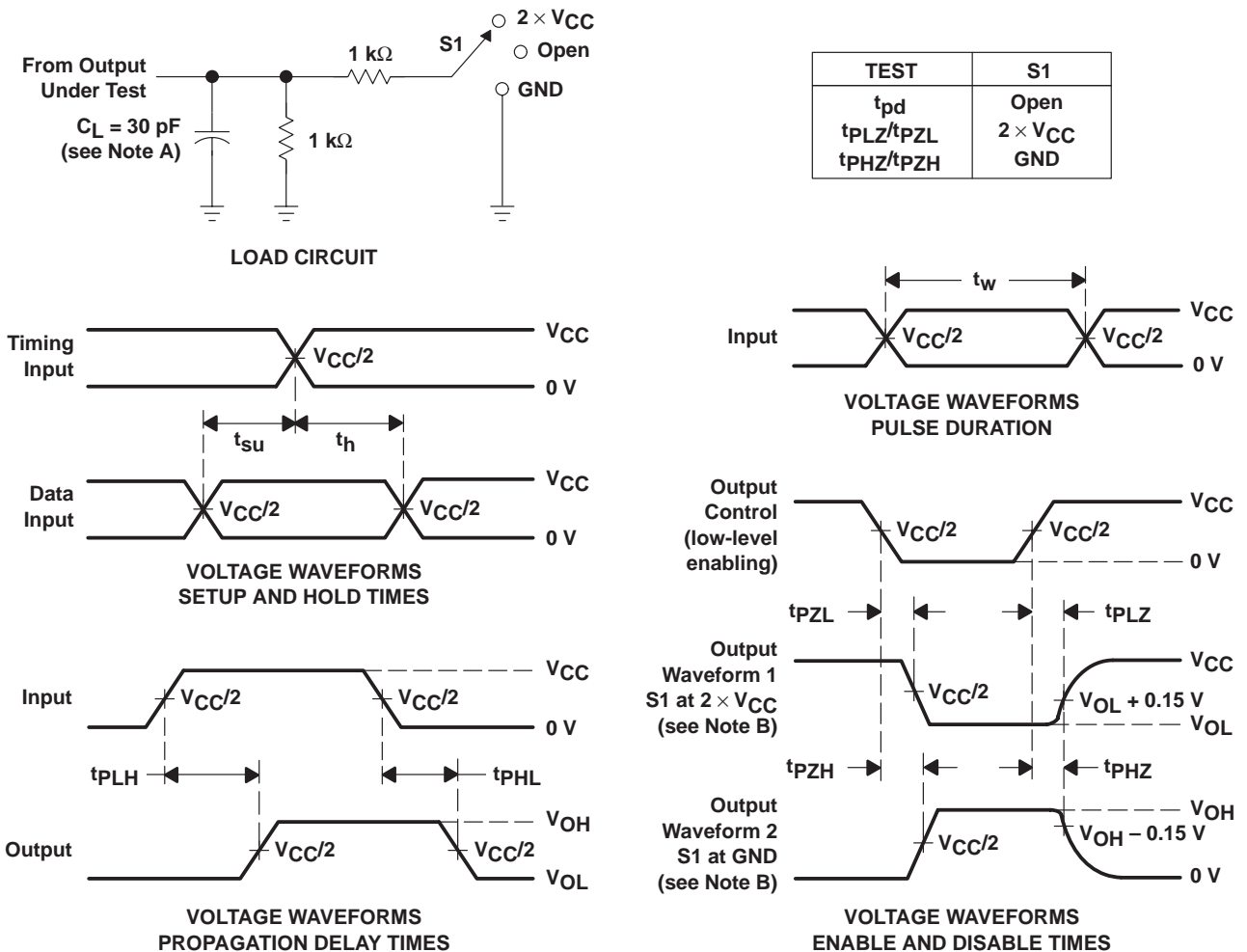
PARAMETER		TEST CONDITIONS	V _{CC} = 1.8 V	V _{CC} = 2.5 V	V _{CC} = 3.3 V	UNIT
			TYP	TYP	TYP	
C _{pd}	Power dissipation capacitance	C _L = 0, f = 10 MHz	†	35.5	40	pF
	Outputs enabled		†	12.5	14	
	Outputs disabled					

† This information was not available at the time of publication.

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PARAMETER MEASUREMENT INFORMATION $V_{CC} = 1.8\text{ V}$



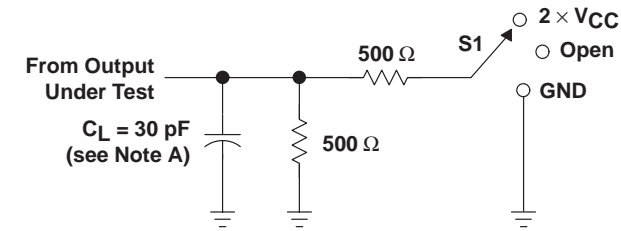
- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 2\text{ ns}$, $t_f \leq 2\text{ ns}$.
 D. The outputs are measured one at a time with one transition per measurement.
 E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 F. t_{PZL} and t_{PZH} are the same as t_{en} .
 G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

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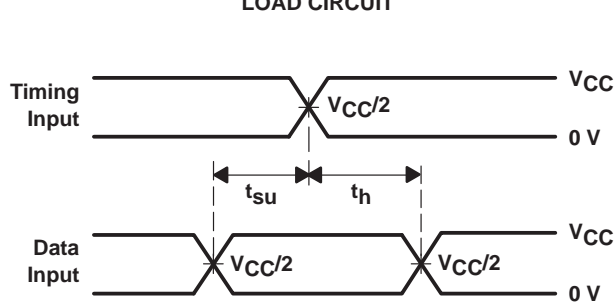
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PARAMETER MEASUREMENT INFORMATION
 $V_{CC} = 2.5 V \pm 0.2 V$

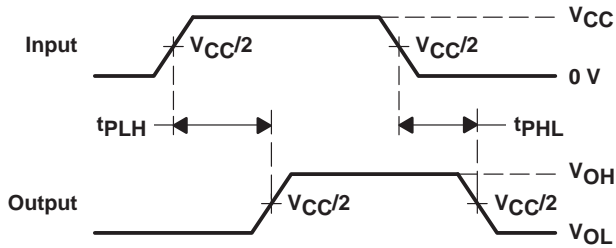


TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND

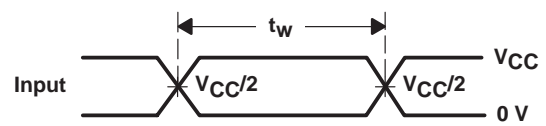
LOAD CIRCUIT



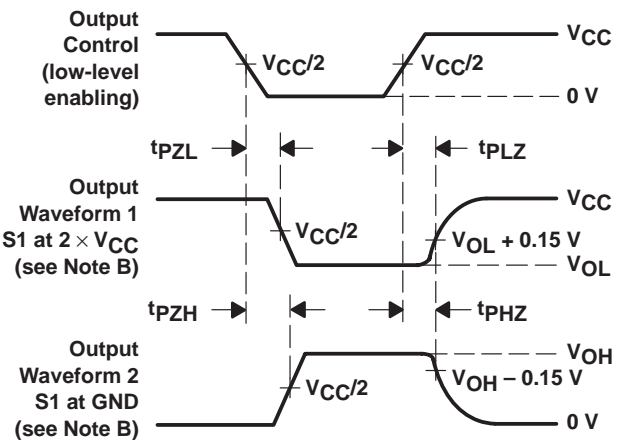
**VOLTAGE WAVEFORMS
 SETUP AND HOLD TIMES**



**VOLTAGE WAVEFORMS
 PROPAGATION DELAY TIMES**



**VOLTAGE WAVEFORMS
 PULSE DURATION**



**VOLTAGE WAVEFORMS
 ENABLE AND DISABLE TIMES**

- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .

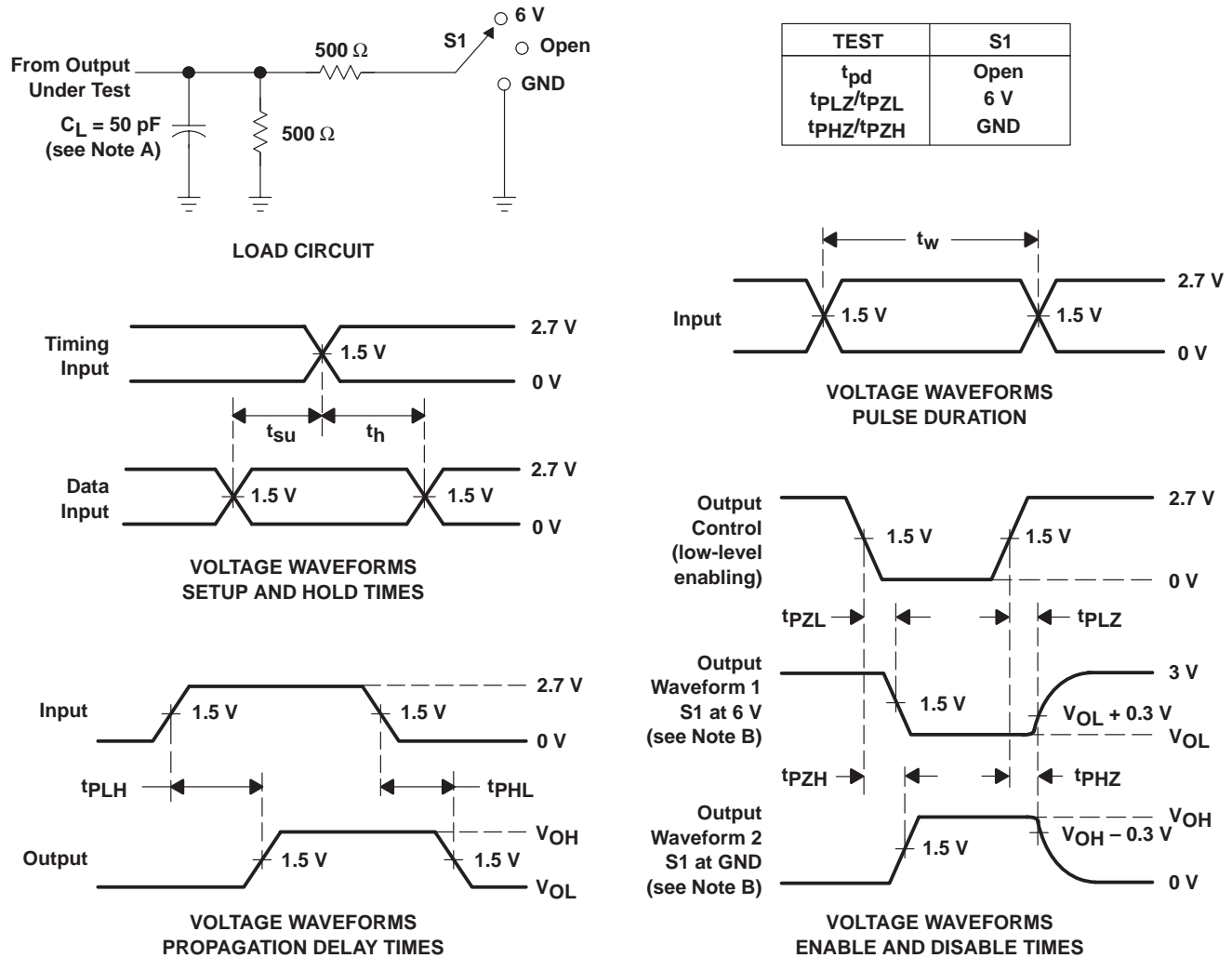
Figure 2. Load Circuit and Voltage Waveforms

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PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 2.7\text{ V AND } 3.3\text{ V} \pm 0.3\text{ V}$



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 2.5\text{ ns}$, $t_f \leq 2.5\text{ ns}$.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 3. Load Circuit and Voltage Waveforms

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TYPICAL CHARACTERISTICS

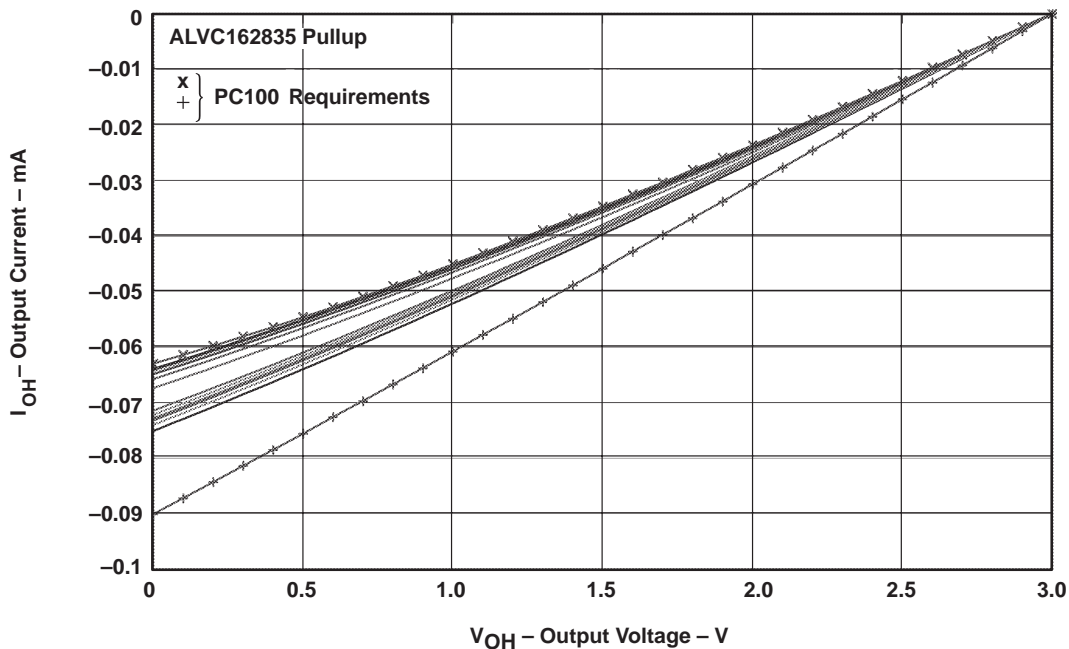


Figure 4. IV Characteristics - Pullup

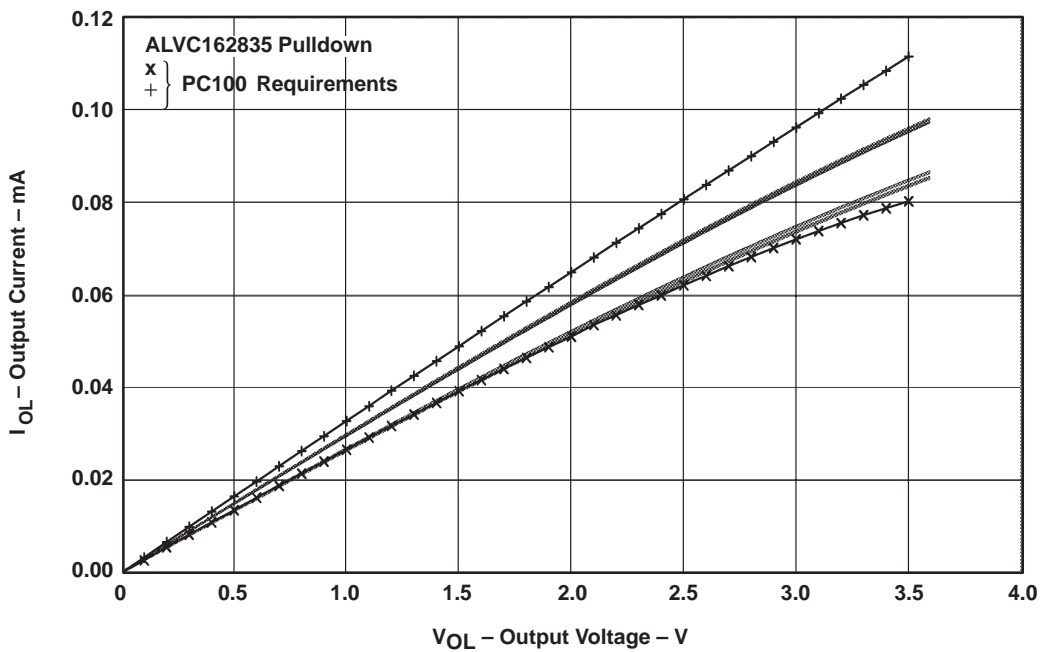


Figure 5. IV Characteristics - Pulldown

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