

# SN74AVC16245 16-BIT BUS TRANSCEIVER WITH 3-STATE OUTPUTS

SCES142L – JULY 1998 – REVISED FEBRUARY 2000

- Member of the Texas Instruments **Widebus™** Family
- **EPIC™** (Enhanced-Performance Implanted CMOS) Submicron Process
- **DOC™** (Dynamic Output Control) Circuit Dynamically Changes Output Impedance, Resulting in Noise Reduction Without Speed Degradation
- Less Than 2-ns Maximum Propagation Delay at 2.5-V and 3.3-V  $V_{CC}$
- Dynamic Drive Capability Is Equivalent to Standard Outputs With  $I_{OH}$  and  $I_{OL}$  of  $\pm 24$  mA at 2.5-V  $V_{CC}$
- Overvoltage-Tolerant Inputs/Outputs Allow Mixed-Voltage-Mode Data Communications
- $I_{off}$  Supports Partial-Power-Down Mode Operation
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
- Latch-Up Performance Exceeds 250 mA Per JESD 78
- Package Options Include Plastic Thin Shrink Small-Outline (DGG) and Thin Very Small-Outline (DGV) Packages

## description

A Dynamic Output Control (DOC) circuit is implemented, which, during the transition, initially lowers the output impedance to effectively drive the load and, subsequently, raises the impedance to reduce noise. Figure 1 shows typical  $V_{OL}$  vs  $I_{OL}$  and  $V_{OH}$  vs  $I_{OH}$  curves to illustrate the output impedance and drive capability of the circuit. At the beginning of the signal transition, the DOC circuit provides a maximum dynamic drive that is equivalent to a high-drive standard-output device. For more information, refer to the TI application reports, *AVC Logic Family Technology and Applications*, literature number SCEA006, and *Dynamic Output Control (DOC™) Circuitry Technology and Applications*, literature number SCEA009.

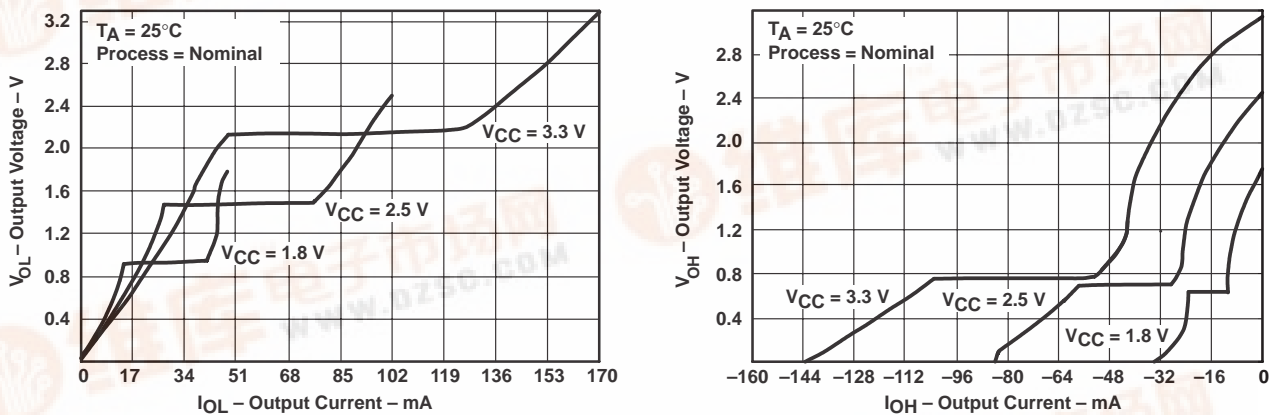


Figure 1. Output Voltage vs Output Current

This 16-bit (dual octal) noninverting bus transceiver is operational at 1.2-V to 3.6-V  $V_{CC}$ , but is designed specifically for 1.65-V to 3.6-V  $V_{CC}$  operation.

The SN74AVC16245 is designed for asynchronous communication between data buses. The control-function implementation minimizes external timing requirements.

This device can be used as two 8-bit transceivers or one 16-bit transceiver. It allows data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ( $\overline{OE}$ ) input can be used to disable the device so that the buses are effectively isolated.

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## 16-BIT BUS TRANSCEIVER

### WITH 3-STATE OUTPUTS

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#### description (continued)

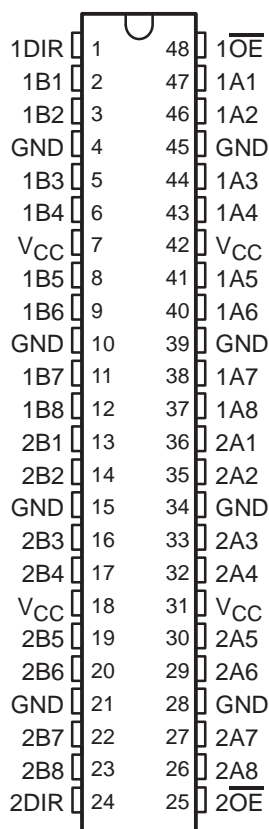
To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

The SN74AVC16245 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

#### terminal assignments

DGG OR DGV PACKAGE  
(TOP VIEW)



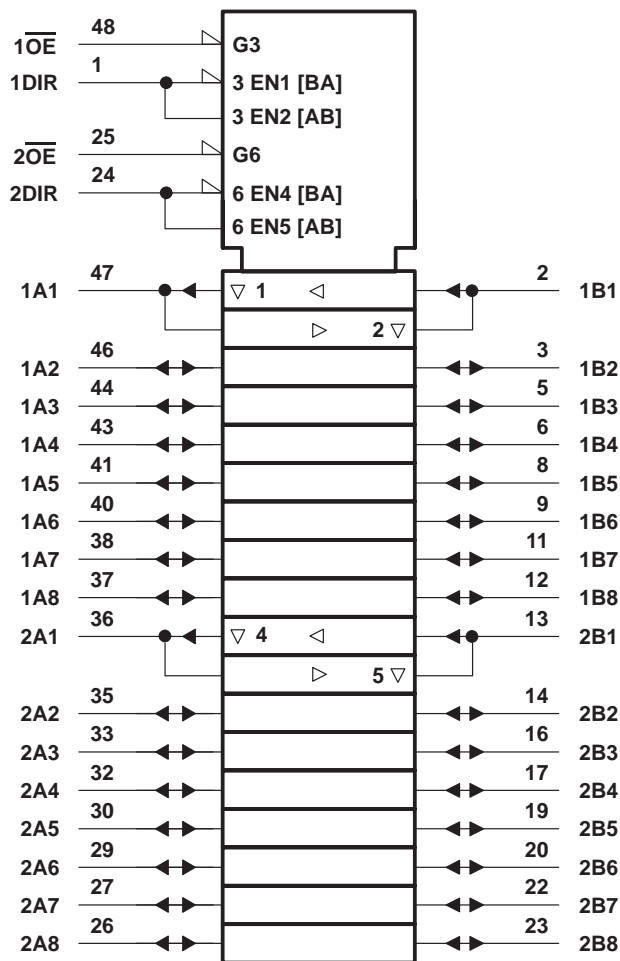
FUNCTION TABLE  
(each 8-bit transceiver)

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

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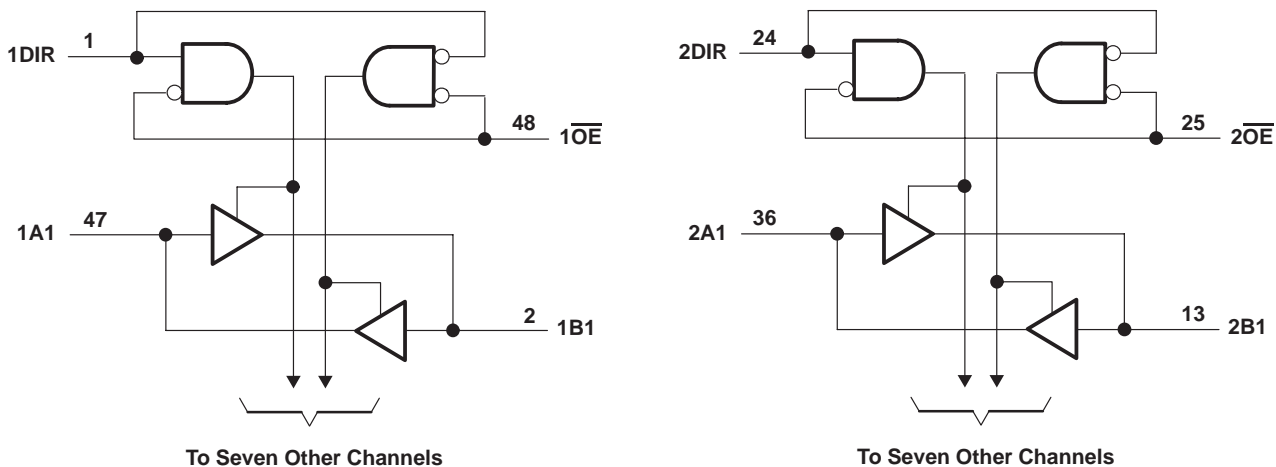
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## logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)





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**recommended operating conditions (see Note 4)**

		MIN	MAX	UNIT	
V <sub>CC</sub>	Supply voltage	Operating	1.4	3.6	V
		Data retention only	1.2		
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 1.2 V	V <sub>CC</sub>		V
		V <sub>CC</sub> = 1.4 V to 1.6 V	0.65 × V <sub>CC</sub>		
		V <sub>CC</sub> = 1.65 V to 1.95 V	0.65 × V <sub>CC</sub>		
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.7		
		V <sub>CC</sub> = 3 V to 3.6 V	2		
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 1.2 V		GND	V
		V <sub>CC</sub> = 1.4 V to 1.6 V		0.35 × V <sub>CC</sub>	
		V <sub>CC</sub> = 1.65 V to 1.95 V		0.35 × V <sub>CC</sub>	
		V <sub>CC</sub> = 2.3 V to 2.7 V		0.7	
		V <sub>CC</sub> = 3 V to 3.6 V		0.8	
V <sub>I</sub>	Input voltage	0	3.6	V	
V <sub>O</sub>	Output voltage	Active state	0	V <sub>CC</sub>	V
		3-state	0	3.6	
I <sub>OHS</sub>	Static high-level output current <sup>†</sup>	V <sub>CC</sub> = 1.4 V to 1.6 V		-2	mA
		V <sub>CC</sub> = 1.65 V to 1.95 V		-4	
		V <sub>CC</sub> = 2.3 V to 2.7 V		-8	
		V <sub>CC</sub> = 3 V to 3.6 V		-12	
I <sub>OLS</sub>	Static low-level output current <sup>†</sup>	V <sub>CC</sub> = 1.4 V to 1.6 V		2	mA
		V <sub>CC</sub> = 1.65 V to 1.95 V		4	
		V <sub>CC</sub> = 2.3 V to 2.7 V		8	
		V <sub>CC</sub> = 3 V to 3.6 V		12	
Δt/Δv	Input transition rise or fall rate	V <sub>CC</sub> = 1.4 V to 3.6 V		5	ns/V
T <sub>A</sub>	Operating free-air temperature		-40	85	°C

<sup>†</sup> Dynamic drive capability is equivalent to standard outputs with I<sub>OH</sub> and I<sub>OL</sub> of ±24 mA at 2.5-V V<sub>CC</sub>. See Figure 1 for V<sub>OL</sub> vs I<sub>OL</sub> and V<sub>OH</sub> vs I<sub>OH</sub> characteristics. Refer to the TI application reports, **AVC Logic Family Technology and Applications**, literature number **SCEA006**, and **Dynamic Output Control (DOC™) Circuitry Technology and Applications**, literature number **SCEA009**.

NOTE 4: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER		TEST CONDITIONS	V <sub>CC</sub>	MIN	TYP†	MAX	UNIT
V <sub>OH</sub>		I <sub>OHS</sub> = -100 μA	1.4 V to 3.6 V	V <sub>CC</sub> -0.2			V
		I <sub>OHS</sub> = -2 mA, V <sub>IH</sub> = 0.91 V	1.4 V	1.05			
		I <sub>OHS</sub> = -4 mA, V <sub>IH</sub> = 1.07 V	1.65 V	1.2			
		I <sub>OHS</sub> = -8 mA, V <sub>IH</sub> = 1.7 V	2.3 V	1.75			
		I <sub>OHS</sub> = -12 mA, V <sub>IH</sub> = 2 V	3 V	2.3			
V <sub>OL</sub>		I <sub>OLS</sub> = 100 μA	1.4 V to 3.6 V			0.2	V
		I <sub>OLS</sub> = 2 mA, V <sub>IL</sub> = 0.49 V	1.4 V			0.4	
		I <sub>OLS</sub> = 4 mA, V <sub>IL</sub> = 0.57 V	1.65 V			0.45	
		I <sub>OLS</sub> = 8 mA, V <sub>IL</sub> = 0.7 V	2.3 V			0.55	
		I <sub>OLS</sub> = 12 mA, V <sub>IL</sub> = 0.8 V	3 V			0.7	
I <sub>I</sub>	Control inputs	V <sub>I</sub> = V <sub>CC</sub> or GND	3.6 V			±2.5	μA
I <sub>off</sub>		V <sub>I</sub> or V <sub>O</sub> = 3.6 V	0			±10	μA
I <sub>OZ</sub> ‡		V <sub>O</sub> = V <sub>CC</sub> or GND, V <sub>I</sub> ( $\overline{\text{OE}}$ ) = V <sub>CC</sub>	3.6 V			±12.5	μA
I <sub>CC</sub>		V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	3.6 V			40	μA
C <sub>i</sub>	Control inputs	V <sub>I</sub> = V <sub>CC</sub> or GND	2.5 V			3	pF
			3.3 V			3	
C <sub>io</sub>	A or B ports	V <sub>O</sub> = V <sub>CC</sub> or GND	2.5 V			9	pF
			3.3 V			9	

† Typical values are measured at T<sub>A</sub> = 25°C.

‡ For I/O ports, the parameter I<sub>OZ</sub> includes the input leakage current.

**switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 2 through 5)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 1.2 V	V <sub>CC</sub> = 1.5 V ± 0.1 V		V <sub>CC</sub> = 1.8 V ± 0.15 V		V <sub>CC</sub> = 2.5 V ± 0.2 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>pd</sub>	A or B	B or A	3.9	0.8	4	0.7	3	0.6	1.9	0.5	1.7	ns
t <sub>en</sub>	$\overline{\text{OE}}$	A or B	8.4	1.5	9.2	1.4	7	1	4.3	0.7	3.7	ns
t <sub>dis</sub>	$\overline{\text{OE}}$	A or B	8.4	2.3	9.3	2.2	7	1.1	4	1.2	3.9	ns

**operating characteristics, T<sub>A</sub> = 25°C**

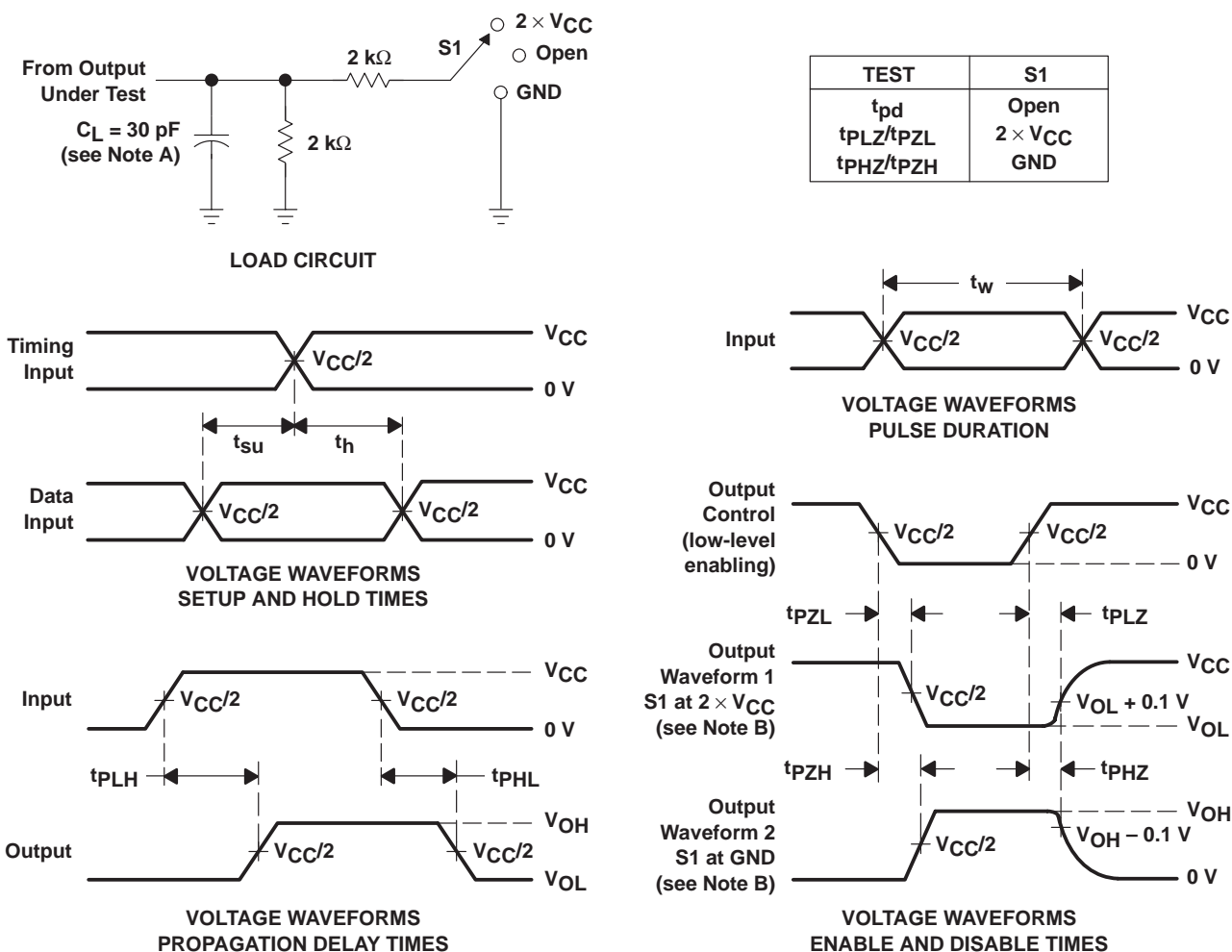
PARAMETER		TEST CONDITIONS	V <sub>CC</sub> = 1.8 V	V <sub>CC</sub> = 2.5 V	V <sub>CC</sub> = 3.3 V	UNIT
			TYP	TYP	TYP	
C <sub>pd</sub>	Power dissipation capacitance	Outputs enabled	35	38	44	pF
		Outputs disabled	6	6	7	

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## PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 1.2\text{ V AND } 1.5\text{ V} \pm 0.1\text{ V}$



- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 2\text{ ns}$ ,  $t_f \leq 2\text{ ns}$ .
  - D. The outputs are measured one at a time with one transition per measurement.
  - E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

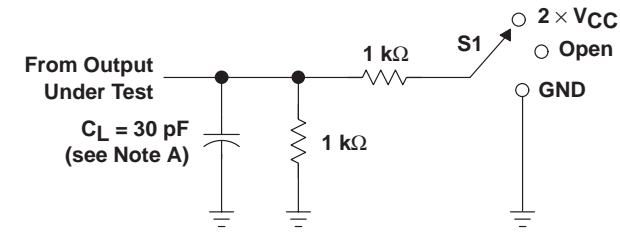
**Figure 2. Load Circuit and Voltage Waveforms**

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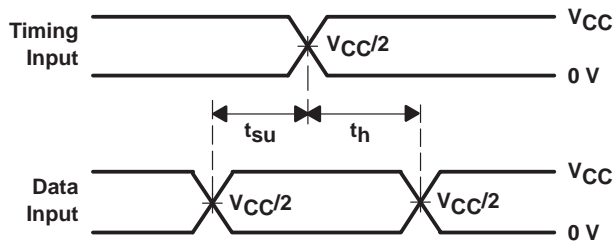
## PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$$

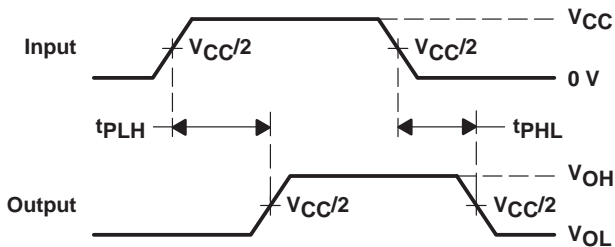


LOAD CIRCUIT

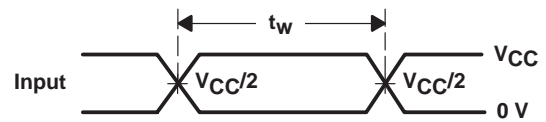
TEST	S1
$t_{pd}$	Open
$t_{PLZ}/t_{PZL}$	2 $\times$ $V_{CC}$
$t_{PHZ}/t_{PZH}$	GND



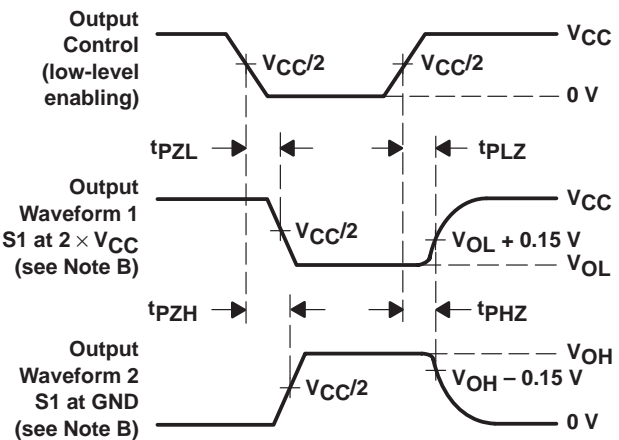
VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES

- NOTES:
- $C_L$  includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2 \text{ ns}$ ,  $t_f \leq 2 \text{ ns}$ .
  - The outputs are measured one at a time with one transition per measurement.
  - $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 3. Load Circuit and Voltage Waveforms

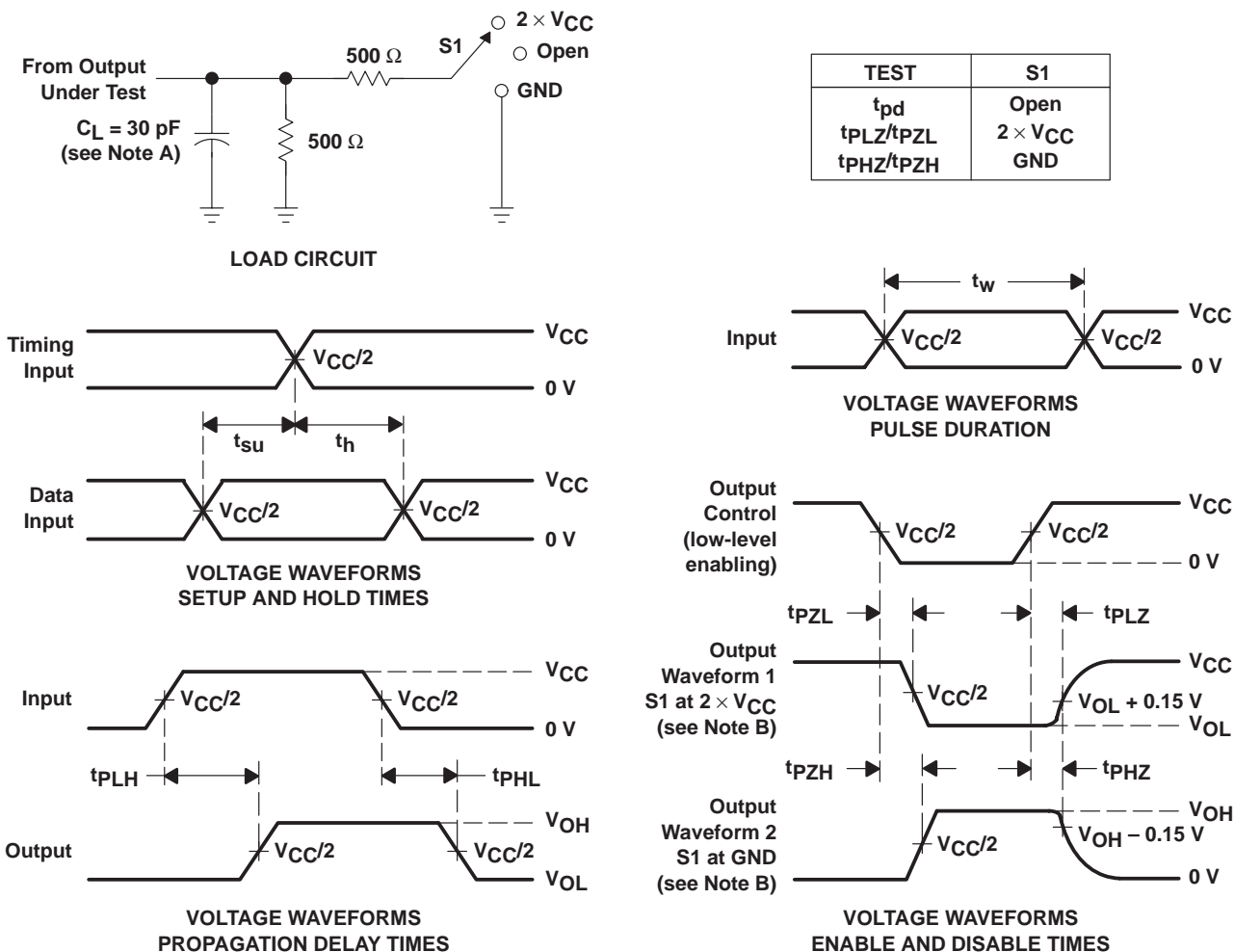


# SN74AVC16245 16-BIT BUS TRANSCEIVER WITH 3-STATE OUTPUTS

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## PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$



- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_O = 50\ \Omega$ ,  $t_r \leq 2\text{ ns}$ ,  $t_f \leq 2\text{ ns}$ .
  - D. The outputs are measured one at a time with one transition per measurement.
  - E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

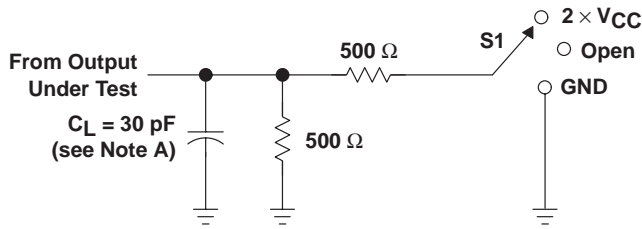
**Figure 4. Load Circuit and Voltage Waveforms**

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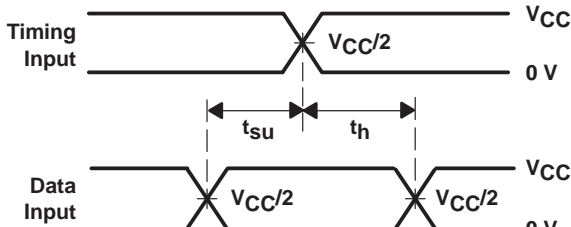
**PARAMETER MEASUREMENT INFORMATION**

$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$

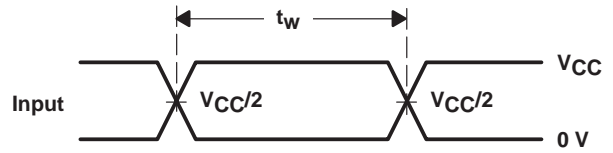


**LOAD CIRCUIT**

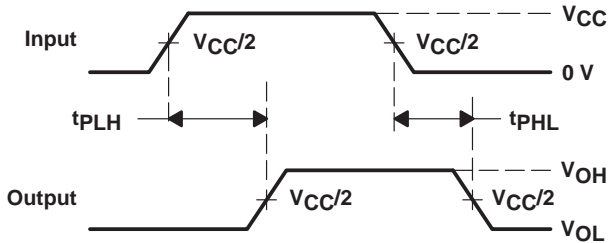
TEST	S1
$t_{pd}$	Open
$t_{PLZ}/t_{PZL}$	$2 \times V_{CC}$
$t_{PHZ}/t_{PZH}$	GND



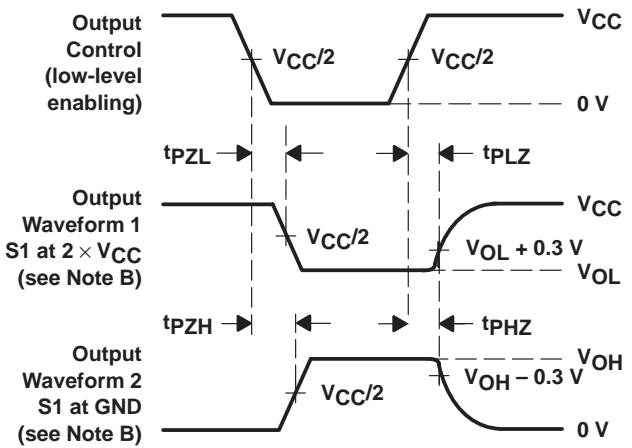
**VOLTAGE WAVEFORMS  
 SETUP AND HOLD TIMES**



**VOLTAGE WAVEFORMS  
 PULSE DURATION**



**VOLTAGE WAVEFORMS  
 PROPAGATION DELAY TIMES**



**VOLTAGE WAVEFORMS  
 ENABLE AND DISABLE TIMES**

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
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 D. The outputs are measured one at a time with one transition per measurement.  
 E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .  
 F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .  
 G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

**Figure 5. Load Circuit and Voltage Waveforms**

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