DGG OR DL PACKAGE

(TOP VIEW)

PRE

SEL0

1A1 3

GND [

1A2

2A3 🛮 17

GND Π

2A4 🛮 19

18

56 CLK

54 1B1

53 GND

52 **1** 1B2

40 **□** 2B3

39 GND

38 **1** 2B4

55 SELEN

- Member of the Texas Instruments Widebus+™ Family
- **EPIC** ™ (Enhanced-Performance Implanted **CMOS) Submicron Process**
- B-Port Outputs Have Equivalent 26- Ω Series Resistors, So No External Resistors **Are Required**
- **UBE** ™ (Universal Bus Exchanger) Allows Synchronous Data Exchange
- **ESD Protection Exceeds 2000 V Per** MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Bus Hold on Data Inputs Eliminates the **Need for External Pullup/Pulldown**
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

NOTE: For tape and reel order entry: The DGGR package is abbreviated to GR.

description

This 9-bit, 4-port universal bus exchanger is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74ALVCH162409 allows synchronous data exchange between four different buses. Data flow is controlled by the select (SEL0-SEL4) inputs. A data-flow state is stored on the rising edge of the clock (CLK) input if the select-enable (SELEN) input is low. Once a data-flow state has been established, data is stored in the flip-flop on the rising edge of CLK if SELEN is high.

1A3 51 **1** 1B3 V_{CC} **∐** 7 50 VCC 1A4 🛮 8 49 1B4 48 🛮 1B5 1A5 📙 1A6 | 10 47 ¶ 1B6 GND II 11 46 ∏ GND 1A7 45 1B7 1A8 13 44 1 1B8 1A9 14 43 1B9 42 2B1 2A1 15 2A2 16 41 2B2

2A5 Π 20 37 **□** 2B5 2A6 21 36 2B6 22 35 [] V_{CC} V_{CC} □ 2A7 23 34 2B7 2A8 24 33 2B8

GND 25 32 GND 2A9 ∏ 26 31 2B9 SEL1 27 30 **∏** SEL4 29 **∏** SEL3 SEL2 [] 28

The data-flow control logic is designed to allow glitch-free data transmission.

The B outputs, which are designed to sink up to 12 mA, include equivalent 26- Ω series resistors to reduce overshoot and undershoot.

When preset (PRE) transitions high, the outputs are disabled immediately, without waiting for a clock pulse. To leave the high-impedance state, both PRE and SELEN must be low and a clock pulse must be applied.

To ensure the high-impedance state during power up or power down, \overline{PRE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH162409 is characterized for operation from -40°C to 85°C.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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SN74ALVCH162409 9-BIT, 4-PORT UNIVERSAL BUS EXCHANGER WITH 3-STATE OUTPUTS SCES189A - FEBRUARY 1999 - REVISED JUNE 1999

Function Tables

	NPUTS	OUTPUT
CLK	SEND PORT	RECEIVE PORT
Х	X	В ₀ †
Х	L	L
Х	Н	Н
1	L	L
1	Н	Н
Н	X	в ₀ †
L	Χ	в ₀ †

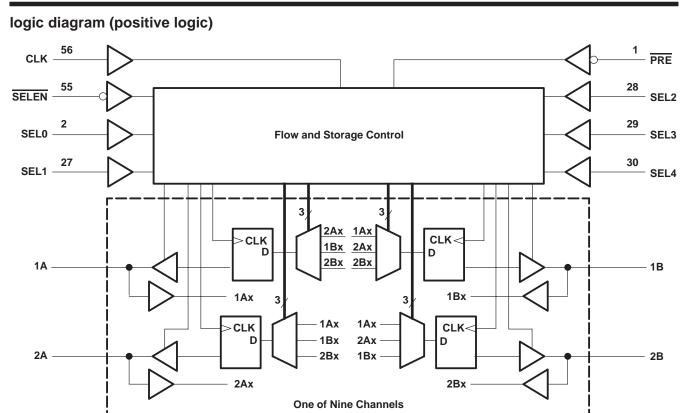
[†] Output level before the indicated steady-state input conditions were established

DATA-FLOW CONTROL

PRE SELEN CLK SELO SEL1 SEL2 SEL3 SEL4 H X X X X X X X No hange L H ↑ X X X X X None, all l/Os off L L ↑ 0 0 0 0 None, all l/Os off L L ↑ 0 0 0 1 Not used L L ↑ 0 0 1 1 Not used L L ↑ 0 0 1 1 Not used L L ↑ 0 0 1 1 Not used L L ↑ 0 0 1 1 Not used L L ↑ 0 0 1 1 Not used L L ↑ 0 0 1 1 Not used	INPUTS							DATA ELOW	
L H ↑ X X X X X None, all I/Os off L L ↑ 0 0 0 0 None, all I/Os off L L ↑ 0 0 0 1 Not used L L ↑ 0 0 1 0 Not used L L ↑ 0 0 1 0 Not used L L ↑ 0 0 1 1 Not used L L ↑ 0 0 1 1 Not used L L ↑ 0 0 1 1 1 Not used L L ↑ 0 0 1 1 Not used L L ↑ 0 1 1 1 Not used L L ↑ 0 1 1 1 Not used L	PRE	SELEN	CLK	SEL0	SEL1	SEL2	SEL3	SEL4	DATA FLOW
L L ↑ 0 0 0 0 None, all I/Os off L L ↑ 0 0 0 1 Not used L L ↑ 0 0 0 1 1 Not used L L ↑ 0 0 1 1 Not used L L ↑ 0 0 1 1 Not used L L ↑ 0 0 1 1 Not used L L ↑ 0 0 1 1 Not used L L ↑ 0 0 1 1 Not used L L ↑ 0 0 1 1 Not used L L ↑ 0 0 1 1 Not used L L ↑ 0 1 1 0 1 1 0 1 1 <td>Н</td> <td>Х</td> <td></td> <td>Х</td> <td>Х</td> <td>Х</td> <td>Χ</td> <td>Х</td> <td>All outputs disabled</td>	Н	Х		Х	Х	Х	Χ	Х	All outputs disabled
L L ↑ 0 0 0 1 Not used L L ↑ 0 0 0 1 0 Not used L L ↑ 0 0 1 0 Not used L L ↑ 0 0 1 1 Not used L L ↑ 0 0 1 1 Not used L L ↑ 0 0 1 1 Not used L L ↑ 0 0 1 1 Not used L L ↑ 0 0 1 1 Not used L L ↑ 0 0 0 2A to 1A and 1B to 2B L L ↑ 0 1 0 0 2A to 1A and 1B to 2B L L ↑ 0 1 0 1 1A to 2A 1B to 1B L	L	Н		X	X	Χ	X	Χ	No change
L L ↑ 0 0 0 1 0 Not used L L ↑ 0 0 1 1 Not used L L ↑ 0 0 1 0 Not used L L ↑ 0 0 1 1 0 Not used L L ↑ 0 0 1 1 0 Not used L L ↑ 0 0 1 1 1 Not used L L ↑ 0 0 1 1 Not used L L ↑ 0 1 0 0 2A to 1A and 1B to 2B L L ↑ 0 1 0 0 2A to 1A and 1B to 2B L L ↑ 0 1 1 0 1 1A to 2A and 1B to 2B L L ↑ 0 1 1	L	L		0	0	0	0	0	None, all I/Os off
L L ↑ 0 0 0 1 1 Not used L L ↑ 0 0 1 0 0 Not used L L ↑ 0 0 1 1 0 Not used L L ↑ 0 0 1 1 0 Not used L L ↑ 0 0 1 1 0 Not used L L ↑ 0 0 1 1 Not used L L ↑ 0 1 1 0 Not used L L ↑ 0 1 0 0 2A to 1A and 1B to 2B L L ↑ 0 1 0 0 1 2A to 1A 1B to 2B L L ↑ 0 1 1 0 1 1A to 2A and 1B to 2B 1B to 1A and 2B to 1B 1B to 1A and 2B to 1B <t< td=""><td>L</td><td>L</td><td></td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>Not used</td></t<>	L	L		0	0	0	0	1	Not used
L L ↑ 0 0 1 0 0 Not used L L ↑ 0 0 1 0 1 Not used L L ↑ 0 0 1 1 0 Not used L L ↑ 0 0 1 1 1 Not used L L ↑ 0 0 1 1 1 Not used L L ↑ 0 1 0 0 2A to 1A and 1B to 2B L L ↑ 0 1 0 0 1 2A to 1A 1B	L	L		0	0	0	1	0	Not used
L L ↑ 0 0 1 0 1 Not used L L ↑ 0 0 1 1 0 Not used L L ↑ 0 0 1 1 1 Not used L L ↑ 0 1 0 0 2A to 1A and 1B to 2B L L ↑ 0 1 0 0 1 2A to 1A 1B to 2B L L ↑ 0 1 0 1 1 2A to 1A and 2B to 1B 1B to 2A and 1B to 2B 1B 1B to 2A and 1B to 2B 1B to 2A and 1B to 2B 1B to 2A 1B to 2A and 2B to 1B 1A to 2A and 2B to 1B 1B to 2B 1B to 1B 1B to 2B 1B to 1B 1B to 1B <td>L</td> <td>L</td> <td></td> <td>0</td> <td>0</td> <td>0</td> <td>1</td> <td>1</td> <td>Not used</td>	L	L		0	0	0	1	1	Not used
L L ↑ 0 0 1 1 0 Not used L L ↑ 0 0 1 1 1 Not used L L ↑ 0 1 0 0 2A to 1A and 1B to 2B L L ↑ 0 1 0 1 0 2B to 1B L L ↑ 0 1 0 1 1 2A to 1A and 2B to 1B L L ↑ 0 1 1 0 1 1A to 2A and 1B to 2B L L ↑ 0 1 1 0 1 1A to 2A and 1B to 2B L L ↑ 0 1 1 0 1 1A to 2A and 1B to 2B L L ↑ 0 1 1 1 1A to 2A and 2B to 1B L L ↑ 1 0 0 0 1A to 1B and 2B to 1B L <td< td=""><td>L</td><td>L</td><td></td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>Not used</td></td<>	L	L		0	0	1	0	0	Not used
L L ↑ 0 0 1 1 1 Not used L L ↑ 0 1 0 0 0 2A to 1A and 1B to 2B L L ↑ 0 1 0 0 1 2A to 1A and 1B to 2B L L ↑ 0 1 0 1 1 2A to 1A L L ↑ 0 1 0 1 1 2A to 1A L L ↑ 0 1 0 1 1 0 1 1A to 2A L L ↑ 0 1 1 0 1 1A to 2A 1B 1B <t< td=""><td>L</td><td>L</td><td></td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>Not used</td></t<>	L	L		0	0	1	0	1	Not used
L L ↑ 0 1 0 0 0 2A to 1A and 1B to 2B L L ↑ 0 1 0 0 1 2A to 1A and 1B to 2B L L ↑ 0 1 0 1 0 2B to 1B L L ↑ 0 1 0 1 1 2A to 1A and 1B to 2B L L ↑ 0 1 0 0 1 1A to 2A and 2B to 1B L L ↑ 0 1 1 0 0 1A to 2A and 1B to 2B L L ↑ 0 1 1 0 1 1A to 2A L L ↑ 0 1 1 1 1 1A to 2A 1B 1B to 2B L L ↑ 1 0 0 0 1A to 1B and 2B to 2A 1B 1B to 2B 1B 1B to 1A 1B to 2B	L	L		0	0	1	1	0	Not used
L L ↑ 0 1 0 0 1 2A to 1A L L ↑ 0 1 0 1 0 2B to 1B L L ↑ 0 1 0 1 1 2A to 1A and 2B to 1B L L ↑ 0 1 1 0 0 1A to 2A and 1B to 2B L L ↑ 0 1 1 0 1 1A to 2A L L ↑ 0 1 1 1 0 1B to 2A L L ↑ 0 1 1 1 0 1B to 2A L L ↑ 1 0 0 0 1A to 1B and 2B to 2B L L ↑ 1 0 0 1 1A to 1B and 2B to 2A L L ↑ 1 0 0 1 1B to 1A and 2A to 2B L L ↑	L	L		0	0	1	1	1	Not used
L L ↑ 0 1 0 1 0 2B to 1B L L ↑ 0 1 0 1 1 2A to 1A and 2B to 1B L L ↑ 0 1 1 0 0 1A to 2A and 1B to 2B L L ↑ 0 1 1 0 1 1A to 2A L L ↑ 0 1 1 0 1B to 2B L L ↑ 0 1 1 1 0 1B to 2A L L ↑ 0 1 1 1 1 1A to 2A and 2B to 1B L L ↑ 1 0 0 0 1A to 1B and 2B to 1B L L ↑ 1 0 0 0 1A to 1B and 2B to 2A L L ↑ 1 0 0 1 1A to 1B and 2A to 2B L L ↑	L	L		0	1	0	0	0	2A to 1A and 1B to 2B
L L ↑ 0 1 0 1 1 2A to 1A and 2B to 1B L L ↑ 0 1 1 0 0 1A to 2A and 1B to 2B L L ↑ 0 1 1 0 1 1A to 2A L L ↑ 0 1 1 1 0 1B to 2B L L ↑ 0 1 1 1 1 1A to 2A and 2B to 1B L L ↑ 1 0 0 0 1A to 1B and 2B to 1B L L ↑ 1 0 0 0 1A to 1B and 2B to 2A L L ↑ 1 0 0 1 1A to 1B and 2B to 2A L L ↑ 1 0 0 1 1A to 1B and 2A to 2B L L ↑ 1 0 1 1 1B to 1A and 2A to 2B L L ↑ <td>L</td> <td>L</td> <td></td> <td>0</td> <td>1</td> <td>0</td> <td>0</td> <td>1</td> <td>2A to 1A</td>	L	L		0	1	0	0	1	2A to 1A
L L ↑ 0 1 1 0 0 1A to 2A and 1B to 2B L L ↑ 0 1 1 0 1 1A to 2A L L ↑ 0 1 1 1 0 1B to 2B L L ↑ 0 1 1 1 1 A to 2A and 2B to 1B L L ↑ 1 0 0 0 1A to 1B and 2B to 1B L L ↑ 1 0 0 0 1A to 1B and 2B to 2A L L ↑ 1 0 0 0 1A to 1B and 2B to 2A L L ↑ 1 0 0 1 1A to 1B and 2B to 2B L L ↑ 1 0 0 1 1A to 1B and 2A to 2B L L ↑ 1 0 0 1B to 1A and 2A to 2B L L ↑ 1 0 1 1B to 1A and 2B to 2A L L ↑ 1 1 0	L	L	1	0	1	0	1	0	2B to 1B
L L ↑ 0 1 1 0 1 1A to 2A L L ↑ 0 1 1 1 0 1B to 2B L L ↑ 0 1 1 1 1A to 2A and 2B to 1B L L ↑ 1 0 0 0 1A to 1B and 2B to 2A L L ↑ 1 0 0 0 1A to 1B and 2B to 2A L L ↑ 1 0 0 1 1A to 1B and 2B to 2A L L ↑ 1 0 0 1 1A to 1B and 2B to 2B L L ↑ 1 0 0 1 1A to 1B and 2B to 2B L L ↑ 1 0 0 1B to 1A and 2A to 2B L L ↑ 1 0 1 1B to 1A and 2B to 2A L L ↑ 1 1 0 0 2B to	L	L		0	1	0	1	1	2A to 1A and 2B to 1B
L L	L	L		0	1	1	0	0	1A to 2A and 1B to 2B
L L ↑ 0 1 1 1 1 1 A to 2A and 2B to 1B L L ↑ 1 0 0 0 0 1A to 1B and 2B to 2A L L ↑ 1 0 0 0 1 1A to 1B and 2B to 2B L L ↑ 1 0 0 1 1 1A to 1B and 2A to 2B L L ↑ 1 0 0 1 1A to 1B and 2A to 2B L L ↑ 1 0 1 0 1 1A to 1B and 2A to 2B L L ↑ 1 0 1 0 1 1B to 1A and 2A to 2B L L ↑ 1 0 1 1 1B to 1A and 2B to 2A L L ↑ 1 0 1 1 1B to 1A and 2B to 2A L L ↑ 1 1 0 0 2B to 1A and 2B to 2A L L ↑ 1 1 0 0 1A to 2B and 1B to 2A <	L	L		0	1	1	0	1	1A to 2A
L L ↑ 1 0 0 0 0 1 1A to 1B and 2B to 2A L L ↑ 1 0 0 0 1 1A to 1B L L ↑ 1 0 0 1 0 2A to 2B L L ↑ 1 0 0 1 1 1 1A to 1B and 2A to 2B L L ↑ 1 0 0 1 1 1 1 1 1 1 0 1 1 1 1 1 1 1 1	L	L		0	1	1	1	0	1B to 2B
L L ↑ 1 0 0 0 1 1A to 1B L L ↑ 1 0 0 1 0 2A to 2B L L ↑ 1 0 0 1 1A to 1B and 2A to 2B L L ↑ 1 0 1 0 1B to 1A and 2A to 2B L L ↑ 1 0 1 0 1 1B to 1A and 2A to 2B L L ↑ 1 0 1 1 1B to 1A 1 1 1B to 1A L L ↑ 1 0 1 1 1B to 1A and 2B to 2A 1 1B to 1A and 2A to 1B 1B to 2A 1	L	L		0	1	1	1	1	1A to 2A and 2B to 1B
L L ↑ 1 0 0 1 0 2A to 2B L L ↑ 1 0 0 1 1 1A to 1B and 2A to 2B L L ↑ 1 0 1 0 1B to 1A and 2A to 2B L L ↑ 1 0 1 0 1 1B to 1A L L ↑ 1 0 1 1 1B to 2A L L ↑ 1 1 0 0 2B to 1A and 2A to 1B L L ↑ 1 1 0 0 2B to 1A and 2A to 1B L L ↑ 1 1 0 0 2B to 1A and 2A to 1B L L ↑ 1 1 0 0 2B to 1A and 2A to 1B L L ↑ 1 1 0 0 1 1B to 2A L L ↑ 1 1 0 1 1A to 2B and 1B to 2A L L ↑ 1 1 <td>L</td> <td>L</td> <td></td> <td>1</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>1A to 1B and 2B to 2A</td>	L	L		1	0	0	0	0	1A to 1B and 2B to 2A
L L ↑ 1 0 0 1 1 1A to 1B and 2A to 2B L L ↑ 1 0 1 0 1B to 1A and 2A to 2B L L ↑ 1 0 1 0 1 1B to 1A L L ↑ 1 0 1 1 0 2B to 2A L L ↑ 1 0 1 1 1B to 1A and 2B to 2A L L ↑ 1 1 0 0 2B to 1A and 2A to 1B L L ↑ 1 1 0 0 2B to 1A and 2A to 1B L L ↑ 1 1 0 0 2B to 1A and 2A to 1B L L ↑ 1 1 0 0 2B to 1A and 2A to 1B L L ↑ 1 1 0 1 1B to 2A L L ↑ 1 1 0 1 1A to 2B and 1B to 2A L L ↑ 1 1	L	L		1	0	0	0	1	1A to 1B
L L ↑ 1 0 1 0 0 1B to 1A and 2A to 2B L L ↑ 1 0 1 0 1 1B to 1A L L ↑ 1 0 1 0 1 1B to 1A L L ↑ 1 0 1 1 0 2B to 2A L L ↑ 1 0 1 1 1 1 1B to 1A and 2B to 2A L L ↑ 1 1 0 0 1 1 1 1B to 1A and 2B to 2A L L ↑ 1 1 0 0 0 2B to 1A and 2A to 1B L L ↑ 1 1 0 0 1 1B to 2A L L ↑ 1 1 0 1 0 2B to 1A L L ↑ 1 1 0 1 0 2B to 1A and 1B to 2A L L ↑ 1 1 0 1 1 2B to 1A and 1B to 2A L L ↑ 1 1 1 0 0 1 1A to 2B and 1B to 2A L L ↑ 1 1 1 1 0 1 2A to 1B	L	L		1	0	0	1	0	2A to 2B
L L ↑ 1 0 1 1B to 1A L L ↑ 1 0 1 1 0 2B to 2A L L ↑ 1 0 1 1 1B to 1A and 2B to 2A L L ↑ 1 1 0 0 0 2B to 1A and 2A to 1B L L ↑ 1 1 0 0 1 1B to 2A L L ↑ 1 1 0 1 0 2B to 1A L L ↑ 1 1 0 1 1 2B to 1A L L ↑ 1 1 0 1 1A to 2B and 1B to 2A L L ↑ 1 1 1 0 1A to 2B and 1B to 2A L L ↑ 1 1 1 0 1A to 2B and 1B to 2A	L	L		1	0	0	1	1	1A to 1B and 2A to 2B
L L ↑ 1 0 1 1 0 2B to 2A L L ↑ 1 0 1 1 1B to 1A and 2B to 2A L L ↑ 1 1 0 0 2B to 1A and 2A to 1B L L ↑ 1 1 0 0 1 1B to 2A L L ↑ 1 1 0 1 0 2B to 1A L L ↑ 1 1 0 1 2B to 1A and 1B to 2A L L ↑ 1 1 0 0 1A to 2B and 1B to 2A L L ↑ 1 1 0 1 1A to 2B L L ↑ 1 1 1 0 2A to 1B	L	L		1	0	1	0	0	1B to 1A and 2A to 2B
L L ↑ 1 0 1 1 1 1B to 1A and 2B to 2A L L ↑ 1 1 0 0 0 2B to 1A and 2A to 1B L L ↑ 1 1 0 0 1 1B to 2A L L ↑ 1 1 0 1 0 2B to 1A L L ↑ 1 1 0 1 1 2B to 1A and 1B to 2A L L ↑ 1 1 1 0 0 1A to 2B and 1B to 2A L L ↑ 1 1 1 0 1 1A to 2B L L ↑ 1 1 1 0 2A to 1B	L	L		1	0	1	0	1	1B to 1A
L L 1 1 0 0 0 2B to 1A and 2A to 1B L L 1 1 0 0 1 1B to 2A L L 1 1 0 1 0 2B to 1A L L 1 1 0 1 1 2B to 1A and 1B to 2A L L 1 1 1 0 0 1A to 2B and 1B to 2A L L 1 1 1 0 1 1A to 2B L L 1 1 1 1 0 2A to 1B	L	L	1	1	0	1	1	0	2B to 2A
L L ↑ 1 1 0 0 1 1B to 2A L L ↑ 1 1 0 1 0 2B to 1A L L ↑ 1 1 0 1 1 2B to 1A and 1B to 2A L L ↑ 1 1 1 0 0 1A to 2B and 1B to 2A L L ↑ 1 1 1 0 1 1A to 2B L L ↑ 1 1 1 0 2A to 1B	L	L		1	0	1	1	1	1B to 1A and 2B to 2A
L L ↑ 1 1 0 1 0 2B to 1A L L ↑ 1 1 0 1 1 2B to 1A and 1B to 2A L L ↑ 1 1 0 0 1A to 2B and 1B to 2A L L ↑ 1 1 1 0 1 1A to 2B L L ↑ 1 1 1 0 2A to 1B	L	L	1	1	1	0	0	0	2B to 1A and 2A to 1B
L L ↑ 1 1 0 1 1 2B to 1A and 1B to 2A L L ↑ 1 1 0 0 1A to 2B and 1B to 2A L L ↑ 1 1 0 1 1A to 2B L L ↑ 1 1 1 0 2A to 1B	L	L		1	1	0	0	1	1B to 2A
L L ↑ 1 1 1 0 0 1A to 2B and 1B to 2A L L ↑ 1 1 0 1 1A to 2B L L ↑ 1 1 1 0 2A to 1B	L	L		1	1	0	1	0	2B to 1A
L L ↑ 1 1 1 0 1 1A to 2B L L ↑ 1 1 1 0 2A to 1B	L	L		1	1_	0	1_	11	2B to 1A and 1B to 2A
L L ↑ 1 1 1 0 2A to 1B	L	L		1	1	1	0	0	1A to 2B and 1B to 2A
	L	L		1	1	1	0	1	1A to 2B
L L ↑ 1 1 1 1 1 1A to 2B and 2A to 1B	L	L		1	1	1	1	0	2A to 1B
	L	L	1	1	1	1	1	1	1A to 2B and 2A to 1B



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	
Input voltage range, V _I : Except I/O ports (see Note 1)	
I/O ports (see Notes 1 and 2)	0.5 V to V _{CC} + 0.5 V
Output voltage range, V _O (see Notes 1 and 2)	
Input clamp current, I _{IK} (V _I < 0)	–50 mA
Output clamp current, I _{OK} (V _O < 0)	–50 mA
Continuous output current, IO	±50 mA
Continuous current through each V _{CC} or GND	±100 mA
Package thermal impedance, θ _{JA} (see Note 3): DGG package	81°C/W
DL package	74°C/W
Storage temperature range, T _{stg}	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

- 2. This value is limited to 4.6 V maximum.
- 3. The package thermal impedance is calculated in accordance with JESD 51.



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recommended operating conditions (see Note 4)

			MIN	MAX	UNIT	
VCC	Supply voltage		1.65	3.6	V	
	$V_{CC} = 1.65 \text{ V to}$		0.65 × V _{CC}			
V_{IH}	High-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		V	
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2			
		V _{CC} = 1.65 V to 1.95 V		0.35 × V _{CC}		
V_{IL}	Low-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	V	
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		0.8		
٧ _I	Input voltage	-	0	VCC	V	
۷o	Output voltage		0	VCC	V	
		V _{CC} = 1.65 V		-4		
ЮН	Light level cutout cumout (A post)	V _{CC} = 2.3 V		-12	mA	
	High-level output current (A port)	V _{CC} = 2.7 V		-12		
		V _{CC} = 3 V		-24		
		V _{CC} = 1.65 V		-2		
	Lligh level cutout current (D next)	V _{CC} = 2.3 V		-6		
	High-level output current (B port)	V _{CC} = 2.7 V		-8		
		V _{CC} = 3 V		-12		
	Output voltage High-level output current (A port) High-level output current (B port) Low-level output current (A port)	V _{CC} = 1.65 V		4		
	Law law law and a submode (A manth)	V _{CC} = 2.3 V		12		
	Low-level output current (A port)	V _{CC} = 2.7 V		12		
la.		V _{CC} = 3 V		24		
lOL		V _{CC} = 1.65 V		2	mA	
	Low lovel output ourrent (P. nort)	V _{CC} = 2.3 V		6		
	Low-level output current (B port)	V _{CC} = 2.7 V		8		
	VCC = 3 V			12		
Δt/Δν	Input transition rise or fall rate	•		10	ns/V	
T _A	Operating free-air temperature		-40	85	°C	

All unused control inputs of the device must be held at VCC or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

$V_{OH} \begin{tabular}{ll} $I_{OH} = -4 \text{ mA} & 1.65 \text{ V} \\ $I_{OH} = -6 \text{ mA} & 2.3 \text{ V} \\ \hline \\ $I_{OH} = -12 \text{ mA} & 2.3 \text{ V} \\ \hline \\ $I_{OH} = -12 \text{ mA} & 2.7 \text{ V} \\ \hline \\ $I_{OH} = -24 \text{ mA} & 3 \text{ V} \\ \hline \\ $I_{OH} = -24 \text{ mA} & 3.0 \text{ V} \\ \hline \\ $I_{OH} = -100 \mu\text{A} & 1.65 \text{ V} \text{ to } 3.6 \text{ V} \text{ V} \\ \hline \\ $I_{OH} = -2 \text{ mA} & 1.65 \text{ V} \\ \hline \\ $I_{OH} = -4 \text{ mA} & 2.3 \text{ V} \\ \hline \end{tabular}$	V _{CC} -0.2 1.2 2 1.7 2.2 2.4 2 V _{CC} -0.2 1.2			
$VOH \begin{tabular}{l l l l l l l l l l l l l l l l l l l $	2 1.7 2.2 2.4 2 V _{CC} -0.2		V	
$VOH \begin{tabular}{ l l l l l l l l l l l l l l l l l l l$	1.7 2.2 2.4 2 V _{CC} -0.2		V	
$VOH \begin{tabular}{c ccccccccccccccccccccccccccccccccccc$	2.2 2.4 2 V _{CC} -0.2 1.2		V	
$VOH \begin{tabular}{c ccccccccccccccccccccccccccccccccccc$	2.4 2 V _{CC} -0.2 1.2			
VOH	2 V _{CC} -0.2 1.2			
$I_{OH} = -100 μA$ 1.65 V to 3.6 V V $I_{OH} = -2 mA$ 1.65 V $I_{OH} = -4 mA$ 2.3 V	V _{CC} -0.2			
$I_{OH} = -100 \mu\text{A}$ 1.65 V to 3.6 V V $I_{OH} = -2 \text{mA}$ 1.65 V $I_{OH} = -4 \text{mA}$ 2.3 V	1.2			
I _{OH} = -4 mA 2.3 V			V	
P nort	1.9			
B port 2.3 V	1.7			
IOH = -6 mA	2.4			
$I_{OH} = -8 \text{ mA}$ 2.7 V	2			
I _{OH} = -12 mA 3 V	2			
$I_{OL} = 100 \mu\text{A}$ 1.65 V to 3.6 V		0.2		
I _{OL} = 4 mA 1.65 V		0.45		
Iou = 6 mA 2.3 V		0.4		
A port 2.3 V		0.7		
I _{OL} = 12 mA 2.7 V		0.4		
I _{OL} = 24 mA 3 V		0.55		
V_{OL} $I_{OL} = 100 \mu A$ $1.65 V \text{ to } 3.6 V$		0.2	V	
I _{OL} = 2 mA 1.65 V		0.45		
I _{OL} = 4 mA 2.3 V		0.4		
B port 2.3 V		0.55		
I _{OL} = 6 mA		0.55		
I _{OL} = 8 mA 2.7 V		0.6		
I _{OL} = 12 mA 3 V		0.8		
$V_{I} = V_{CC}$ or GND 3.6 V		±5	μΑ	
V _I = 0.58 V	25			
V _I = 1.07 V	-25			
V _I = 0.7 V	45			
I _I (hold) 2.3 V	-45		μΑ	
VI = 0.8 V	75			
V _I = 2 V	- 75			
$V_1 = 0 \text{ to } 3.6 \text{ V}^{\ddagger}$ 3.6 V	,	±500		
IOZ $VO = VCC$ or GND 3.6 V		±10	μΑ	
ICC $V_I = V_{CC}$ or GND, $I_O = 0$ 3.6 V		40	μΑ	
ΔICC One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND 3 V to 3.6 V		750	μΑ	
C_i Control inputs $V_1 = V_{CC}$ or GND 3.3 V			pF	
C _{io} A or B ports V _O = V _{CC} or GND 3.3 V	:		pF	

[†] All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

[§] For I/O ports, the parameter I_{OZ} includes the input leakage current.



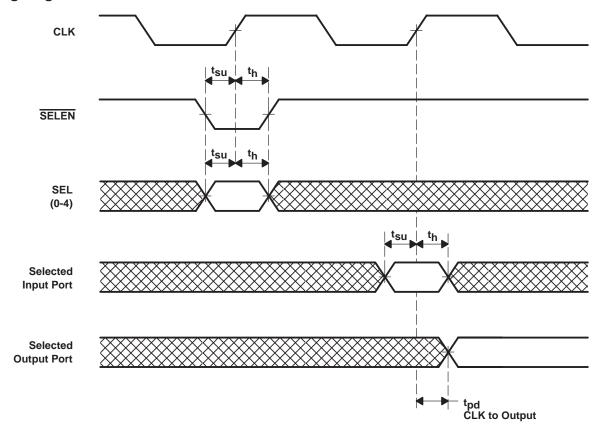
[‡] This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

SN74ALVCH162409 9-BIT, 4-PORT UNIVERSAL BUS EXCHANGER WITH 3-STATE OUTPUTS SCES189A – FEBRUARY 1999 – REVISED JUNE 1999

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

			V _{CC} =	1.8 V	V _{CC} =		V _{CC} =	2.7 V	V _{CC} =		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
fclock	Clock frequency										MHz
t _W	Pulse duration, CLK high or low										ns
	Setup time	A or B before CLK↑									ns
١.		SEL before CLK↑									
t _{su}		SELEN before CLK↑									
		PRE before CLK↑									
	Hold time	A or B after CLK↑									
th		SEL after CLK↑									ns
		SELEN after CLK↑									

timing diagram





9-BIT, 4-PORT UNIVERSAL BUS EXCHANGER WITH 3-STATE OUTPUTS

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switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

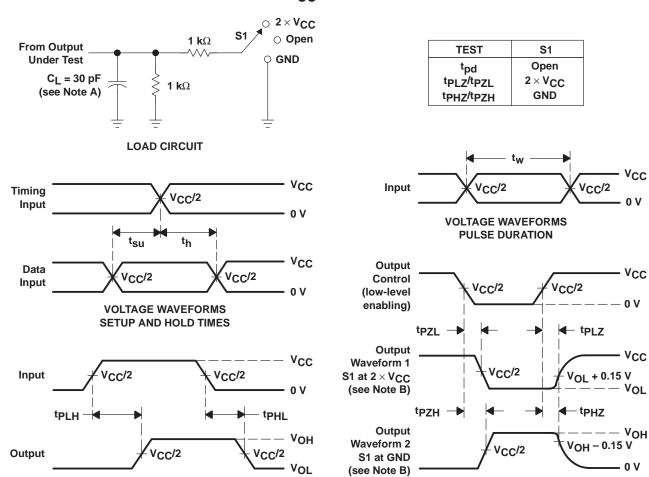
PARAMETER	FROM TO (INPUT) (OUTPUT)		V _{CC} = 1.8 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT	
	(INPUT) (OUTPUT)	(001F01)	MIN	TYP	MIN	MAX	MIN	MAX	MIN	MAX		
fmax											MHz	
t _{pd}	CLK	A or B									ns	
t _{en}	CLK	A or B									ns	
+	CLK	A or B									Τ	
^t dis	PRE	AUID									ns	

operating characteristics, $T_A = 25^{\circ}C$

PARAMETER			TEST COI	NDITIONS	V _{CC} = 1.8 V TYP	V _{CC} = 2.5 V TYP	V _{CC} = 3.3 V TYP	UNIT
	Power dissipation	All outputs enabled	C. 50 pF	f 40 MH=				~F
C _{pd}	capacitance	All outputs disabled	$C_L = 50 \text{ pF},$	f = 10 MHz				pF

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PARAMETER MEASUREMENT INFORMATION V_{CC} = 1.8 V



- NOTES: A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

VOLTAGE WAVEFORMS

ENABLE AND DISABLE TIMES

- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_r \leq$ 2 ns. $t_f \leq$ 2 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.

VOLTAGE WAVEFORMS

PROPAGATION DELAY TIMES

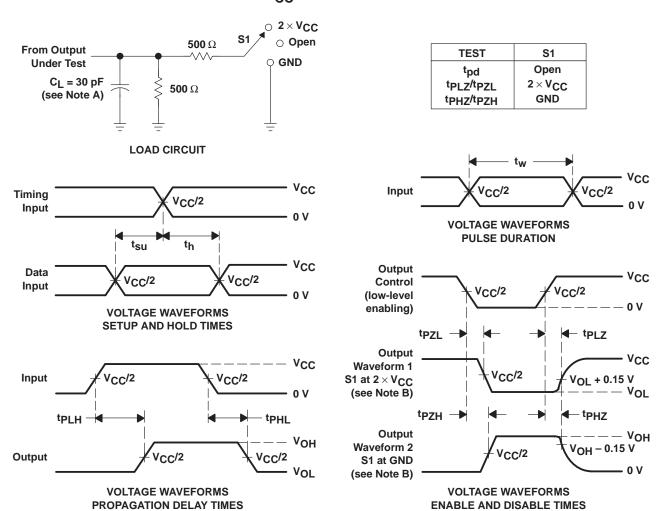
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms



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PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.5 V \pm 0.2 V



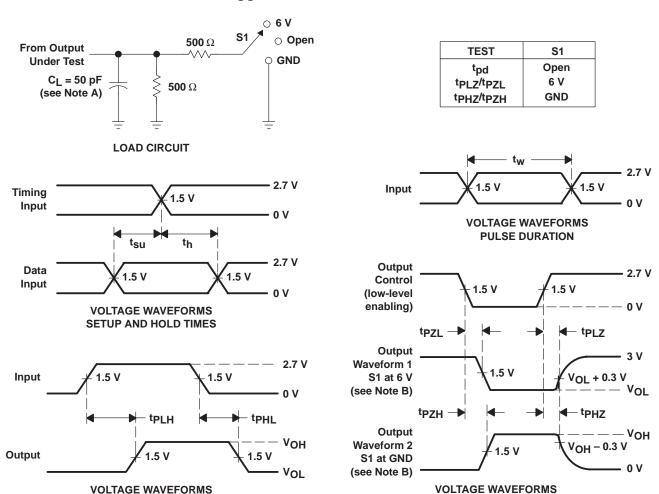
- NOTES: A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_Q = 50 \Omega$, $t_r \leq 2$ ns, $t_f \leq 2$ ns.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tpLz and tpHz are the same as tdis.
 - F. tpzL and tpzH are the same as ten.
 - G. tpLH and tpHL are the same as tpd.

Figure 2. Load Circuit and Voltage Waveforms



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PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.7 V AND 3.3 V \pm 0.3 V



- NOTES: A. C_I includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

ENABLE AND DISABLE TIMES

- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_Q = 50 \Omega$, $t_f \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpl 7 and tpHZ are the same as tdis.

PROPAGATION DELAY TIMES

- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 3. Load Circuit and Voltage Waveforms



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