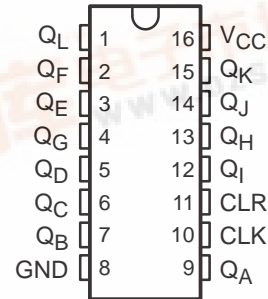
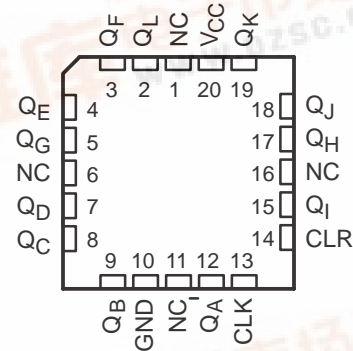


- **EPIC™** (Enhanced-Performance Implanted CMOS) Process
- Typical  $V_{OLP}$  (Output Ground Bounce)  $<0.8\text{ V}$  at  $V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$
- Typical  $V_{OHV}$  (Output  $V_{OH}$  Undershoot)  $>2.3\text{ V}$  at  $V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$
- 2-V to 5.5-V  $V_{CC}$  Operation
- Support Mixed-Mode Voltage Operation on All Ports
- High On-Off Output-Voltage Ratio
- Low Crosstalk Between Switches
- Individual Switch Controls
- Extremely Low Input Current
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)
- Package Options Include Plastic Small-Outline (D, NS), Shrink Small-Outline (DB), Thin Very Small-Outline (DGV), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Ceramic (J) DIPs

SN54LV4040A ... J OR W PACKAGE  
SN74LV4040A ... D, DB, DGV, NS, OR PW PACKAGE  
(TOP VIEW)



SN54LV4040A ... FK PACKAGE  
(TOP VIEW)



NC – No internal connection

## description

The 'LV4040A devices are 12-bit asynchronous binary counters with the outputs of all stages available externally. A high level at the clear (CLR) input asynchronously clears the counter and resets all outputs low. The count is advanced on a high-to-low transition at the clock (CLK) input. Applications include time-delay circuits, counter controls, and frequency-dividing circuits.

The SN54LV4040A is characterized for operation over the full military temperature range of  $-55^\circ\text{C}$  to  $125^\circ\text{C}$ . The SN74LV4040A is characterized for operation from  $-40^\circ\text{C}$  to  $85^\circ\text{C}$ .

FUNCTION TABLE  
(each buffer)

INPUTS		FUNCTION
CLK	CLR	
↑	L	No change
↓	L	Advance to next stage
X	H	All outputs L

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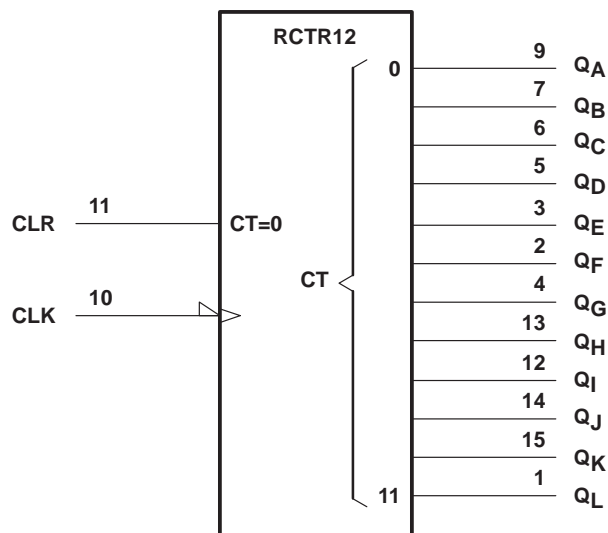
UNLESS OTHERWISE NOTED this document contains PRODUCTION DATA information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

# SN54LV4040A, SN74LV4040A

## 12-BIT ASYNCHRONOUS BINARY COUNTERS

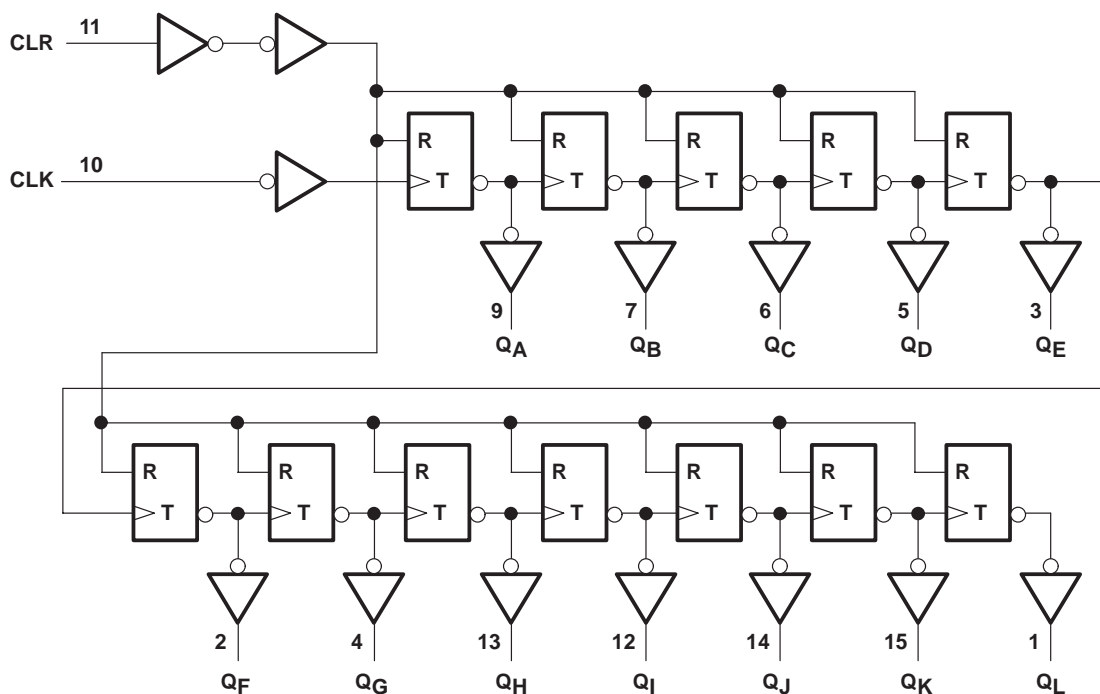
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### logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.  
Pin numbers shown are for the D, DB, DGV, J, NS, PW, and W packages.

### logic diagram (positive logic)



Pin numbers shown are for the D, DB, DGV, J, NS, PW, and W packages.

# SN54LV4040A, SN74LV4040A

## 12-BIT ASYNCHRONOUS BINARY COUNTERS

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### absolute maximum ratings over operating free-air temperature range†

Supply voltage range, $V_{CC}$	–0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high-impedance or power-off state, $V_O$ (see Note 1)	–0.5 V to 7 V
Output voltage range, $V_O$ (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	–20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	±50 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	±25 mA
Continuous current through $V_{CC}$ or GND	±50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 3): D package	73°C/W
DB package	82°C/W
DGV package	120°C/W
NS package	64°C/W
PW package	108°C/W
Storage temperature range, $T_{stg}$	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
  2. This value is limited to 5.5 V maximum.
  3. The package thermal impedance is calculated in accordance with JESD 51.

# SN54LV4040A, SN74LV4040A

## 12-BIT ASYNCHRONOUS BINARY COUNTERS

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### recommended operating conditions (see Note 4)

			SN54LV4040A		SN74LV4040A		UNIT
			MIN	MAX	MIN	MAX	
V <sub>CC</sub>	Supply voltage		2	5.5	2	5.5	V
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 2 V	1.5		1.5		V
		V <sub>CC</sub> = 2.3 V to 2.7 V	V <sub>CC</sub> × 0.7		V <sub>CC</sub> × 0.7		
		V <sub>CC</sub> = 3 V to 3.6 V	V <sub>CC</sub> × 0.7		V <sub>CC</sub> × 0.7		
		V <sub>CC</sub> = 4.5 V to 5.5 V	V <sub>CC</sub> × 0.7		V <sub>CC</sub> × 0.7		
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 2 V		0.5		0.5	V
		V <sub>CC</sub> = 2.3 V to 2.7 V		V <sub>CC</sub> × 0.3		V <sub>CC</sub> × 0.3	
		V <sub>CC</sub> = 3 V to 3.6 V		V <sub>CC</sub> × 0.3		V <sub>CC</sub> × 0.3	
		V <sub>CC</sub> = 4.5 V to 5.5 V		V <sub>CC</sub> × 0.3		V <sub>CC</sub> × 0.3	
V <sub>I</sub>	Input voltage		0	5.5	0	5.5	V
V <sub>O</sub>	Output voltage		0	V <sub>CC</sub>	0	V <sub>CC</sub>	V
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 2 V		–50		–50	μA
		V <sub>CC</sub> = 2.3 V to 2.7 V		–2		–2	
		V <sub>CC</sub> = 3 V to 3.6 V		–6		–6	mA
		V <sub>CC</sub> = 4.5 V to 5.5 V		–12		–12	
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 2 V		50		50	μA
		V <sub>CC</sub> = 2.3 V to 2.7 V		2		2	
		V <sub>CC</sub> = 3 V to 3.6 V		6		6	mA
		V <sub>CC</sub> = 4.5 V to 5.5 V		12		12	
Δt/Δv	Input transition rise or fall rate	V <sub>CC</sub> = 2.3 V to 2.7 V	0	200	0	200	ns/V
		V <sub>CC</sub> = 3 V to 3.6 V	0	100	0	100	
		V <sub>CC</sub> = 4.5 V to 5.5 V	0	20	0	20	
T <sub>A</sub>	Operating free-air temperature		–55	125	–40	85	°C

NOTE 4: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

# SN54LV4040A, SN74LV4040A 12-BIT ASYNCHRONOUS BINARY COUNTERS

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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	SN54LV4040A			SN74LV4040A			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V <sub>OH</sub>	I <sub>OH</sub> = -50 μA	2 V to 5.5 V	V <sub>CC</sub> -0.1			V <sub>CC</sub> -0.1			V
	I <sub>OH</sub> = -2 mA	2.3 V	2			2			
	I <sub>OH</sub> = -6 mA	3 V	2.48			2.48			
	I <sub>OH</sub> = -12 mA	4.5 V	3.8			3.8			
V <sub>OL</sub>	I <sub>OL</sub> = 50 μA	2 V to 5.5 V	0.1			0.1			V
	I <sub>OL</sub> = 2 mA	2.3 V	0.4			0.4			
	I <sub>OL</sub> = 6 mA	3 V	0.44			0.44			
	I <sub>OL</sub> = 12 mA	4.5 V	0.55			0.55			
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	0 V to 5.5 V	±1			±1			μA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V	20			20			μA
I <sub>off</sub>	V <sub>I</sub> or V <sub>O</sub> = 0 to 5.5 V	0 V	5			5			μA
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	3.3 V	1.9			1.9			pF

**timing requirements over recommended operating free-air temperature range, V<sub>CC</sub> = 2.5 V ± 0.2 V (unless otherwise noted) (see Figure 1)**

		T <sub>A</sub> = 25°C	SN54LV4040A		SN74LV4040A		UNIT
			MIN	MAX	MIN	MAX	
t <sub>w</sub> Pulse duration	CLK high or low	7	7	7	7	7	ns
	CLR high	6.5	6.5	6.5	6.5	6.5	
t <sub>su</sub> Setup time	CLR inactive before CLK↓	6.5	6.5	6.5	6.5	6.5	ns

**timing requirements over recommended operating free-air temperature range, V<sub>CC</sub> = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)**

		T <sub>A</sub> = 25°C	SN54LV4040A		SN74LV4040A		UNIT
			MIN	MAX	MIN	MAX	
t <sub>w</sub> Pulse duration	CLK high or low	5	5	5	5	5	ns
	CLR high	5	5	5	5	5	
t <sub>su</sub> Setup time	CLR inactive before CLK↓	5	5	5	5	5	ns

**timing requirements over recommended operating free-air temperature range, V<sub>CC</sub> = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)**

		T <sub>A</sub> = 25°C	SN54LV4040A		SN74LV4040A		UNIT
			MIN	MAX	MIN	MAX	
t <sub>w</sub> Pulse duration	CLK high or low	5	5	5	5	5	ns
	CLR high	5	5	5	5	5	
t <sub>su</sub> Setup time	CLR inactive before CLK↓	5	5	5	5	5	ns

# SN54LV4040A, SN74LV4040A

## 12-BIT ASYNCHRONOUS BINARY COUNTERS

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**switching characteristics over recommended operating free-air temperature range,  
V<sub>CC</sub> = 2.5 V ± 0.2 V (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T <sub>A</sub> = 25°C			SN54LV4040A		SN74LV4040A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f <sub>max</sub>			C <sub>L</sub> = 15 pF	50*	115*		40*		40		MHz
			C <sub>L</sub> = 50 pF	40	95		35		35		
t <sub>PLH</sub>	CLK	Q <sub>A</sub>	C <sub>L</sub> = 15 pF	8.7* 19.4*			1*	23*	1	23	ns
t <sub>PHL</sub>				8.7* 19.4*			1*	23*	1	23	
t <sub>PHL</sub>	CLR	Any Q	C <sub>L</sub> = 15 pF	9.3* 19.9*			1*	24*	1	24	ns
t <sub>PLH</sub>	$\overline{\text{CLK}}$	Q <sub>A</sub>	C <sub>L</sub> = 50 pF	10.5 24.1			1	28	1	28	ns
t <sub>PHL</sub>				10.5 24.1			1	28	1	28	
t <sub>PHL</sub>	CLR	Any Q	C <sub>L</sub> = 50 pF	11.7 24.5			1	28	1	28	ns
Δt <sub>pd</sub>	Q <sub>n</sub>	Q <sub>n+1</sub>	C <sub>L</sub> = 50 pF	1.7 5.9				7		7	ns

\* On products compliant to MIL-PRF-38535, this parameter is not production tested.

**switching characteristics over recommended operating free-air temperature range,  
V<sub>CC</sub> = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T <sub>A</sub> = 25°C			SN54LV4040A		SN74LV4040A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f <sub>max</sub>			C <sub>L</sub> = 15 pF	75*	160*		75*		75		MHz
			C <sub>L</sub> = 50 pF	55	130		50		50		
t <sub>PLH</sub>	CLK	Q <sub>A</sub>	C <sub>L</sub> = 15 pF	6.1* 11.9*			1*	14*	1	14	ns
t <sub>PHL</sub>				6.1* 11.9*			1*	14*	1	14	
t <sub>PHL</sub>	CLR	Any Q	C <sub>L</sub> = 15 pF	7.1* 12.8*			1*	15*	1	15	ns
t <sub>PLH</sub>	$\overline{\text{CLK}}$	Q <sub>A</sub>	C <sub>L</sub> = 50 pF	7.5 15.4			1	17.5	1	17.5	ns
t <sub>PHL</sub>				7.5 15.4			1	17.5	1	17.5	
t <sub>PHL</sub>	CLR	Any Q	C <sub>L</sub> = 50 pF	9 16.3			1	18.5	1	18.5	ns
Δt <sub>pd</sub>	Q <sub>n</sub>	Q <sub>n+1</sub>	C <sub>L</sub> = 50 pF	1.2 4.4				5		5	ns

\* On products compliant to MIL-PRF-38535, this parameter is not production tested.

**switching characteristics over recommended operating free-air temperature range,  
V<sub>CC</sub> = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T <sub>A</sub> = 25°C			SN54LV4040A		SN74LV4040A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f <sub>max</sub>			C <sub>L</sub> = 15 pF	150*	235*		125*		125		MHz
			C <sub>L</sub> = 50 pF	95	185		80		80		
t <sub>PLH</sub>	CLK	Q <sub>A</sub>	C <sub>L</sub> = 15 pF	4.2* 7.3*			1*	8.5*	1	8.5	ns
t <sub>PHL</sub>				4.2* 7.3*			1*	8.5*	1	8.5	
t <sub>PHL</sub>	CLR	Any Q	C <sub>L</sub> = 15 pF	5.3* 8.6*			1*	10*	1	10	ns
t <sub>PLH</sub>	$\overline{\text{CLK}}$	Q <sub>A</sub>	C <sub>L</sub> = 50 pF	5.3 9.3			1	10.5	1	10.5	ns
t <sub>PHL</sub>				5.3 9.3			1	10.5	1	10.5	
t <sub>PHL</sub>	CLR	Any Q	C <sub>L</sub> = 50 pF	6.8 10.6			1	12	1	12	ns
Δt <sub>pd</sub>	Q <sub>n</sub>	Q <sub>n+1</sub>	C <sub>L</sub> = 50 pF	0.8 3.1				3.5		3.5	ns

\* On products compliant to MIL-PRF-38535, this parameter is not production tested.

# SN54LV4040A, SN74LV4040A 12-BIT ASYNCHRONOUS BINARY COUNTERS

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noise characteristics,  $V_{CC} = 3.3\text{ V}$ ,  $C_L = 50\text{ pF}$ ,  $T_A = 25^\circ\text{C}$  (see Note 5)

PARAMETER		SN74LV4040A			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic $V_{OL}$		0.5	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic $V_{OL}$		–0.5	–0.8	V
$V_{IH(D)}$	High-level dynamic input voltage	2.31			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.99	V

NOTE 5: Characteristics are for surface-mount packages only.

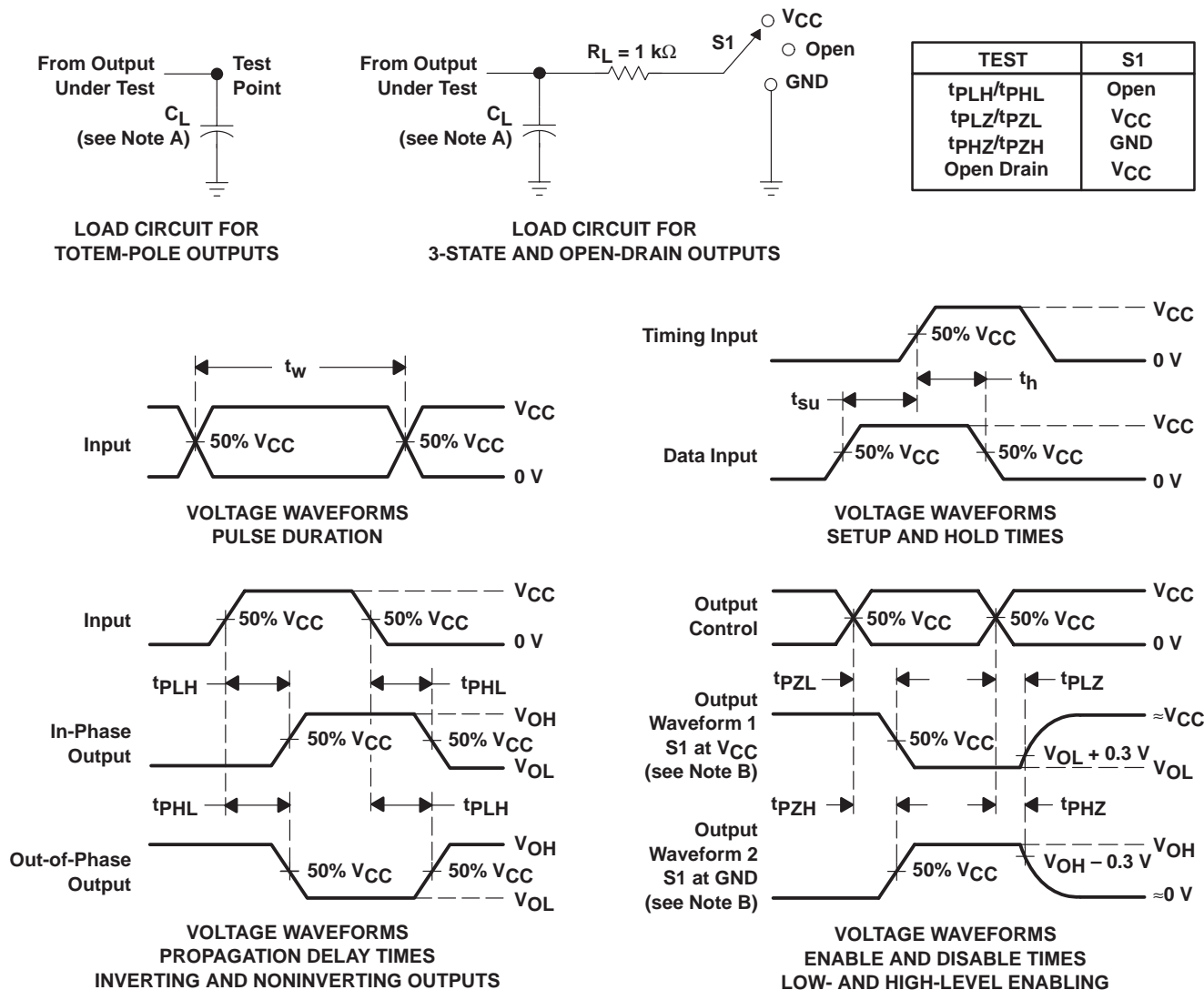
operating characteristics,  $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	$V_{CC}$	TYP	UNIT
$C_{pd}$	Power dissipation capacitance	$C_L = 50\text{ pF}$ , $f = 10\text{ MHz}$	3.3 V	11.9	pF
			5 V	13.1	

# SN54LV4040A, SN74LV4040A 12-BIT ASYNCHRONOUS BINARY COUNTERS

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## PARAMETER MEASUREMENT INFORMATION



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 3\text{ ns}$ ,  $t_f \leq 3\text{ ns}$ .  
 D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms



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