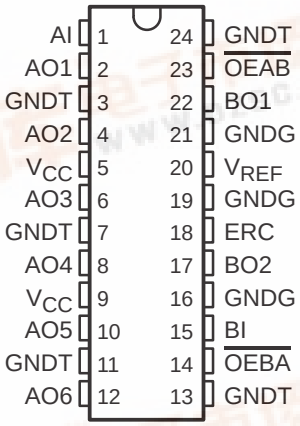
SN74GTLP817
GTL+-TO-LVTTL 1-TO-6 FANOUT DRIVER

SCES285A – OCTOBER 1999 – REVISED DECEMBER 1999

- **Bidirectional Interface Between GTL+ Signal Levels and LVTTL Logic Levels**
- **GTL+-to-LVTTL 1-to-6 Fanout Driver**
- **LVTTL-to-GTL+ 1-to-2 Fanout Driver**
- **LVTTL Interfaces Are 5-V Tolerant**
- **Medium-Drive GTL+ Outputs (50 mA)**
- **Reduced-Drive LVTTL Outputs (–12 mA/12 mA)**
- **Variable Edge-Rate Control (ERC) Input Selects GTL+ Rise and Fall Times for Optimal Data-Transfer Rate and Signal Integrity**
- **I_{off} and Power-Up 3-State Support Hot Insertion**
- **Distributed GND-Pin Configuration Minimizes High-Speed Switching Noise**
- **Package Options Include Plastic Small-Outline (DW), Thin Very Small-Outline (DGV), and Thin Shrink Small-Outline (PW) Packages**

DGV, DW, OR PW PACKAGE
(TOP VIEW)



description

The SN74GTLP817 is a low-drive fanout driver that provides LVTTL-to-GTL+ and GTL+-to-LVTTL signal-level translation. The device provides a high-speed interface between cards operating at LVTTL logic levels and a backplane operating at GTL+ signal levels. High-speed (about two times faster than standard TTL or LVTTL) backplane operation is a direct result of GTLP's reduced output swing (<1 V), reduced input threshold levels, improved differential input, and output edge control (OEC™). Improved GTLP OEC circuits minimize bus settling time and have been designed and tested using several backplane models. The medium drive is suitable for driving double-terminated backplanes.

GTL+ is the Texas Instruments derivative of the Gunning transceiver logic (GTL) JEDEC standard JESD 8-3. The AC specification of the SN74GTLP817 is given only at the preferred higher noise margin GTL+, but the user has the flexibility of using this device at either GTL (V_{TT} = 1.2 V and V_{REF} = 0.8 V) or GTL+ (V_{TT} = 1.5 V and V_{REF} = 1 V) signal levels.

Normally, the B port operates at GTL or GTL+ levels, while the A-port and control inputs are compatible with LVTTL logic levels and are 5-V tolerant. V_{REF} is the reference input voltage for the B port.

GNDT is the TTL output ground, while GNDG is the GTL+ output ground, and both should be separated from each other for a quieter device.

This device is fully specified for hot-insertion applications using I_{off} and power-up 3-state. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

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description (continued)

This device features adjustable edge-rate control (ERC). Changing the ERC input voltage between GND and V_{CC} adjusts the B-port output rise and fall times. This allows the designer to optimize system data-transfer rate and signal integrity to the backplane load.

When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, the output-enable ($\overline{OE}$) input should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74GTLP817 is characterized for operation from –40°C to 85°C.

functional description

The SN74GTLP817 is a fanout driver providing LVTTL-to-GTL+ translation and GTL+-to-LVTTL translation in the same package.

The LVTTL-to-GTL+ direction is a 1-to-2 fanout driver with a single output enable ($\overline{OEAB}$).

The GTL+-to-LVTTL direction is a 1-to-6 fanout driver with a single output enable ($\overline{OEBA}$).

Data polarity is inverting for both directions.

Function Tables

A TO B

INPUTS		OUTPUT	MODE
AI	$\overline{OEAB}$	BOn	
H	L	L	Inverted transparent
L	L	H	Inverted transparent
X	H	Z	Isolation

B TO A

INPUTS		OUTPUT	MODE
BI	$\overline{OEBA}$	AOn	
H	L	L	Inverted transparent
L	L	H	Inverted transparent
X	H	Z	Isolation

B-PORT EDGE-RATE CONTROL (ERC)

INPUT ERC		OUTPUT B-PORT EDGE RATE
LOGIC LEVEL	NOMINAL VOLTAGE	
H	V_{CC}	Slow
L	GND	Fast

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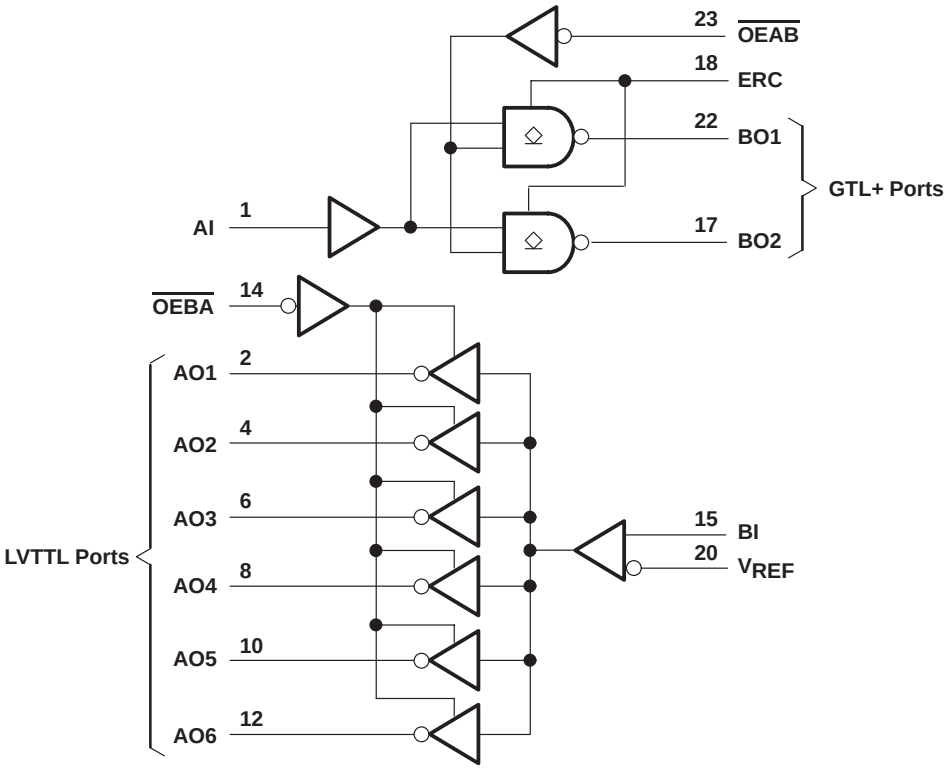
logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . . –0.5 V to 7 V
Voltage range applied to any output in the high-impedance or power-off state, V_O
(see Note 1) . . . . . –0.5 V to 7 V
Voltage range applied to any output in the high or low state, V_O
(see Note 1): A port . . . . . –0.5 V to V_{CC} + 0.5 V
B port . . . . . –0.5 V to 4.6 V
Current into any output in the low state, I_O: A port . . . . . 24 mA
B port . . . . . 100 mA
Current into any A-port output in the high state, I_O (see Note 2) . . . . . 24 mA
Continuous current through each V_{CC} or GND . . . . . ±100 mA
Input clamp current, I_{IK} (V_I < 0) . . . . . –50 mA
Output clamp current, I_{OK} (V_O < 0) . . . . . –50 mA
Package thermal impedance, θ_{JA} (see Note 3): DGV package . . . . . 86°C/W
DW package . . . . . 46°C/W
PW package . . . . . 88°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Notes 4 through 6)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		3.15	3.3	3.45	V
V_{TT}	Termination voltage	GTL	1.14	1.2	1.26	V
		GTL+	1.35	1.5	1.65	
V_{REF}	Supply voltage	GTL	0.74	0.8	0.87	V
		GTL+	0.87	1	1.1	
V_I	Input voltage	BI			V_{TT}	V
		AI, $\overline{OE}$			V_{CC}	
V_{IH}	High-level input voltage	BI	V_{REF}+0.05			V
		ERC	V_{CC}–0.6	V_{CC}	515	
		AI, $\overline{OE}$	2			
V_{IL}	Low-level input voltage	BI			V_{REF}–0.05	V
		ERC		GND	0.6	
		AI, $\overline{OE}$			0.8	
I_{IK}	Input clamp current				–18	mA
I_{OH}	High-level output current	AO port			–12	mA
I_{OL}	Low-level output current	AO port			12	mA
		BO port			50	
T_A	Operating free-air temperature		–40		85	°C

NOTES: 4. All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.
5. Normal connection sequence is GND first and V_{CC} = 3.3 V, I/O, control inputs, V_{TT}, V_{REF} (any order) last.
6. V_{TT} and R_{TT} can be adjusted to accommodate backplane impedances as long as they do not exceed the DC absolute I_{OL} ratings. Similarly, V_{REF} can be adjusted to optimize noise margins, but normally is 2/3 V_{TT}.

electrical characteristics over recommended operating free-air temperature range for GTL+ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 3.15 V,	I_I = –18 mA			–1.2	V
V_{OH}	AO port	V_{CC} = 3.15 V to 3.45 V,	I_{OH} = –100 µA	V_{CC}–0.2			V
		V_{CC} = 3.15 V	I_{OH} = –100 µA	V_{CC}–0.2			
			I_{OH} = –6 mA	2.4			
			I_{OH} = –12 mA	2.2			
V_{OL}	AO port	V_{CC} = 3.15 V to 3.45 V,	I_{OL} = 100 µA			0.2	V
		V_{CC} = 3.15 V	I_{OL} = 100 µA			0.2	
			I_{OL} = 6 mA			0.4	
			I_{OL} = 12 mA			0.5	
	BO port	V_{CC} = 3.15 V	I_{OL} = 100 µA			0.2	
			I_{OL} = 40 mA			0.5	
			I_{OL} = 50 mA			0.55	
I_I	BI	V_{CC} = 3.45 V	V_I = 0 or 1.5 V			±5	µA
	AI, $\overline{OE}$, ERC		V_I = 0 or 5.5 V			±5	
I_{OZ}	AO port	V_{CC}= 3.45 V	V_O = 0 or 5.5 V			±5	µA
	BO port		V_O = 1.5 V			5	
I_{CC}	AO or BO port	V_{CC} = 3.45 V, I_O = 0, V_I (A-port or control input) = V_{CC} or GND V_I (B port) = V_{TT} or GND	Outputs high			10	mA
			Outputs low			10	
			Outputs disabled			10	
ΔI_{CC}‡	AI, $\overline{OE}$	V_{CC} = 3.45 V, One A-port or control input at 3.45 V, Other A-port or control inputs at V_{CC} or GND, V_I = V_{CC} –0.6				1	mA
C_i	AI, $\overline{OE}$, ERC	V_I = V_{CC} or 0					pF
	BI	V_I = V_{TT} or 0					
C_o	AO port	V_O = V_{CC} or 0					pF
	BO port	V_O = V_{TT} or 0					

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ This is the increase in supply current for each input that is at the specified LVTTL voltage level rather than V_{CC} or GND.

hot-insertion specifications for A port over recommended operating free-air temperature range

PARAMETER	TEST CONDITIONS			MIN	MAX	UNIT
I_{off}	V_{CC} = 0,	V_I or V_O = 0 to 5.5 V			30	µA
I_{OZPU}	V_{CC} = 0 to 1.5 V,	V_O = 0.5 V to 3 V,	$\overline{OE}$ = 0		±100	µA
I_{OZPD}	V_{CC} = 1.5 V to 0,	V_O = 0.5 V to 3 V,	$\overline{OE}$ = 0		±100	µA

hot-insertion specifications for B port over recommended operating free-air temperature range

PARAMETER	TEST CONDITIONS			MIN	MAX	UNIT
I_{off}	V_{CC} = 0,	V_I or V_O = 0 to 1.5 V			30	µA
I_{OZPU}	V_{CC} = 0 to 1.5 V,	V_O = 0.5 V to 1.5 V,	$\overline{OE}$ = 0		±100	µA
I_{OZPD}	V_{CC} = 1.5 V to 0,	V_O = 0.5 V to 1.5 V,	$\overline{OE}$ = 0		±100	µA

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature, V_{TT} = 1.5 V and V_{REF} = 1 V for GTL+ (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	EDGE RATE†	MIN	TYP‡	MAX	UNIT
t_{PLH}	AI	BO	Slow				ns
			Fast				
t_{PHL}	AI	BO	Slow				ns
			Fast				
t_{en}	$\overline{OEAB}$	BO	Slow				ns
			Fast				
t_{dis}	$\overline{OEAB}$	BO	Slow				ns
			Fast				
t_r	Rise time, B outputs (20% to 80%)		Slow				ns
			Fast				
t_f	Fall time, B outputs (80% to 20%)		Slow				ns
			Fast				
t_r	Rise time, A outputs (10% to 90%)						ns
t_f	Fall time, A outputs (90% to 10%)						ns
t_{PLH}	BI	AO					ns
t_{PHL}							
t_{en}	$\overline{OEBA}$	AO					ns
t_{dis}	$\overline{OEBA}$	AO					ns

† Slow (ERC = V_{CC}) and Fast (ERC = GND)
‡ All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

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extended electrical characteristics over recommended ranges of supply voltage and operating free-air temperature, V_{REF} = 1 V (unless otherwise noted), C_L = 30 pF for B port, and C_L = 50 pF for A port

PARAMETER	FROM (INPUT)	TO (OUTPUT)	EDGE RATE†	MIN	TYP‡	MAX	UNIT
$t_{sk(LH)}$ (see Note 7)	A	B	Slow				ns
			Fast				
$t_{sk(HL)}$ (see Note 7)	A	B	Slow				ns
			Fast				
$t_{sk(pp)}$ (see Notes 8 and 9)	A	B	Slow				ns
			Fast				
$t_{sk(LH)}$ (see Note 7)	$\overline{B}$	A					ns
$t_{sk(HL)}$ (see Note 7)	$\overline{B}$	A					ns
t_{OST}	B	A					ns
t_{PV}	B	A					ns

† Slow (ERC = V_{CC}) and Fast (ERC = GND)

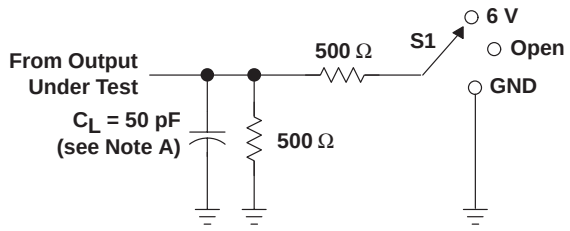
‡ All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

NOTES: 7. Output-to-output skew is defined as the absolute value of the difference between the actual propagation delay for all outputs within the same packaged device. The specifications are given for specific worst case V_{CC} and temperature and apply to any outputs switching in the same direction either high to low ($t_{sk(HL)}$) or low to high ($t_{sk(LH)}$), or in opposite directions, both HL and LH (t_{OST}). This parameter is specified by design and statistical-process distribution. Actual skew values between the GTLP outputs could vary on the backplane due to the loading and impedance seen by the device.

8. Part-to-part skew is defined as the absolute value of the difference between the actual propagation design for all outputs from device to device. The parameter is specified for a specific worst case V_{CC} and temperature. The parameter is specified by design and statistical-process distribution. Actual skew values between the GTLP outputs could vary on the backplane due to the loading and impedance seen by the device.

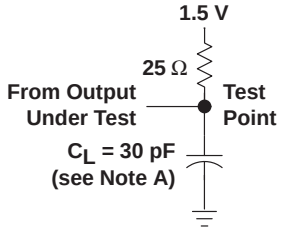
9. Due to the open-drain structure on GTLP outputs, t_{OST} and $t_{sk(pp)}$ in the A-to-B direction are not specified. Skew on these paths is dependent on the V_{TT} and R_{TT} values on the backplane.

PARAMETER MEASUREMENT INFORMATION

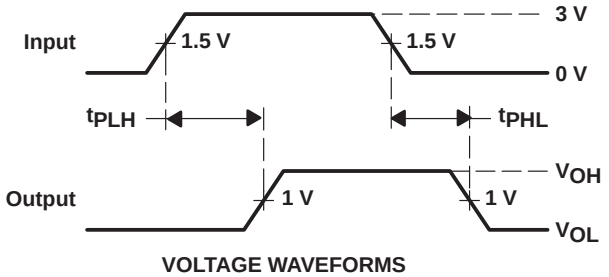


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND

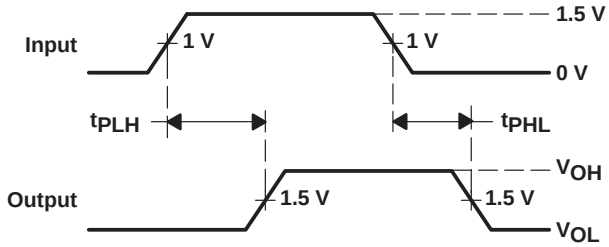
LOAD CIRCUIT FOR A OUTPUTS



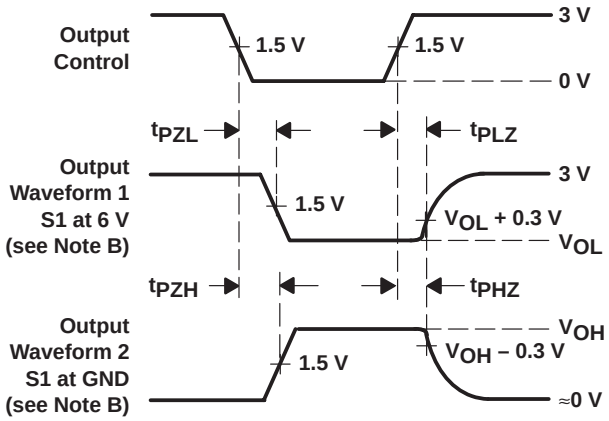
LOAD CIRCUIT FOR B OUTPUTS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
(A port to B port)



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
(B port to A port)



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
(A port)

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, slew rate ≤ 1 V/ns.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

DISTRIBUTED-LOAD BACKPLANE SWITCHING CHARACTERISTICS

This data sheet is specified for and tested to the lump load shown in Figure 1. However, the designer probably uses this GTLP device in a distributed load like that shown in Figure 2, in which actual B-port backplane switching characteristics are different. Therefore, the device is modeled as shown in Figure 3, which very closely matches the results obtained using Figure 2. Switching characteristics based on Figure 3 more closely match actual backplane design requirements.

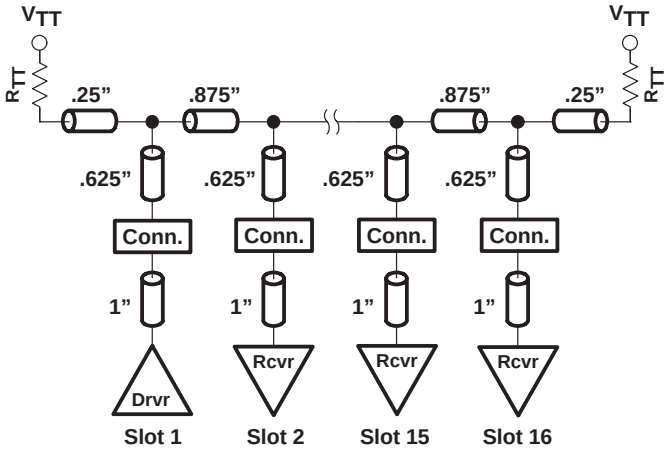


Figure 2. Test Backplane Model

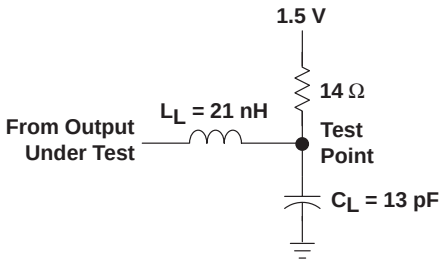


Figure 3. Distributed-Load Circuit for B Outputs

PRODUCT PREVIEW

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, V_{TT} = 1.5 V and V_{REF} = 1 V for GTL+ (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	EDGE RATE†	MIN	TYP‡	MAX	UNIT
t_{PLH}	AI	BO	Slow				ns
			Fast				
t_{PHL}	AI	BO	Slow				ns
			Fast				
t_{en}	$\overline{OEAB}$	BO	Slow				ns
			Fast				
t_{dis}	$\overline{OEAB}$	BO	Slow				ns
			Fast				
t_r	Rise time, B outputs (20% to 80%)		Slow				ns
			Fast				
t_f	Fall time, B outputs (80% to 20%)		Slow				ns
			Fast				
t_{sko} (see Note 8)	AI	BO	Slow				ns
			Fast				
$t_{sk(pp)}$ (see Notes 8 and 9)	AI	BO	Slow				ns
			Fast				

† Slow (ERC = V_{CC}) and Fast (ERC = GND)
‡ All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

NOTES: 8. Part-to-part skew is defined as the absolute value of the difference between the actual propagation design for all outputs from device to device. The parameter is specified for a specific worst case V_{CC} and temperature. The parameter is specified by design and statistical-process distribution. Actual skew values between the GTLP outputs could vary on the backplane due to the loading and impedance seen by the device.

9. Due to the open-drain structure on GTLP outputs, t_{OST} and $t_{sk(pp)}$ in the A-to-B direction are not specified. Skew on these paths is dependent on the V_{TT} and R_{TT} values on the backplane.

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