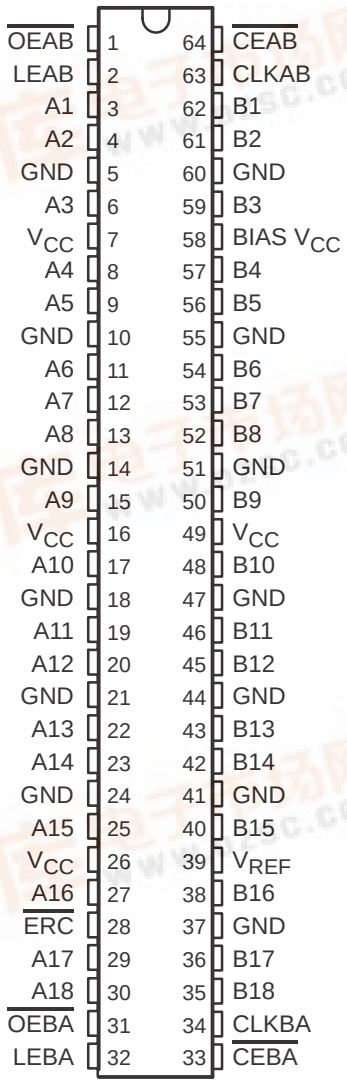
- ***UBT***™ **(Universal Bus Transceiver) Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, Clocked, or Clock-Enabled Mode**
- **Bidirectional Interface Between GTL+ Signal Levels and LVTTL Logic Levels**
- **Equivalent to ’16601 Function**
- **LVTTL Interfaces Are 5-V Tolerant**
- **High-Drive GTL+ Outputs (100 mA)**
- **LVTTL Outputs (–24 mA/24 mA)**
- **Variable Edge-Rate Control ($\overline{ERC}$) Input Selects GTL+ Rise and Fall Times for Optimal Data-Transfer Rate and Signal Integrity**
- **I_{off}, Power-Up 3-State, and BIAS V_{CC} Support Live Insertion**
- **Bus Hold on A-Port Data Inputs**
- **Distributed V_{CC} and GND-Pin Configuration Minimizes High-Speed Switching Noise**
- **Packaged in Plastic Thin Shrink Small-Outline Package**

DGG PACKAGE
(TOP VIEW)



description

The SN74GTLPH1612 is a high-drive 18-bit universal bus transceiver (UBT) that provides LVTTL-to-GTL+ and GTL+-to-LVTTL signal-level translation. It allows for transparent, latched, clocked, or clock-enabled modes of data transfer identical to the ’16601 function. The device provides a high-speed interface between cards operating at LVTTL logic levels and a backplane operating at GTL+ signal levels. High-speed (about two times faster than standard TTL or LVTTL) backplane operation is a direct result of GTLP’s reduced output swing (<1 V), reduced input threshold levels, improved differential input, and output edge control (OEC™). Improved GTLP OEC circuits minimize bus settling time and have been designed and tested using several backplane models. The high drive is suitable for driving double-terminated low-impedance backplanes using incident-wave switching.

PRODUCT PREVIEW

OEC and UBT are trademarks of Texas Instruments Incorporated.

description (continued)

GTL+ is the Texas Instruments derivative of the Gunning transceiver logic (GTL) JEDEC standard JESD 8-3. The AC specification of the SN74GTLPH1612 is given only at the preferred higher noise margin GTL+, but the user has the flexibility of using this device at either GTL (V_{TT} = 1.2 V and V_{REF} = 0.8 V) or GTL+ (V_{TT} = 1.5 V and V_{REF} = 1 V) signal levels.

Normally, the B port operates at GTL or GTL+ levels, while the A-port and control inputs are compatible with LVTTL logic levels and are 5-V tolerant. V_{REF} is the reference input voltage for the B port.

This device is fully specified for live-insertion applications using I_{off}, power-up 3-state, and BIAS V_{CC}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict. The BIAS V_{CC} circuitry precharges and preconditions the B-port input/output connections, preventing disturbance of active data on the backplane during card insertion or removal, and permits true live-insertion capability.

High-drive GTLP backplane interface devices feature adjustable edge-rate control ($\overline{ERC}$). Changing the $\overline{ERC}$ input voltage between GND and V_{CC} adjusts the B-port output rise and fall times. This allows the designer to optimize system data-transfer rate and signal integrity to the backplane load.

Active bus-hold circuitry is provided to hold unused or undriven LVTTL inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, the output-enable ($\overline{OE}$) input should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74GTLPH1612 is characterized for operation from –40°C to 85°C.

functional description

The SN74GTLPH1612 is a high-drive (100 mA) 36-bit UBT containing D-type latches and D-type flip-flops for data-path operation in transparent, latched, clocked, or clock-enabled modes and can replace any of the functions shown in Table 1.

Table 1. SN74GTLPH1612 UBT Replacement Functions

FUNCTION	8 BIT	9 BIT	10 BIT	16 BIT	18 BIT
Transceiver	’245, ’623, ’645	’863	’861	’16245, ’16623	’16863
Buffer/Driver	’241, ’244, ’541		’827	’16241, ’16244, ’16541	’16825
Latched transceiver	’543			’16543	’16472
Latch	’373, ’573	’843	’841	’16373	’16843
Registered transceiver	’646, ’652			’16646, ’16652	’16474
Flip-flop	’374, ’574		’821	’16374	
Standard UBT					’16500, ’16501
Universal bus driver					’16835
Registered transceiver with CLK enable	’2952			’16470, ’16952	
Flip-flop with CLK enable	’377	’823			’16823
Standard UBT with CLK enable					’16600, ’16601
SN74GTLPH1612 UBT replaces all above functions					

functional description (continued)

Data flow in each direction is controlled by output-enable ($\overline{OEAB}$ and $\overline{OEBA}$), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. The clock can be controlled by clock-enable ($\overline{CEAB}$ and $\overline{CEBA}$) inputs. $\overline{OEAB}$ and $\overline{OEBA}$ control the 18 bits of data for the A-to-B and B-to-A directions, respectively.

For A-to-B data flow, the devices operate in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if $\overline{CEAB}$ is low and CLKAB is held at a high or low logic level. If LEAB is low, the A data is stored in the latch/flip-flop on the low-to-high transition of CLKAB if $\overline{CEAB}$ also is low. When $\overline{OEAB}$ is low, the outputs are active. When $\overline{OEAB}$ is high, the outputs are in the high-impedance state.

Data flow for B to A is similar to that for A to B, buses $\overline{OEBA}$, LEBA, CLKBA, and $\overline{CEBA}$.

Function Tables

OUTPUT ENABLE†

INPUTS					OUTPUT B	MODE
$\overline{CEAB}$	$\overline{OEAB}$	LEAB	CLKAB	A		
X	H	X	X	X	Z	Isolation
L	L	L	H	X	B_0‡	Latched storage of A data
L	L	L	L	X	B_0§	
X	L	H	X	L	L	Transparent
X	L	H	X	H	H	
L	L	L	↑	L	L	Clocked storage of A data
L	L	L	↑	H	H	
H	L	L	X	X	B_0§	Clock inhibit

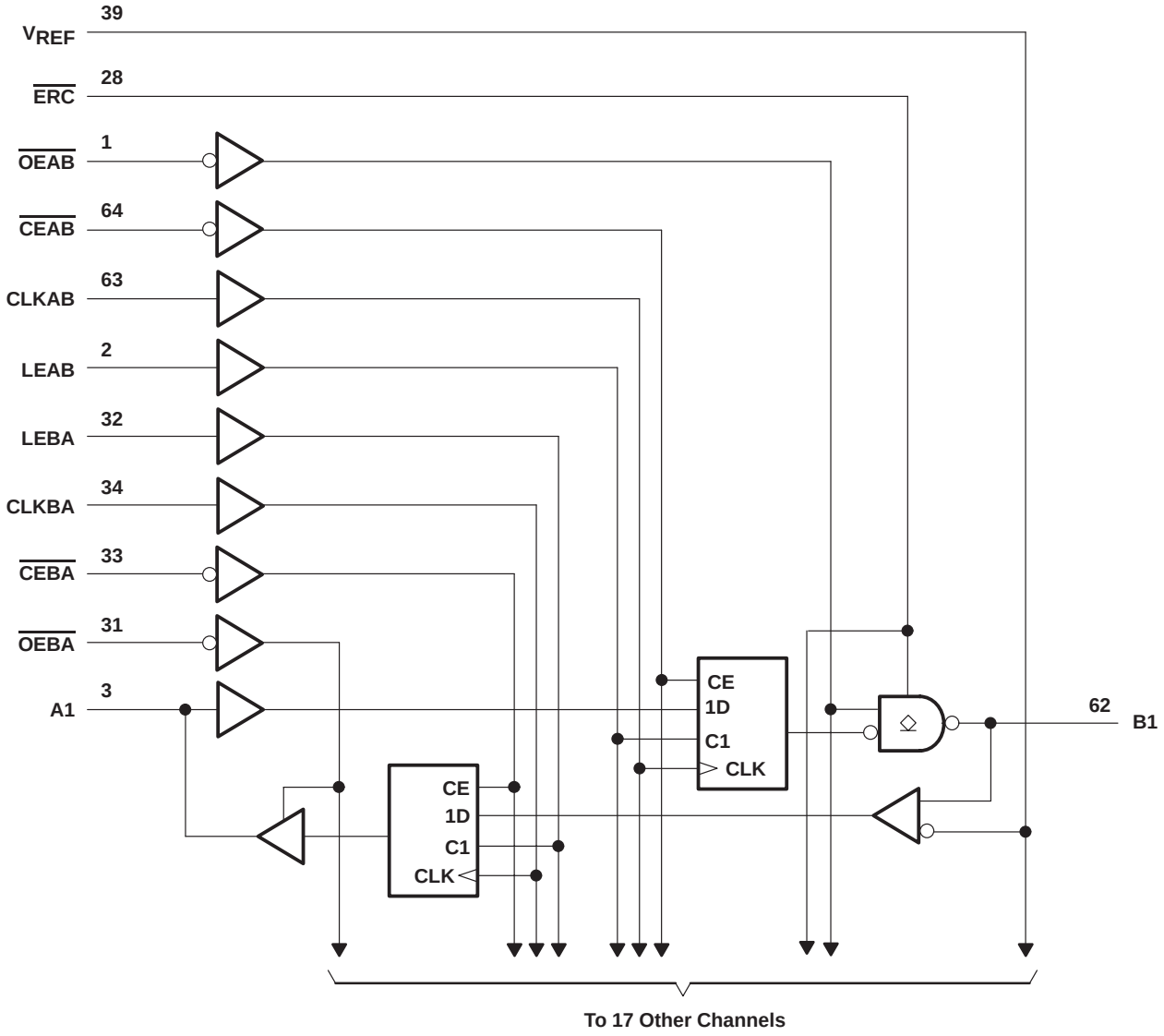
† A-to-B data flow is shown: B-to-A data flow is similar but uses $\overline{OEBA}$, LEBA, CLKBA, and $\overline{CEBA}$.
‡ Output level before the indicated steady-state input conditions were established, provided that CLKAB was high before LEAB went low
§ Output level before the indicated steady-state input conditions were established

B-PORT EDGE-RATE CONTROL ($\overline{ERC}$)

INPUT $\overline{ERC}$		OUTPUT B-PORT EDGE RATE
LOGIC LEVEL	NOMINAL VOLTAGE	
L	GND	Slow
H	V_{CC}	Fast

PRODUCT PREVIEW

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} and BIAS V_{CC} . . . . . –0.5 V to 4.6 V
Input voltage range, V_I (see Note 1): A-port and control inputs . . . . . –0.5 V to 7 V
B port, $\overline{ERC}$, and V_{REF} . . . . . –0.5 V to 4.6 V
Voltage range applied to any output in the high-impedance or power-off state, V_O
(see Note 1): A port . . . . . –0.5 V to 7 V
B port . . . . . –0.5 V to 4.6 V
Voltage range applied to any output in the high or low state, V_O
(see Note 1): A port . . . . . –0.5 V to V_{CC} + 0.5 V
B port . . . . . –0.5 V to 4.6 V
Current into any output in the low state, I_O: A port . . . . . 48 mA
B port . . . . . 200 mA
Current into any A-port output in the high state, I_O (see Note 2) . . . . . 48 mA
Continuous current through each V_{CC} or GND . . . . . ±100 mA
Input clamp current, I_{IK} (V_I < 0) . . . . . –50 mA
Output clamp current, I_{OK} (V_O < 0) . . . . . –50 mA
Package thermal impedance, θ_{JA} (see Note 3) . . . . . 55°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
3. The package thermal impedance is calculated in accordance with JESD 51.

PRODUCT PREVIEW

recommended operating conditions (see Notes 4 through 6)

			MIN	NOM	MAX	UNIT
V_{CC}, BIAS V_{CC}	Supply voltage		3.15	3.3	3.45	V
V_{TT}	Termination voltage	GTL	1.14	1.2	1.26	V
		GTL+	1.35	1.5	1.65	
V_{REF}	Supply voltage	GTL	0.74	0.8	0.87	V
		GTL+	0.87	1	1.1	
V_I	Input voltage	B port			V_{TT}	V
		Except B port			V_{CC}	
V_{IH}	High-level input voltage	B port	V_{REF}+0.05			V
		$\overline{ERC}$	V_{CC} –0.6	V_{CC}		
		Except B port and $\overline{ERC}$	2			
V_{IL}	Low-level input voltage	B port			V_{REF}–0.05	V
		$\overline{ERC}$		GND	0.6	
		Except B port and $\overline{ERC}$			0.8	
I_{IK}	Input clamp current				–18	mA
I_{OH}	High-level output current	A port			–24	mA
I_{OL}	Low-level output current	A port			24	mA
		B port			100	
T_A	Operating free-air temperature		–40		85	°C

NOTES: 4. All unused control and B-port inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

5. Normal connection sequence is GND first, BIAS V_{CC} = 3.3 V second, and V_{CC} = 3.3 V, I/O, control inputs, V_{TT} and V_{REF} (any order) last. However, if the B-port I/O precharge is not required, the acceptable connection sequence is GND first and V_{CC} = 3.3 V, BIAS V_{CC} = 3.3 V, I/O, control inputs, V_{TT} and V_{REF} (any order) last. When V_{CC} is connected, the BIAS V_{CC} circuitry is disabled.

6. V_{TT} and R_{TT} can be adjusted to accommodate backplane impedances as long as they do not exceed the DC absolute I_{OL} ratings. Similarly, V_{REF} can be adjusted to optimize noise margins, but normally is 2/3 V_{TT}.

electrical characteristics over recommended operating free-air temperature range for GTL+ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 3.15 V,	I_I = –18 mA			–1.2	V
V_{OH}	A port	V_{CC} = 3.15 V to 3.45 V,	I_{OH} = –100 μA	V_{CC}–0.2			V
		V_{CC} = 3.15 V	I_{OH} = –12 mA	2.4			
			I_{OH} = –24 mA	2			
V_{OL}	A port	V_{CC} = 3.15 V to 3.45 V,	I_{OL} = 100 μA			0.2	V
		V_{CC} = 3.15 V	I_{OL} = 12 mA			0.4	
			I_{OL} = 24 mA			0.5	
	B port	V_{CC} = 3.15 V	I_{OL} = 10 mA			0.2	
			I_{OL} = 64 mA			0.4	
			I_{OL} = 100 mA			0.55	
I_I‡	B port	V_{CC} = 3.45 V,	V_I = 0 to 1.5 V			±10	μA
	A-port and control inputs	V_{CC} = 3.45 V	V_I = 0 or V_{CC}			±10	
			V_I = 5.5 V			±20	
I_{BHL}§	A port	V_{CC} = 3.15 V,	V_I = 0.8 V	75			μA
I_{BHH}¶	A port	V_{CC} = 3.15 V,	V_I = 2 V	–75			μA
I_{BHLO}#	A port	V_{CC} = 3.45 V,	V_I = 0 to V_{CC}			500	μA
I_{BHHO}‖	A port	V_{CC} = 3.45 V,	V_I = 0 to V_{CC}			–500	μA
I_{CC}	A or B port	V_{CC} = 3.45 V, I_O = 0, V_I (A-port or control input) = V_{CC} or GND, V_I (B port) = V_{TT} or GND	Outputs high			80	mA
			Outputs low			80	
			Outputs disabled			80	
ΔI_{CC}☆		V_{CC} = 3.45 V, One A-port or control input at V_{CC} – 0.6 V, Other A-port or control inputs at V_{CC} or GND				1	mA
C_i	Control inputs	V_I = 3.15 V or 0					pF
C_{io}	A port	V_O = 3.15 V or 0					pF
	B port	V_O = 1.5 V or 0					

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ For I/O ports, the parameter I_I includes the off-state output leakage current.
§ The bus-hold circuit can sink at least the minimum low sustaining current at V_{IL}max. I_{BHL} should be measured after lowering V_{IN} to GND and then raising it to V_{IL}max.
¶ The bus-hold circuit can source at least the minimum high sustaining current at V_{IH}min. I_{BHH} should be measured after raising V_{IN} to V_{CC} and then lowering it to V_{IH}min.
# An external driver must source at least I_{BHLO} to switch this node from low to high.
‖ An external driver must sink at least I_{BHHO} to switch this node from high to low.
☆ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

live-insertion specifications for A port over recommended operating free-air temperature range

PARAMETER	TEST CONDITIONS			MIN	MAX	UNIT
I_{off}	V_{CC} = 0,	BIAS V_{CC} = 0,	V_I or V_O = 0 to 5.5 V		100	μA
I_{OZPU}	V_{CC} = 0 to 1.5 V,	V_O = 0.5 V to 3 V,	$\overline{OE}$ = 0		±100	μA
I_{OZPD}	V_{CC} = 1.5 V to 0,	V_O = 0.5 V to 3 V,	$\overline{OE}$ = 0		±100	μA

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live-insertion specifications for B port over recommended operating free-air temperature range

PARAMETER	TEST CONDITIONS			MIN	MAX	UNIT
I_{off}	V_{CC} = 0,	BIAS V_{CC} = 0,	V_I or V_O = 0 to 1.5 V		100	µA
I_{OZPU}	V_{CC} = 0 to 1.5 V,	V_O = 0.5 V to 1.5 V,	$\overline{OE}$ = 0		±100	µA
I_{OZPD}	V_{CC} = 1.5 V to 0,	V_O = 0.5 V to 1.5 V,	$\overline{OE}$ = 0		±100	µA
I_{CC} (BIAS V_{CC})	V_{CC} = 0 to 3.15 V	BIAS V_{CC} = 3.15 V to 3.45 V,	V_O (B port) = 0 to 1.5 V		5	mA
	V_{CC} = 3.15 V to 3.45 V				10	µA
V_O	V_{CC} = 0,	BIAS V_{CC} = 3.3 V		0.95	1.05	V
I_O	V_{CC} = 0,	BIAS V_{CC} = 3.15 V to 3.45 V,	V_O (B port) = 0.6 V	–1		µA

timing requirements over recommended ranges of supply voltage and operating free-air temperature, V_{TT} = 1.5 V and V_{REF} = 1 V for GTL+ (normal mode) (unless otherwise noted)

			MIN	MAX	UNIT
f_{clock}	Clock frequency				MHz
t_w	Pulse duration	LEAB or LEBA high			ns
		CLKAB or CLKBA high or low			
t_{su}	Setup time	A before CLKAB↑			ns
		B before CLKBA↑			
		A before LEAB↓, CLK = don't care			
		B before LEBA↓, CLK = don't care			
		$\overline{CEAB}$ before CLKAB↑			
		$\overline{CEBA}$ before CLKBA↑			
t_h	Hold time	A after CLKAB↑			ns
		B after CLKBA↑			
		A after LEAB↓, CLK = don't care			
		B after LEBA↓, CLK = don't care			
		$\overline{CEAB}$ after CLKAB↑			
		$\overline{CEBA}$ after CLKBA↑			

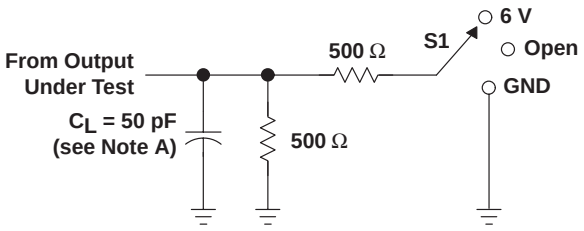
switching characteristics over recommended ranges of supply voltage and operating free-air temperature, V_{TT} = 1.5 V and V_{REF} = 1 V for GTL+ (normal mode) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	EDGE RATE†	MIN	TYP‡	MAX	UNIT
f_{max}							MHz
t_{pd}	A	B	Slow				ns
			Fast				
	LEAB	B	Slow				
			Fast				
	CLKAB	B	Slow				
			Fast				
t_{en}	$\overline{OEAB}$	B	Slow				ns
t_{dis}							
t_{en}	$\overline{OEAB}$	B	Fast				ns
t_{dis}							
t_r	Rise time, B outputs (0.6 V to 1.3 V)		Slow				ns
			Fast				
t_f	Fall time, B outputs (1.3 V to 0.6 V)		Slow				ns
			Fast				
t_{pd}	B	A					ns
	LEBA						
	CLKBA						
t_{en}	$\overline{OEBA}$	A					ns
t_{dis}							

† Slow ($\overline{ERC}$ = GND) and Fast ($\overline{ERC}$ = V_{CC})
‡ All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

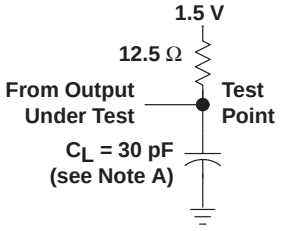
PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

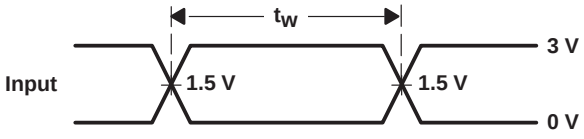


LOAD CIRCUIT FOR A OUTPUTS

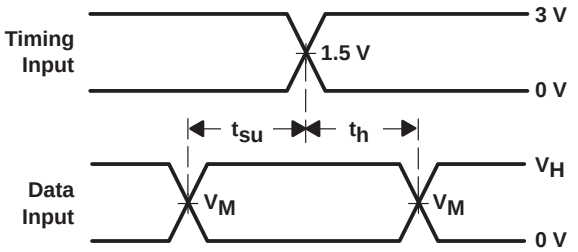
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



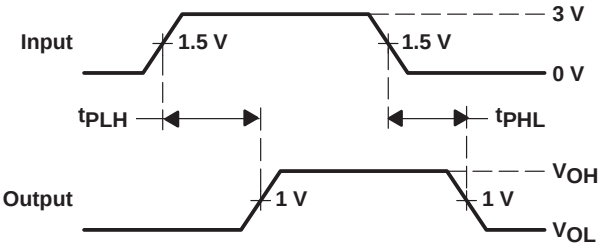
LOAD CIRCUIT FOR B OUTPUTS



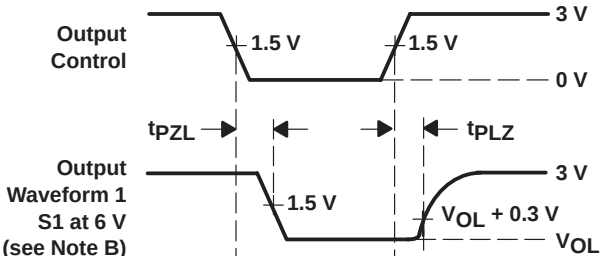
VOLTAGE WAVEFORMS
PULSE DURATION



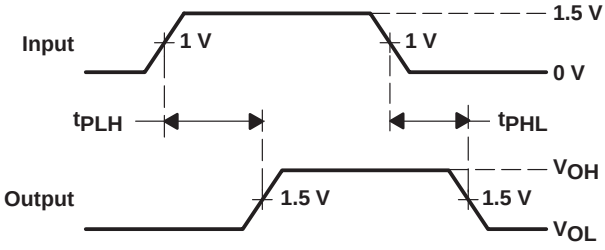
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES
(V_M = 1.5 V for A port and 1 V for B port)
(V_H = 3 V for A port and 1.5 V for B port)



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
(A port to B port)



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
(A port)



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
(B port to A port)

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, slew rate ≤ 1 V/ns.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

DISTRIBUTED-LOAD BACKPLANE SWITCHING CHARACTERISTICS

This data sheet is specified for and tested to the lump load shown in Figure 1. However, the designer probably uses this GTLP device in a distributed load like that shown in Figure 2, in which actual B-port backplane switching characteristics are different. Therefore, the device is modeled as shown in Figure 3, which very closely matches the results obtained using Figure 2. Switching characteristics based on Figure 3 more closely match actual backplane design requirements.

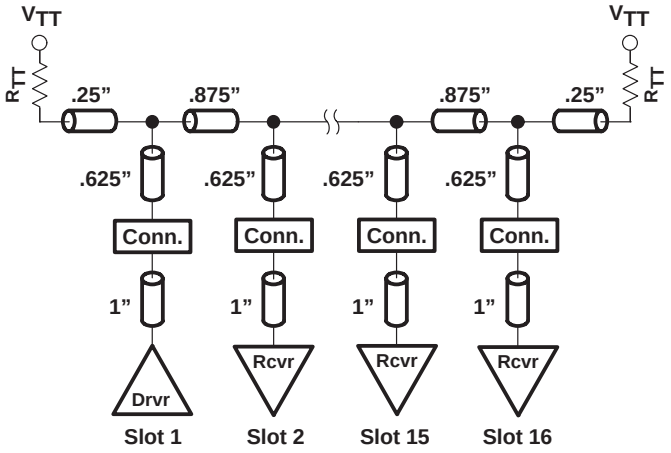


Figure 2. Test Backplane Model

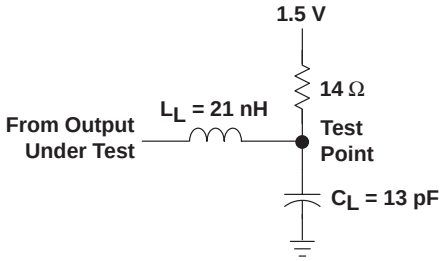


Figure 3. Distributed-Load Circuit for B Outputs

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, V_{TT} = 1.5 V and V_{REF} = 1 V for GTL+ (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	EDGE RATE†	MIN	TYP‡	MAX	UNIT
f_{max}							MHz
t_{pd}	A	B	Slow				ns
			Fast				
	LEAB	B	Slow				
			Fast				
	CLK	B	Slow				
			Fast				
t_{en}	$\overline{OEAB}$	B	Slow				ns
t_{dis}							
t_{en}	$\overline{OEAB}$	B	Fast				ns
t_{dis}							
t_r	Rise time, B outputs (0.6 V to 1.3 V)		Slow				ns
			Fast				
t_f	Fall time, B outputs (1.3 V to 0.6 V)		Slow				ns
			Fast				

† Slow ($\overline{ERC}$ = GND) and Fast ($\overline{ERC}$ = V_{CC})
‡ All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

PRODUCT PREVIEW

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