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TEXAS INSTRUMENTS

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# CD4048B Types

## CMOS Multifunction Expandable 8-Input Gate

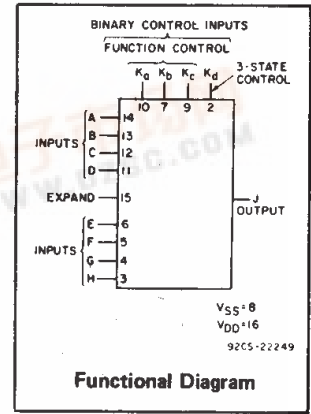
High-Voltage Types (20-Volt Rating)

CD4048B is an 8-input gate having four control inputs. Three binary control inputs — Ka, Kb, and Kc — provide the implementation of eight different logic functions. These functions are OR, NOR, AND, NAND, OR/AND, OR/NAND, AND/OR and AND/NOR.

A fourth control input, Kd, provides the user with a 3-state output. When control input Kd is high, the output is either a logic 1 or a logic 0 depending on the inner states. When control input Kd is low, the output is an open circuit. This feature enables the user to connect this device to a common bus line.

In addition to the eight input lines, an EXPAND input is provided that permits the user to increase the number of inputs into a CD4048B (see Fig. 2). For example, two CD4048B's can be cascaded to provide a 16-input multifunction gate. When the EXPAND input is not used, it should be connected to VSS.

The CD4048B-series types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), and in chip form (H suffix).



### MAXIMUM RATINGS, Absolute-Maximum Values:

#### DC SUPPLY-VOLTAGE RANGE, (VDD)

Voltages referenced to VSS Terminal ..... -0.5V to +20V

INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5V to VDD +0.5V

DC INPUT CURRENT, ANY ONE INPUT ..... ±10mA

#### POWER DISSIPATION PER PACKAGE (PD):

For TA = -55°C to +100°C ..... 500mW

For TA = +100°C to +125°C ..... Derate Linearly at 12mW/°C to 200mW

#### DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR TA = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) ..... 100mW

OPERATING-TEMPERATURE RANGE (TA) ..... -55°C to +125°C

STORAGE TEMPERATURE RANGE (Tstg) ..... -65°C to +150°C

#### LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max ..... +265°C

### Features:

- Three-state output
- Many logic functions available in one package
- Standardized, symmetrical output characteristics
- 100% tested for quiescent current at 20 V
- Maximum input current of 1 μA at 18 V (full package-temperature range), 100 nA at 18 V and 25°C
- Noise margin (full package-temperature range) = 1 V at VDD=5 V, 2 V at VDD = 10 V, 2.5 V at VDD=15 V
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13B, 'Standard Specifications for Description of 'B' Series CMOS Devices'

### Applications:

- Selection of up to 8 logic functions
- Digital control of logic
- General-purpose gating logic
  - Decoding
  - Encoding

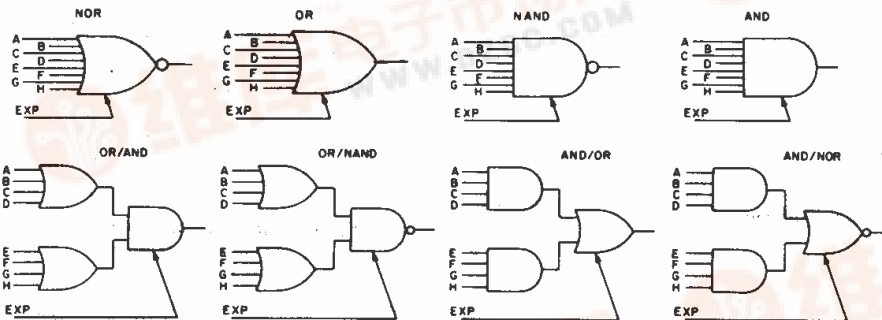
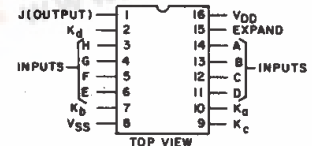


Fig. 1 - Basic logic configurations.



### TERMINAL ASSIGNMENT

### RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For TA = Full Package Temperature Range)	3	18	V

3  
COMMERCIAL CMOS  
HIGH VOLTAGE ICs



# CD4048B Types

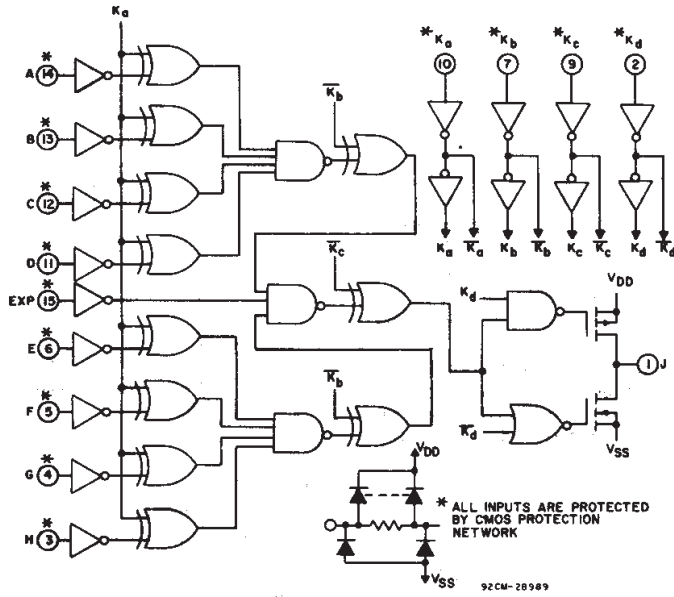


Fig. 2 - Logic diagram.

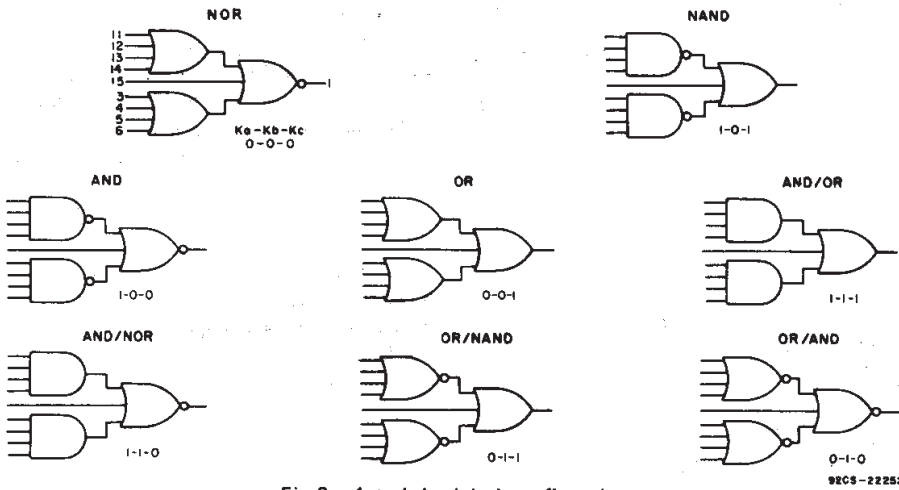


Fig. 3 - Actual-circuit logic configurations.

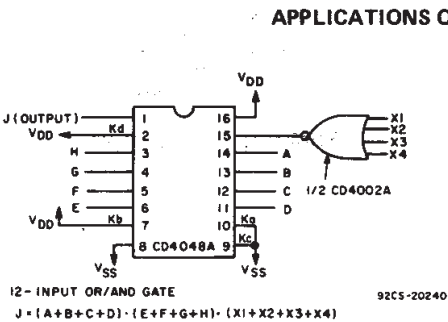


Fig. 4 - 12-input OR/AND gate.

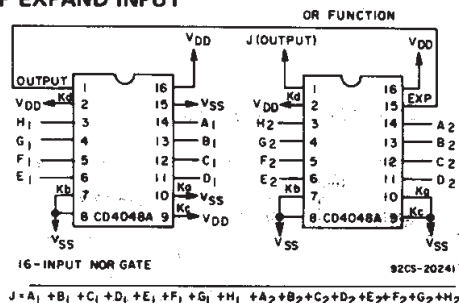


Fig. 5 - 16-input NOR gate.

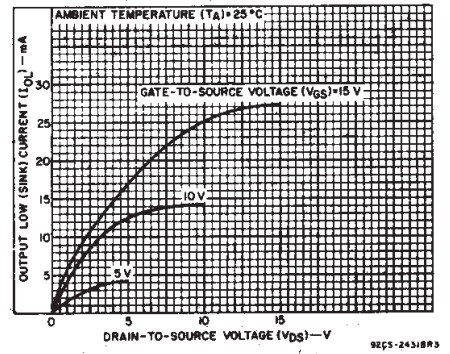


Fig. 6 - Typical output low (sink) current characteristics.

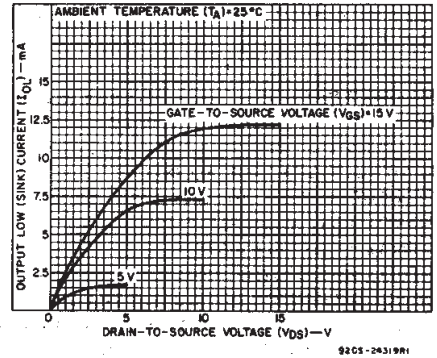


Fig. 7 - Minimum output low (sink) current characteristics.

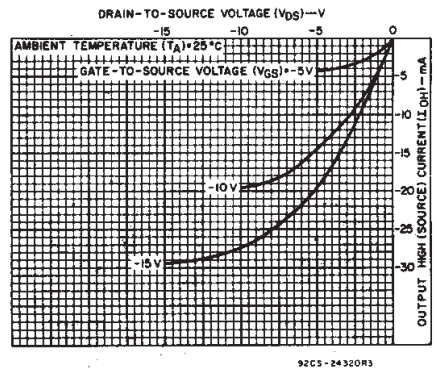


Fig. 8 - Typical output high (source) current characteristics.

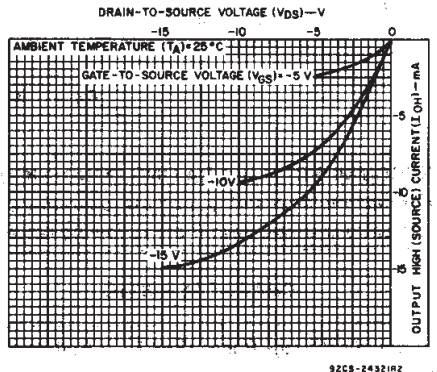


Fig. 9 - Minimum output high (source) current characteristics.

# CD4048B Types

## STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
	V <sub>O</sub> (V)	V <sub>IN</sub> (V)	V <sub>DD</sub> (V)	-55			+25				
				-55	-40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I <sub>DD</sub> Max.	—	0,5	5	0.25	0.25	7.5	7.5	—	0.01	0.25	μA
	—	0,10	10	0.5	0.5	15	15	—	0.01	0.5	
	—	0,15	15	1	1	30	30	—	0.01	1	
	—	0,20	20	5	5	150	150	—	0.02	5	
Output Low (Sink) Current I <sub>OL</sub> Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	—	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	—	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	—	
Output High (Source) Current, I <sub>OH</sub> Min.	4.6	0,5	5	-0.64	-0.61	-0.42	-0.36	-0.51	-1	—	mA
	2.5	0,5	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	—	
	9.5	0,10	10	-1.6	-1.5	-1.1	-0.9	-1.3	-2.6	—	
Output Voltage: Low-Level, V <sub>OL</sub> Max.	—	0,5	5	0.05			—	0	0.05	—	V
	—	0,10	10	0.05			—	0	0.05	—	
	—	0,15	15	0.05			—	0	0.05	—	
Output Voltage: High-Level, V <sub>OH</sub> Min.	—	0,5	5	4.95			4.95	5	—	—	V
	—	0,10	10	9.95			9.95	10	—	—	
	—	0,15	15	14.95			14.95	15	—	—	
Input Low Voltage, V <sub>IL</sub> Max.	0.5,4.5	—	5	1.5			—	—	1.5	—	V
	1.9	—	10	3			—	—	3	—	
	1.5,13.5	—	15	4			—	—	4	—	
Input High Voltage, V <sub>IH</sub> Min.	0.5,4.5	—	5	3.5			3.5	—	—	—	V
	1.9	—	10	7			7	—	—	—	
	1.5,13.5	—	15	11			11	—	—	—	
Input Current I <sub>IN</sub> Max.		0,18	18	±0.1	±0.1	±1	±1	—	±10 <sup>-5</sup>	±0.1	μA
3-State Output Current, I <sub>OUT</sub>	0,18	0,18	18	±0.4	±0.4	±12	±12	—	±10 <sup>-4</sup>	±0.4	μA

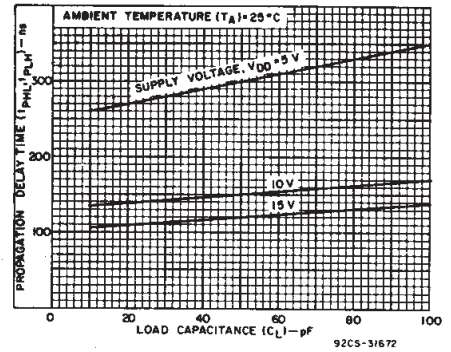


Fig. 10 — Typical propagation delay time (logic inputs to output) as a function of load capacitance.

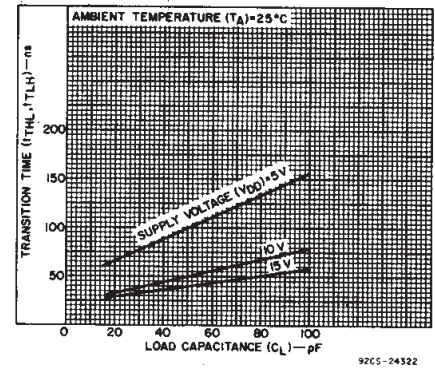


Fig. 11 — Typical transition time vs. load capacitance.

## IMPLEMENTATION OF EXPAND INPUT FOR 9 OR MORE INPUTS

OUTPUT FUNCTION	FUNCTION NEEDED AT EXPAND INPUT	OUTPUT BOOLEAN EXPRESSION
NOR	OR	$J = \overline{(A+B+C+D+E+F+G+H)} + (\text{EXP})$
OR	OR	$J = (A+B+C+D+E+F+G+H) + (\text{EXP})$
AND	NAND	$J = (ABCDEFHG) \cdot \overline{(\text{EXP})}$
NAND	NAND	$J = (ABCDEFHG) \cdot (\text{EXP})$
OR/AND	NOR	$J = (A+B+C+D) \cdot \overline{(E+F+G+H)} \cdot \overline{(\text{EXP})}$
OR/NAND	NOR	$J = (A+B+C+D) \cdot \overline{(E+F+G+H)} \cdot (\text{EXP})$
AND/NOR	AND	$J = \overline{(ABCD)} + (EFGH) + (\text{EXP})$
AND/OR	AND	$J = (ABCD) + (EFGH) + (\text{EXP})$

Note: (EXP) designates the EXPAND function (i.e.,  $X_1 + X_2 + \dots + X_N$ ).

**NOTE:**  
Refer to FUNCTION TRUTH TABLE for connection of unused inputs.

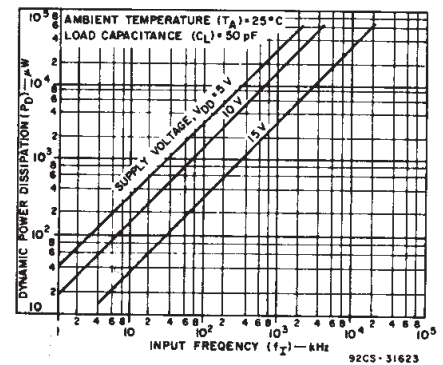


Fig. 12 — Typical power dissipation as a function of input frequency.

## CD4048B Types

**DYNAMIC CHARACTERISTICS** at  $T_A=25^\circ\text{C}$ ,  $C_L=50\text{ pF}$ , Input  $t_r, t_f=20\text{ ns}$ ,  
 $R_L=200\text{ k}\Omega$  unless otherwise specified

CHARACTERISTIC	TEST CONDITIONS	LIMITS		UNITS	
		V <sub>DD</sub> V	All Package Types		
			Typ.		Max.
Propagation Delay: $t_{PHL}, t_{PLH}$ Inputs to Output and Ka to Output		5	300	600	ns
		10	150	300	
		15	120	240	
Kb to Output		5	225	450	
		10	85	170	
		15	55	110	
Kc to Output		5	140	280	
		10	50	100	
		15	40	80	
Expand Input to Output		5	190	380	
		10	90	180	
		15	65	130	
3-State Propagation Delay: Kd to Output $t_{PHZ}, t_{PLZ}$ $t_{PZH}, t_{PZL}$	$R_L=1\text{ k}\Omega$ See Fig.21	5	80	160	
		10	35	70	
		15	25	50	
Transition Time: $t_{THL}, t_{TLH}$		5	100	200	
		10	50	100	
		15	40	80	
Input Capacitance: $C_i$	Any Input	5	7	pF	
3-State Output Capacitance		5	10		

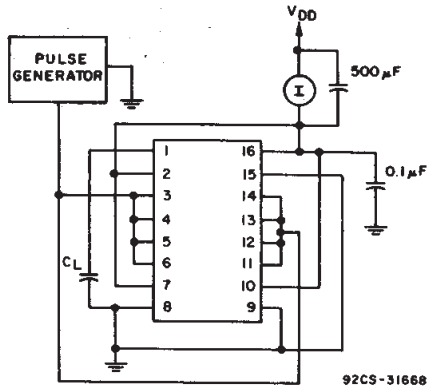


Fig. 13 – Dynamic power dissipation test circuit.

### FUNCTION TRUTH TABLE

OUTPUT FUNCTION	BOOLEAN EXPRESSION	K <sub>a</sub>	K <sub>b</sub>	K <sub>c</sub>	UNUSED INPUT*
NOR	$J = \overline{A+B+C+D+E+F+G+H}$	0	0	0	V <sub>SS</sub>
OR	$J = A+B+C+D+E+F+G+H$	0	0	1	V <sub>SS</sub>
OR/AND	$J = (A+B+C+D) \cdot (E+F+G+H)$	0	1	0	V <sub>SS</sub>
OR/NAND	$J = (A+B+C+D) \cdot \overline{(E+F+G+H)}$	0	1	1	V <sub>SS</sub>
AND	$J = ABCDEFGH$	1	0	0	V <sub>DD</sub>
NAND	$J = \overline{ABCDEFGH}$	1	0	1	V <sub>DD</sub>
AND/NOR	$J = \overline{ABCD} + \overline{EFGH}$	1	1	0	V <sub>DD</sub>
AND/OR	$J = \overline{ABCD} + EFGH$	1	1	1	V <sub>DD</sub>
K <sub>d</sub> =1 Normal Inverter Action					
K <sub>d</sub> =0 High Impedance Output					

EXPAND Input=0

\* See Figs. 1,2,3,4, and 5.

### TEST CIRCUITS - STATIC MEASUREMENTS

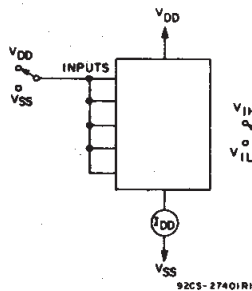


Fig. 14 – Quiescent device current test circuit.

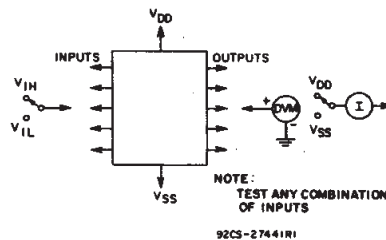


Fig. 15 – Input voltage test circuit.

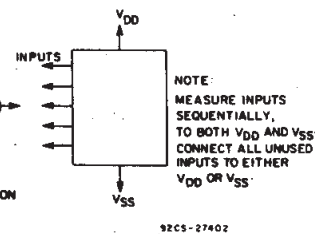


Fig. 16 – Input current test circuit.

92CS-27402

# CD4048B Types

## TEST CIRCUITS - DYNAMIC MEASUREMENTS

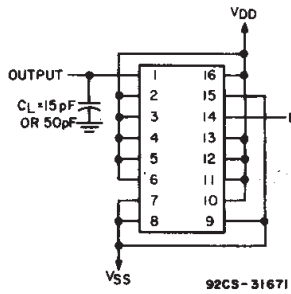


Fig. 17 - Test circuit for  $t_{PHL}$ ,  $t_{THL}$ , and  $t_{TLH}$  (AND) measurements.

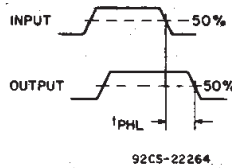


Fig. 18 - Waveforms for  $t_{PHL}$  and  $t_{PHL}$  (AND).

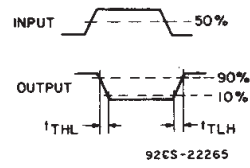


Fig. 19 - Waveforms for  $t_{THL}$  and  $t_{TLH}$  (AND).

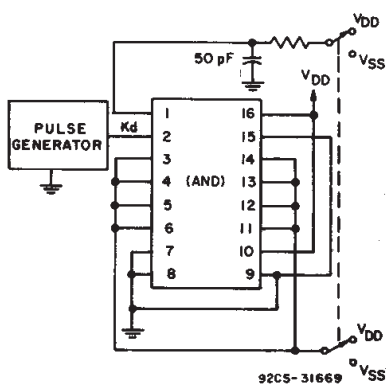


Fig. 20 - Test circuit for  $t_{PZL}$ ,  $t_{PZH}$ ,  $t_{PLZ}$ , and  $t_{PHZ}$  (AND).

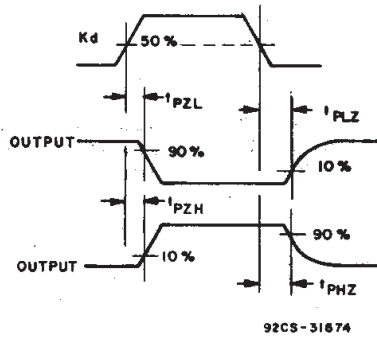
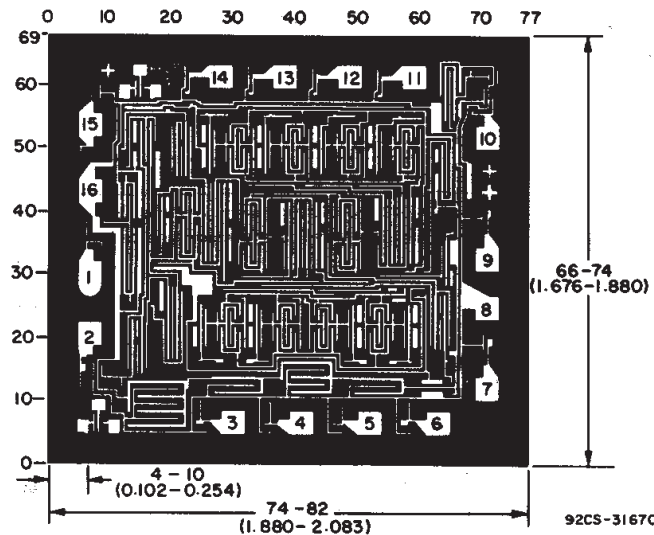


Fig. 21 - Waveforms for  $t_{PZL}$ ,  $t_{PZH}$ ,  $t_{PLZ}$ , and  $t_{PHZ}$  (AND).



Dimensions and pad layout for CD4048BH.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils ( $10^{-3}$  inch).

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