



Data sheet acquired from Harris Semiconductor
SCHS070

CMOS Dual 4-Bit Latch

High-Voltage Types (20-Volt Rating)

■ CD4508B dual 4-bit latch contains two identical 4-bit latches with separate STROBE, RESET, and OUTPUT DISABLE controls. With the STROBE line in the high state, the data on the "D" inputs appear at the corresponding "Q" outputs provided the DISABLE line is in the low state. Changing the STROBE line to the low state locks the data into the latch. A high on the reset line forces the outputs to a low level regardless of the state of the STROBE input. The outputs are forced to the high-impedance state for bus line applications by a high level on the DISABLE input.

The CD4508B types are supplied in the 24-lead dual-in-line ceramic packages (D and F suffixes), 24-lead dual-in-line plastic packages (E suffix), and in chip form (H suffix).

The CD4508B is similar to industry type MC14508.

Features:

- Two independent 4-bit latches
- Individual master reset for each 4-bit latch
- 3-state outputs with high-impedance state for bus line applications
- Medium-speed operation: $t_{PHL} = t_{PLH} = 70 \text{ ns}$ (typ.) at $V_{DD} = 10 \text{ V}$ and $C_L = 50 \text{ pF}$
- 100% tested for quiescent current at 20 V
- 5-V, 10-V, and 15-V parametric ratings
- Standardized, symmetrical output characteristics
- Maximum input current of $1 \mu\text{A}$ at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (full package-temperature range) =
 - 1 V at $V_{DD} = 5 \text{ V}$
 - 2 V at $V_{DD} = 10 \text{ V}$
 - 2.5 V at $V_{DD} = 15 \text{ V}$
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications:

- Buffer storage
- Holding registers
- Data storage and multiplexing

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V_{DD})	-0.5V to +20V
Voltages referenced to V_{SS} Terminal	
INPUT VOLTAGE RANGE, ALL INPUTS	-0.5V to $V_{DD} + 0.5\text{V}$
DC INPUT CURRENT, ANY ONE INPUT	$\pm 10\text{mA}$
POWER DISSIPATION PER PACKAGE (P_D):	
For $T_A = -55^\circ\text{C}$ to $+100^\circ\text{C}$	500mW
For $T_A = +100^\circ\text{C}$ to $+125^\circ\text{C}$	Derate Linearly at $12\text{mW}/^\circ\text{C}$ to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
FOR $T_A = \text{FULL PACKAGE-TEMPERATURE RANGE (All Package Types)}$	100mW
OPERATING-TEMPERATURE RANGE (T_A)	-55°C to $+125^\circ\text{C}$
STORAGE TEMPERATURE RANGE (T_{stg})	-65°C to $+150^\circ\text{C}$
LEAD TEMPERATURE (DURING SOLDERING):	
At distance $1/16 \pm 1/32$ inch ($1.59 \pm 0.79\text{mm}$) from case for 10s max	$+265^\circ\text{C}$

RECOMMENDED OPERATING CONDITIONS at $T_A = 25^\circ\text{C}$, Except as Noted. For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS		UNITS
		Min.	Max.	
Supply-Voltage Range (For $T_A = \text{Full Package-Temperature Range}$)		3	18	V
Reset Pulse Width, $t_W(R)$	5	200	—	ns
	10	140	—	
	15	100	—	
Strobe Pulse Width, $t_W(st)$	5	140	—	ns
	10	80	—	
	15	70	—	
Setup Time, t_{SU}	5	50	—	ns
	10	30	—	
	15	20	—	
	5	0	—	
	10	0	—	
	15	0	—	

CD4508B Types

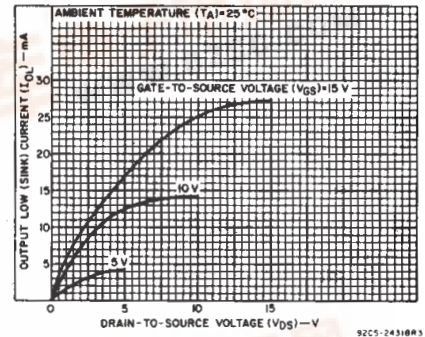
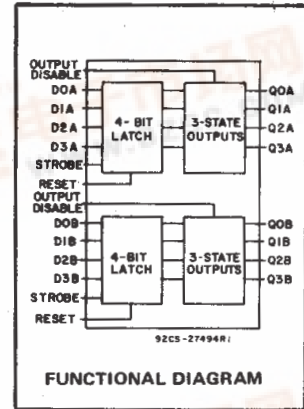


Fig.2 - Typical output low (sink) current characteristics.

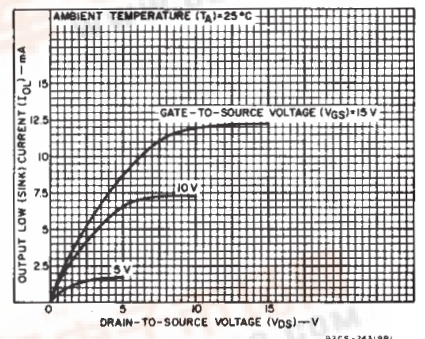


Fig.3 - Minimum output low (sink) current characteristics.

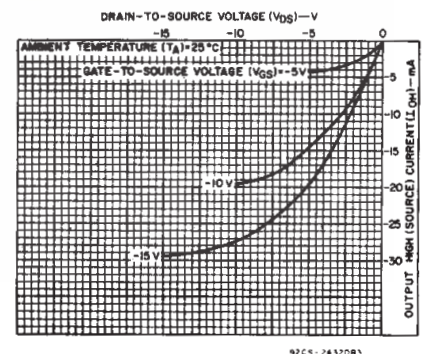


Fig.4 - Typical output high (source) current characteristics.

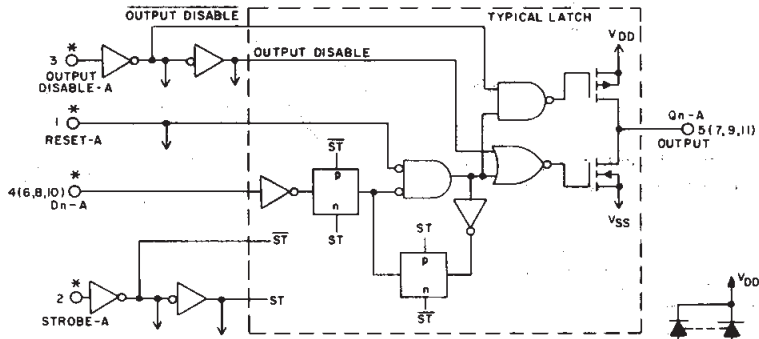
3
COMMERCIAL CMOS
HIGH VOLTAGE ICs



CD4508B Types

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
	V _O (V)	V _{IN} (V)	V _{DD} (V)					+25			
				-55	-40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I _{DD} Max.	-	0,5	5	5	5	150	150	-	0,04	5	μA
	-	0,10	10	10	10	300	300	-	0,04	10	
	-	0,15	15	20	20	600	600	-	0,04	20	
	-	0,20	20	100	100	3000	3000	-	0,08	100	
Output Low (Sink) Current I _{OL} Min.	0,4	0,5	5	0,64	0,61	0,42	0,36	0,51	1	-	mA
	0,5	0,10	10	1,6	1,5	1,1	0,9	1,3	2,6	-	
	1,5	0,15	15	4,2	4	2,8	2,4	3,4	6,8	-	
Output High (Source) Current, I _{OH} Min.	4,6	0,5	5	-0,64	-0,61	-0,42	-0,36	-0,51	-1	-	mA
	2,5	0,5	5	-2	-1,8	-1,3	-1,15	-1,6	-3,2	-	
	9,5	0,10	10	-1,6	-1,5	-1,1	-0,9	-1,3	-2,6	-	
	13,5	0,15	15	-4,2	-4	-2,8	-2,4	-3,4	-6,8	-	
Output Voltage: Low-Level, V _{OL} Max.	-	0,5	5	0,05				-	0	0,05	V
	-	0,10	10	0,05				-	0	0,05	
	-	0,15	15	0,05				-	0	0,05	
Output Voltage: High-Level, V _{OH} Min.	-	0,5	5	4,95				4,95	5	-	V
	-	0,10	10	9,95				9,95	10	-	
	-	0,15	15	14,95				14,95	15	-	
Input Low Voltage, V _{IL} Max.	0,5, 4,5	-	5	1,5				-	-	1,5	V
	1,9	-	10	3				-	-	3	
	1,5, 13,5	-	15	4				-	-	4	
Input High Voltage, V _{IH} Min.	0,5, 4,5	-	5	3,5				3,5	-	-	V
	1,9	-	10	7				7	-	-	
	1,5, 13,5	-	15	11				11	-	-	
Input Current I _{IN} Max.	-	0,18	18	±0,1	±0,1	±1	±1	-	±10 ⁻⁵	±0,1	μA
3-State Output Leakage Current I _{OUT} Max.	0,18	0,18	18	±0,4	±0,4	±12	±12	-	±10 ⁻⁴	±0,4	μA



RESET	DISABLE	STROBE	D INPUT	Q OUTPUT
0	0	1	1	1
0	0	1	0	0
0	0	0	X	LATCHED
1	0	X	X	0
X	1	X	X	Z

1 = HIGH LEVEL X = DON'T CARE
0 = LOW LEVEL Z = HIGH IMPEDANCE

Fig. 7 - Logic diagram (A-Section), 1 of 4 identical latches with common output disable, reset, and strobe.

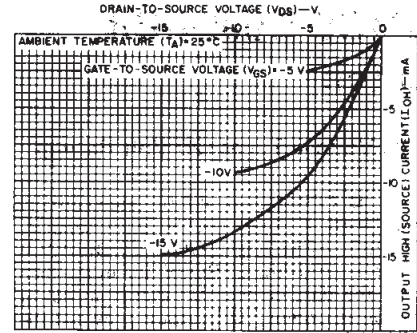


Fig. 4 - Minimum output high (source) current characteristics.

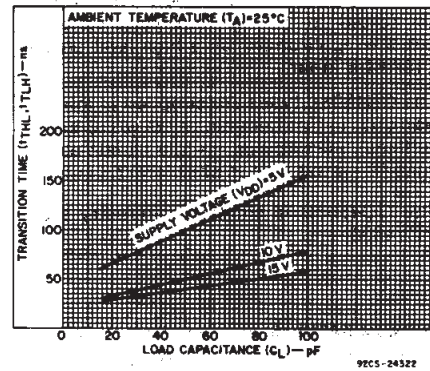


Fig. 5 - Typical transition time as a function of load capacitance.

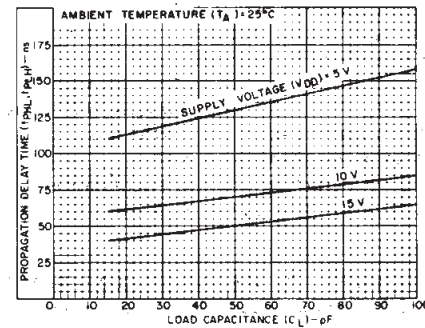


Fig. 6 - Typical propagation delay time as a function of load capacitance (strobe to data out).

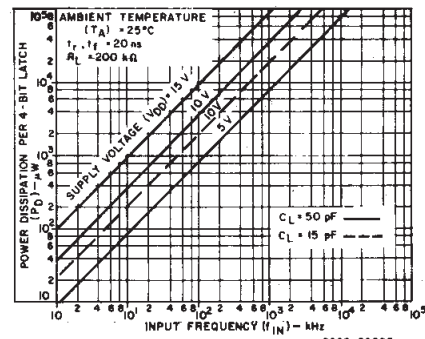


Fig. 8 - Typical power dissipation as a function of frequency.

CD4508B Types

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25^\circ\text{C}$; Input $t_r, t_f = 20 \text{ ns}$, $C_L = 50 \text{ pF}$, $R_L = 200 \text{ k}\Omega$, unless otherwise specified.

CHARACTERISTIC	TEST CONDITIONS	LIMITS			UNITS
		VDD	Typ.	Max.	
Transition Time, t_{THL}, t_{TLH}		5	100	200	
		10	50	100	
		15	40	80	
Minimum Reset Pulse Width, $t_{W(R)}$		5	100	200	
		10	70	140	
		15	50	100	
Minimum Strobe Pulse Width, $t_{W(st)}$		5	70	140	
		10	40	80	
		15	35	70	
Minimum Setup Time, t_{SU}		5	25	50	
		10	15	30	
		15	10	20	
Minimum Hold Time, t_H		5	0	0	
		10	0	0	
		15	0	0	
Propagation Delay Times: t_{PHL}, t_{PLH} Strobe to Data Out		5	130	260	ns
		10	70	140	
		15	50	100	
Data In to Data Out		5	105	210	
		10	60	120	
		15	45	90	
Reset to Data Out		5	90	180	
		10	50	100	
		15	40	80	
3-State Propagation Delay Times: Output High to High Impedance, t_{PHZ}		5	90	180	
		10	50	100	
		15	35	70	
High Impedance to Output High, t_{PZH}		5	90	180	
		10	50	100	
		15	35	70	
Output Low to High Impedance, t_{PLZ}		5	90	180	
		10	50	100	
		15	35	70	
High Impedance to Output Low, t_{PZL}		5	90	180	
		10	50	100	
		15	35	70	
Input Capacitance, C_{IN}	Any Input	—	5	7.5	pF

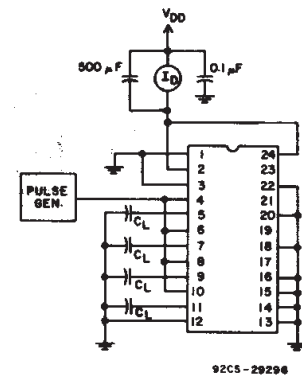


Fig. 9 — Power dissipation test circuit.

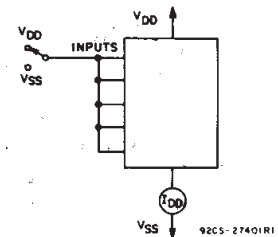


Fig. 10 — Quiescent device current test circuit.

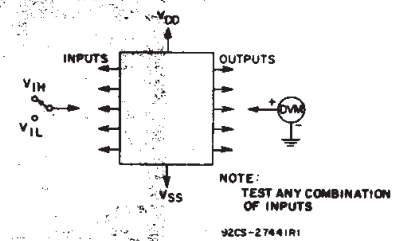


Fig. 11 — Input voltage test circuit.

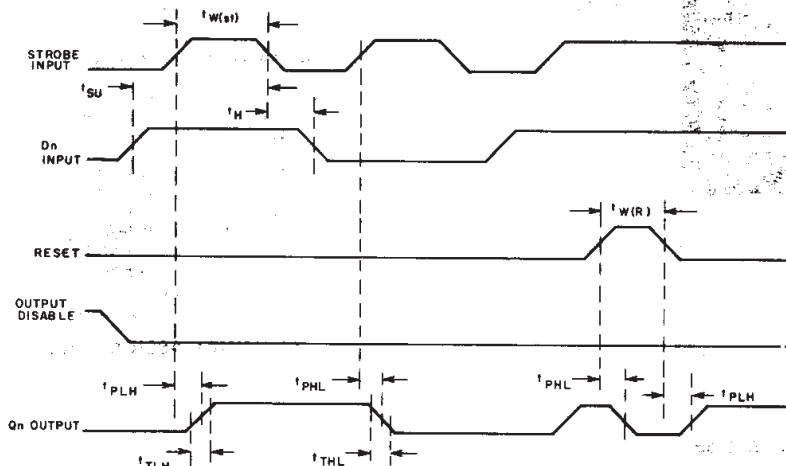


Fig. 12 — Test waveforms.

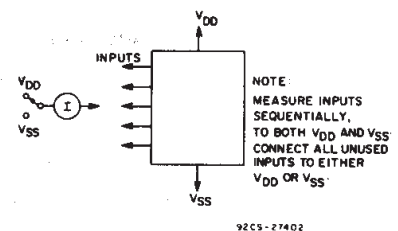
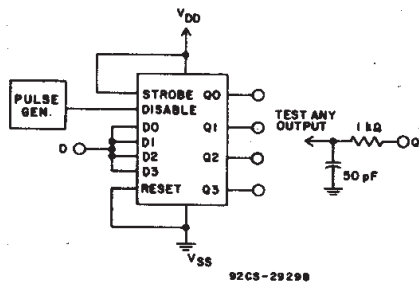
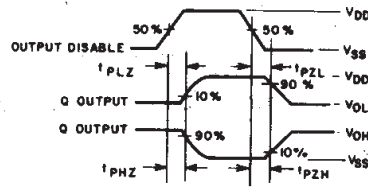


Fig. 13 — Input current test circuit.

CD4508B Types



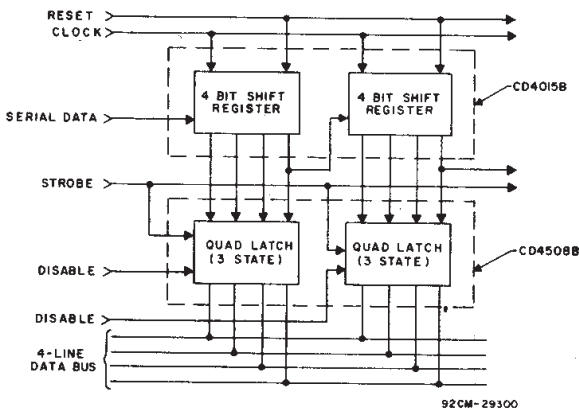
92CS-29298



CHAR.	TEST VOLT.	AT D	AT Q
t_{PHZ}	V_{DD}	V_{SS}	
t_{PLZ}	V_{SS}	V_{DD}	
t_{PZL}	V_{SS}	V_{DD}	
t_{PZH}	V_{DD}	V_{SS}	

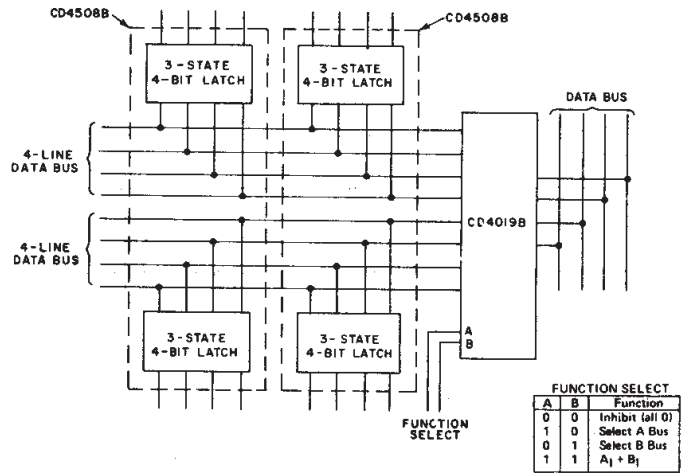
92CS-29299

Fig. 14 - Output disable test circuit and waveforms.



92CM-29300

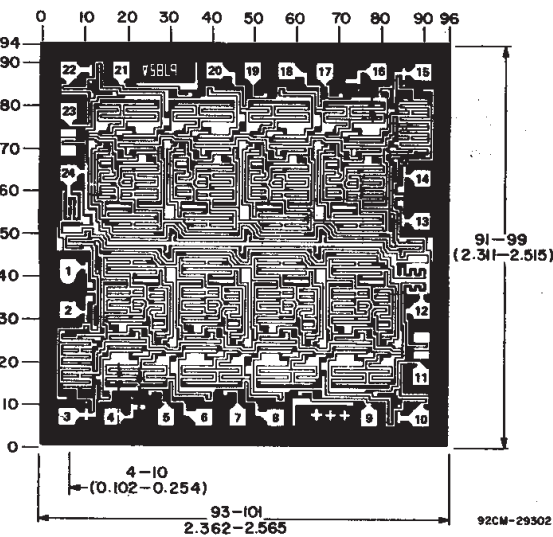
Fig. 15 - Bus register.



FUNCTION SELECT		
A	B	Function
0	0	Inhibit (all 0)
1	0	Select A Bus
0	1	Select B Bus
1	1	$A_1 + B_1$

92CM-29301

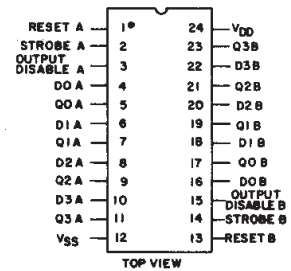
Fig. 16 - Dual multiplexed bus register with function select.



92CM-29302

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

Chip dimensions and pad layout for CD4508B.



92CS-27804

TOP VIEW

TERMINAL ASSIGNMENT

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