



Data sheet acquired from Harris Semiconductor
SCHS199

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CD74HC4016

High-Speed CMOS Logic Quad Bilateral Switch

Features

- Wide Analog-Input-Voltage Range 0V to 10V
- Low "ON" Resistance
 - 45Ω (Typ) $V_{CC} = 4.5V$
 - 35Ω (Typ) $V_{CC} = 6V$
 - 30Ω (Typ) $1fcV_{CC} = 9V$
- Fast Switching and Propagation Delay Times
- Low "OFF" Leakage Current
- Built-In "Break-Before-Make" Switching
- Suitable for Sample and Hold Applications
- Wide Operating Temperature Range . . . -55°C to 125°C
- HC Types
 - 2V to 10V Operation
 - High Noise Immunity: $N_{IL} = 30\%$, $N_{IH} = 30\%$ of V_{CC} at $V_{CC} = 5V$

Description

The Harris CD74HC4016 contains four independent digitally controlled analog switches that use silicon-gate CMOS technology to achieve operating speeds similar to LSTTL with the low power consumption of standard CMOS integrated circuits.

Each switch has two input/output terminals (nY, nZ) and an active high enable input (nE). Current through the switch will not cause additional V_{CC} current provided the analog voltage is maintained between V_{CC} and GND.

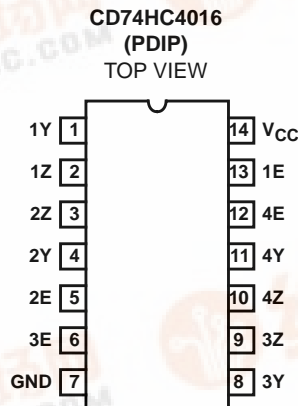
Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74HC4016E	-55 to 125	14 Ld PDIP	E14.3
CD74HC4016E	-55 to 125	14 Ld SOIC	M14.15

NOTES:

1. When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.
2. Wafer and die for this part number is available which meets all electrical specifications. Please contact your local sales office or Harris customer service for ordering information.

Pinout



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Absolute Maximum Ratings

DC Supply Voltage, V_{CC}	-0.5V to 7V
DC Input Diode Current, I_{IK}	
For $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$	$\pm 20mA$
DC Drain Current, per Output, I_O	
For $-0.5V < V_O < V_{CC} + 0.5V$	$\pm 25mA$
DC Output Diode Current, I_{OK}	
For $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$	$\pm 20mA$
DC Output Source or Sink Current per Output Pin, I_O	
For $V_O > -0.5V$ or $V_O < V_{CC} + 0.5V$	$\pm 25mA$
DC V_{CC} or Ground Current, I_{CC}	$\pm 50mA$

Thermal Information

Thermal Resistance (Typical, Note 3)	θ_{JA} ($^{\circ}C/W$)
PDIP Package	90
Maximum Junction Temperature (Plastic Package)	$150^{\circ}C$
Maximum Storage Temperature Range	$-65^{\circ}C$ to $150^{\circ}C$
Maximum Lead Temperature (Soldering 10s)	$300^{\circ}C$

Operating Conditions

Temperature Range, T_A	$-55^{\circ}C$ to $125^{\circ}C$
Supply Voltage Range, V_{CC}	
HC Types2V to 10V
DC Input or Output Voltage, V_I, V_O	0V to V_{CC}
Input Rise and Fall Time	
2V	1000ns (Max)
4.5V	500ns (Max)
6V	400ns (Max)
9V	250ns (Max)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

- θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

DC Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS			25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
		V_I (V)	V_{IS} (V)	V_{CC} (V)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES												
High Level Input Voltage	V_{IH}	-	-	2	1.5	-	-	1.5	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	3.15	-	V
				6	4.2	-	-	4.2	-	4.2	-	V
Low Level Input Voltage	V_{IL}	-	-	2	-	-	0.5	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	-	1.35	V
				6	-	-	1.8	-	1.8	-	1.8	V
"ON" Resistance $I_O = 1mA$	R_{ON}	V_{IH} or V_{IL}	V_{CC} or GND	4.5	-	45	180	-	225	-	270	Ω
				6	-	35	160	-	200	-	240	Ω
				9	-	30	135	-	170	-	205	Ω
				4.5	-	85	320	-	400	-	480	Ω
				6	-	55	240	-	300	-	360	Ω
				9	-	35	170	-	215	-	255	Ω
Maximum "ON" Resistance Between Any Two Switches	ΔR_{ON}	V_{IL} or V_{IH}	V_{CC} or GND	4.5	-	10	-	-	-	-	Ω	
				6	-	8.5	-	-	-	-	Ω	
Switch Off Leakage Current	I_{IZ}	$E_n =$ GND	V_{CC} or GND	6	-	-	± 0.1	-	± 1	-	± 1	μA
				10	-	-	± 0.1	-	± 1	-	± 1	μA
Logic Input Leakage Current	I_I	V_{CC} or GND	-	6	-	-	± 0.1	-	± 1	-	± 1	μA

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DC Electrical Specifications (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS			25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
		V _I (V)	V _{IS} (V)	V _{CC} (V)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	
Quiescent Device Current I _O = 0mA	I _{CC}	V _{CC} or GND	V _{CC} or GND	6	-	-	2	-	20	-	40	μA
				10	-	-	16	-	160	-	320	μA

NOTE: For dual-supply systems theoretical worst case (V_I = 2.4V, V_{CC} = 5.5V) specification is 1.8mA.

Switching Specifications Input t_r, t_f = 6ns

PARAMETER	SYMBOL	TEST CONDITIONS	V _{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS	
				MIN	TYP	MAX	MIN	MAX	MIN	MAX		
HC TYPES												
Propagation Delay, Switch In to Switch Out	t _{PLH} , t _{PHL}	C _L = 50pF	2	-	-	60	-	75	-	90	ns	
			4.5	-	-	12	-	15	-	18	ns	
		C _L = 15pF	5	-	4	-	-	-	-	-	ns	
		C _L = 50pF	6	-	-	10	-	13	-	15	ns	
			9	-	-	8	-	10	-	12	ns	
Propagation Delay, Switch Turn-On En to Out	t _{PZH} , t _{PZL}	C _L = 50pF	2	-	-	190	-	240	-	285	ns	
			4.5	-	-	38	-	48	-	57	ns	
		C _L = 15pF	5	-	16	-	-	-	-	-	ns	
		C _L = 50pF	6	-	-	32	-	41	-	48	ns	
			9	-	-	28	-	35	-	42	ns	
Propagation Delay, Switch Turn-Off En to Out	t _{PHZ} , t _{PLZ}	C _L = 50pF	2	-	-	145	-	180	-	220	ns	
			4.5	-	-	29	-	36	-	44	ns	
		C _L = 15pF	5	-	12	-	-	-	-	-	ns	
		C _L = 50pF	6	-	-	25	-	31	-	38	ns	
			9	-	-	22	-	28	-	33	ns	
Input Capacitance	C _I	-	-	-	-	10	-	10	-	10	pF	
Power Dissipation Capacitance (Notes 4, 5)	C _{PD}	-	5	-	12	-	-	-	-	-	pF	

NOTES:

- C_{PD} is used to determine the dynamic power consumption, per package.
- $P_D = C_{PD} V_{CC}^2 f_i + \sum (C_L + C_S) V_{CC}^2 f_o$ where f_i = input frequency, f_o = output frequency, C_L = output load capacitance, C_S = switch capacitance, V_{CC} = supply voltage.

Analog Channel Specifications T_A = 25°C

PARAMETER	TEST CONDITIONS	V _{CC} (V)	CD74HC4016	UNITS
Switch Frequency Response Bandwidth at -3dB Figure 3	Figure 6, Notes 6, 7	4.5	>200	MHz
Crosstalk Between Any Two Switches, Figure 4	Figure 5, Notes 7, 8	4.5	TBE	dB
Total Harmonic Distortion	1kHz, V _{IS} = 4V _{P-P} Figure 7	4, 5	0.078	%
	1kHz, V _{IS} = 8V _{P-P} Figure 7	9	0.018	%

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Analog Channel Specifications $T_A = 25^\circ\text{C}$ (Continued)

PARAMETER	TEST CONDITIONS	V_{CC} (V)	CD74HC4016	UNITS
Control to Switch Feedthrough Noise	Figure 8	4.5	TBE	mV
		9	TBE	mV
Switch "OFF" Signal Feedthrough, Figure 4	Figure 9, Notes 7, 8	4.5	-62	dB
Switch Input Capacitance, C_S		-	5	pF

NOTES:

6. Adjust input level for 0dBm at output, $f = 1\text{MHz}$.
7. V_{IS} is centered at $V_{CC}/2$.
8. Adjust input for 0dBm at V_{IS} .

Typical Performance Curves

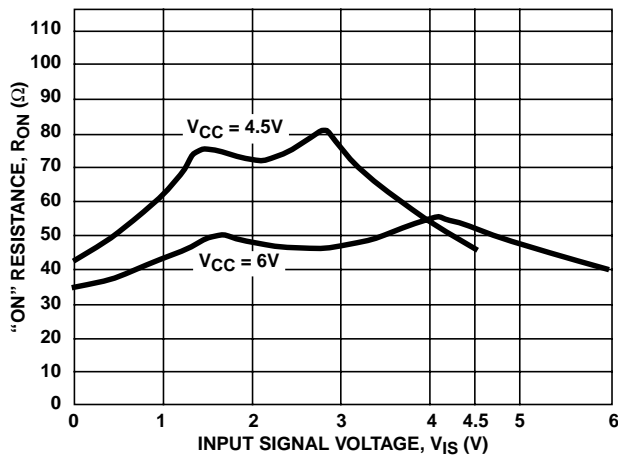


FIGURE 1. TYPICAL "ON" RESISTANCE vs INPUT SIGNAL VOLTAGE

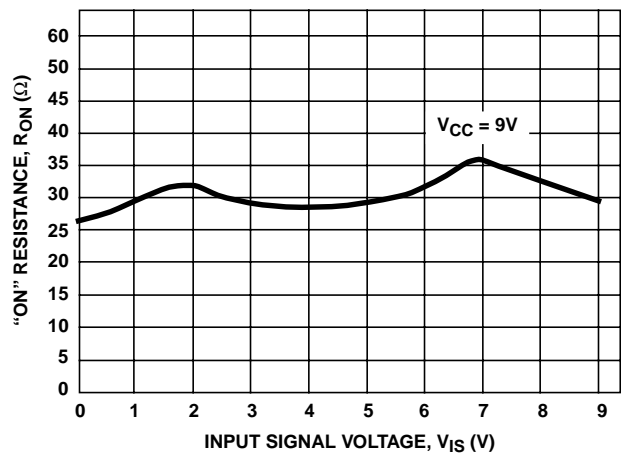


FIGURE 2. TYPICAL "ON" RESISTANCE vs INPUT SIGNAL VOLTAGE

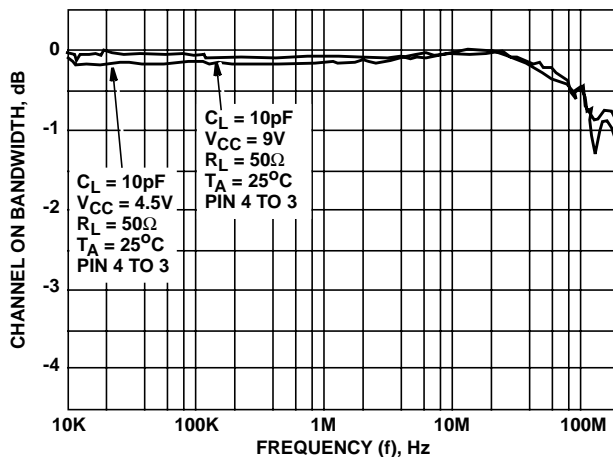


FIGURE 3. SWITCH FREQUENCY RESPONSE

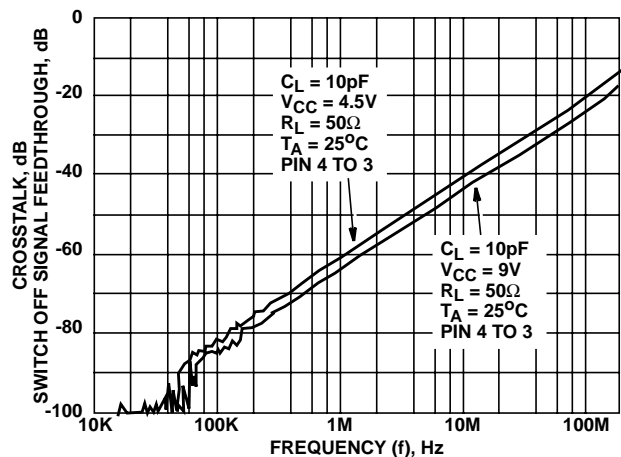


FIGURE 4. SWITCH-OFF SIGNAL FEEDTHROUGH AND CROSSTALK vs FREQUENCY

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Analog Test Circuits

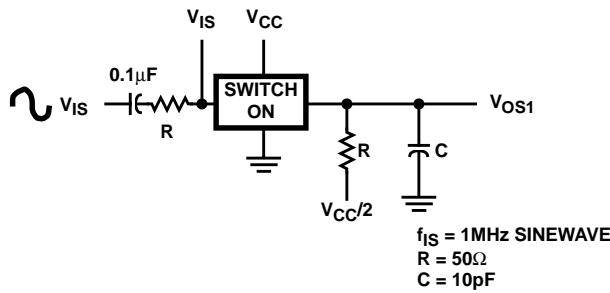


FIGURE 5. CROSTALK BETWEEN TWO SWITCHES TEST CIRCUIT

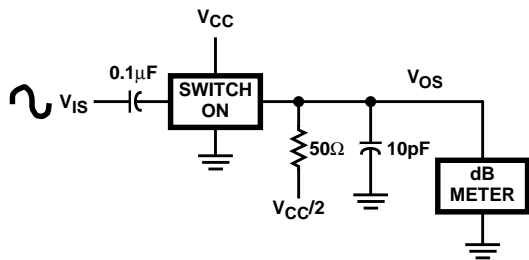
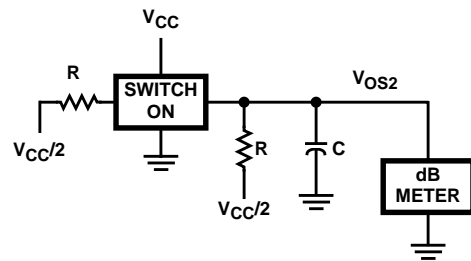


FIGURE 6. FREQUENCY RESPONSE TEST CIRCUIT

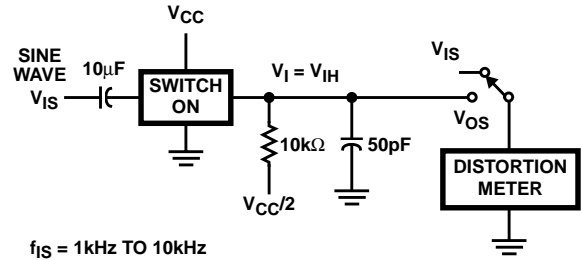


FIGURE 7. TOTAL HARMONIC DISTORTION TEST CIRCUIT

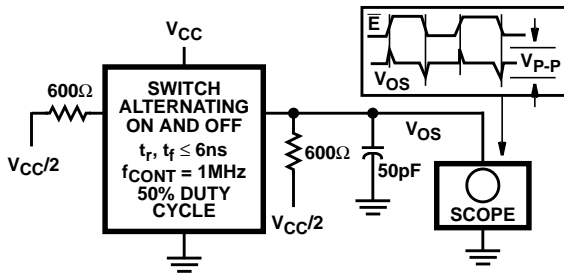


FIGURE 8. CONTROL-TO-SWITCH FEEDTHROUGH NOISE TEST CIRCUIT

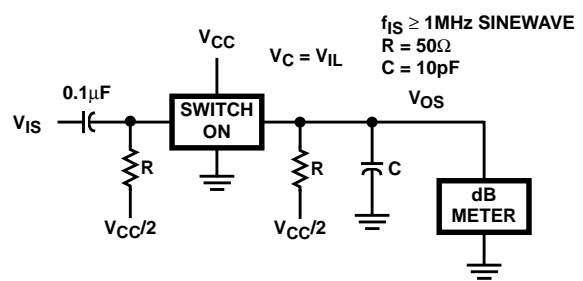


FIGURE 9. SWITCH OFF SIGNAL FEEDTHROUGH

Test Circuits and Waveforms

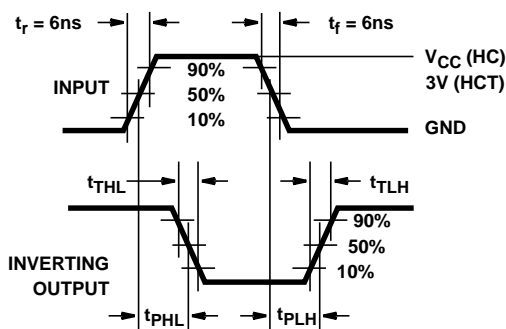


FIGURE 10. HC/HCT TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

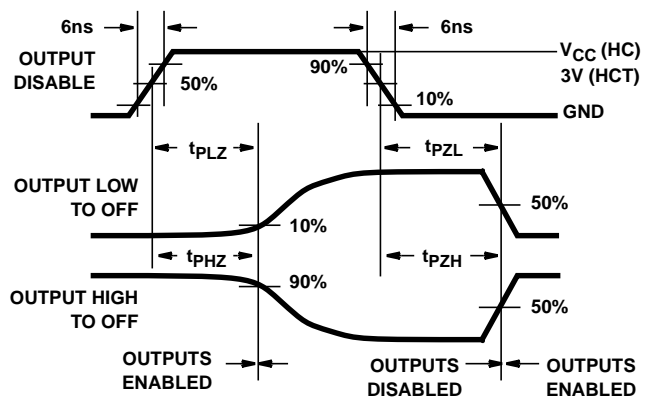


FIGURE 11. SWITCH TURN-ON AND TURN OFF PROPAGATION DELAY TIMES

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