CD54/74HC4351, CD74HCT4351, CD74HC4352

TEXAS INSTRUMENTS

Data sheet acquired from Harris Semiconductor
SCHS213A

September 1998 - Revised May 2000

High Speed CMOS Logic Analog Multiplexers/Demultiplexers with Latch

Features

- **Wide Analog Input Voltage Range . . . . . ±5V (Max)**
- **Low "On" Resistance**
  - **V_{CC} - V_{EE} = 4.5V . . . . . 70Ω (Typ)**
  - **V_{CC} - V_{EE} = 9V . . . . . 40Ω (Typ)**
- **Low Crosstalk Between Switches**
- **Fast Switching and Propagation Speeds**
- **"Break-Before-Make" Switching**
- **Wide Operating Temperature Range . . . -55°C to 125°C**
- **HC Types**
  - **2V to 6V Operation, Control; 0V to 10V Switch**
  - **High Noise Immunity: N_{IL} = 30%, N_{IH} = 30% of V_{CC} at V_{CC} = 5V**
- **HCT Types**
  - **4.5V to 5.5V Operation, Control; 0V to 10V Switch**
  - **Direct LSTTL Input Logic Compatibility, V_{IL}= 0.8V (Max), V_{IH} = 2V (Min)**
  - **CMOS Input Compatibility, $I_I \leq 1\mu A$ at V_{OL}, V_{OH}**

Description

The 'HC4351, CD74HCT4351, and CD74HC4352 are digitally controlled analog switches which utilize silicon-gate CMOS technology to achieve operating speeds similar to LSTTL with the low power consumption of standard CMOS integrated circuits.

These analog multiplexers/demultiplexers are, in essence, the HC/HCT4015 and HC4052 preceded by address latches that are controlled by an active low Latch Enable input ($\overline{LE}$). Two Enable inputs, one active low ($\overline{E1}$), and the other active high (E2) are provided allowing enabling with either input voltage level.

Ordering Information

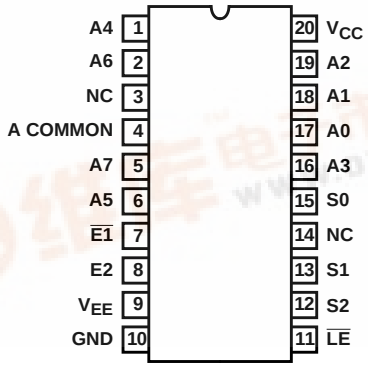
PART NUMBER	TEMP. RANGE (°C)	PACKAGE
CD54HC4351F3A	-55 to 125	20 Ld CERDIP
CD74HC4351E	-55 to 125	20 Ld PDIP
CD74HC4351M	-55 to 125	20 Ld SOIC
CD74HCT4351E	-55 to 125	20 Ld PDIP
CD74HC4352E	-55 to 125	20 Ld PDIP

NOTES:

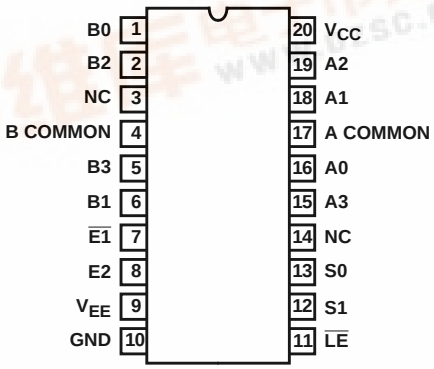
1. When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.
2. Wafer and die for this part number is available which meets all electrical specifications. Please contact your local TI sales office or customer service for ordering information.

Pinouts

CD54HC4351
(CERDIP)
CD74HC4351, CD74HCT4351
(PDIP, SOIC)
TOP VIEW

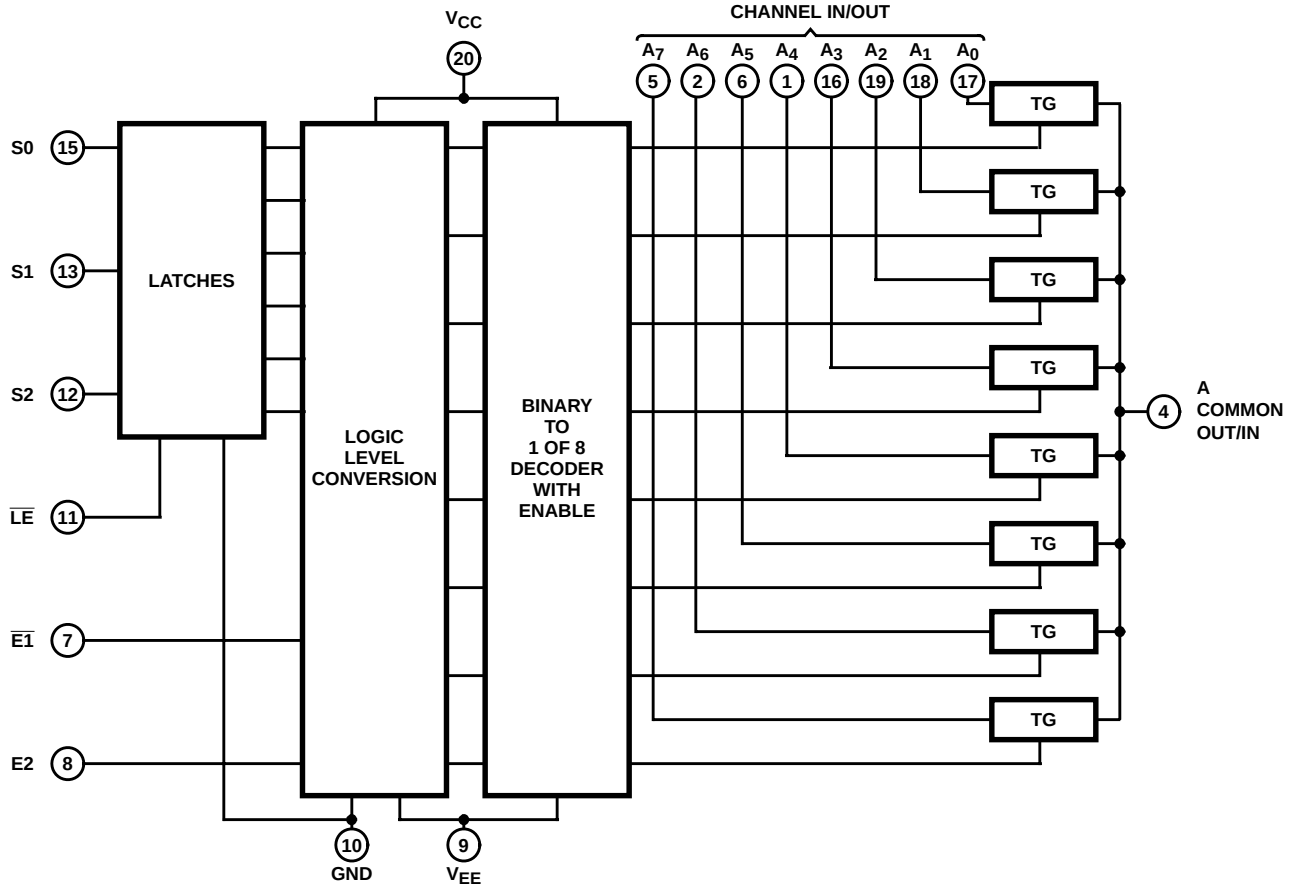


CD74HC4352
(PDIP)
TOP VIEW



Functional Diagram

'HC4351, CD74HCT4351



TRUTH TABLE
'HC4351, CD74HCT4351

INPUT STATES					(NOTE 3) "ON" SWITCHES
$\overline{E1}$	E2	S2	S1	S0	$\overline{LE}$ = H
L	H	L	L	L	A_0
L	H	L	L	H	A_1
L	H	L	H	L	A_2
L	H	L	H	H	A_3
L	H	H	L	L	A_4
L	H	H	L	H	A_5
L	H	H	H	L	A_6
L	H	H	H	H	A_7
H	L	X	X	X	None

NOTE:

3. When $\overline{LE}$ is low S0-S2 data are latched and switches cannot change state.
   H = High Voltage Level, L = Low Voltage Level, X = Don't Care

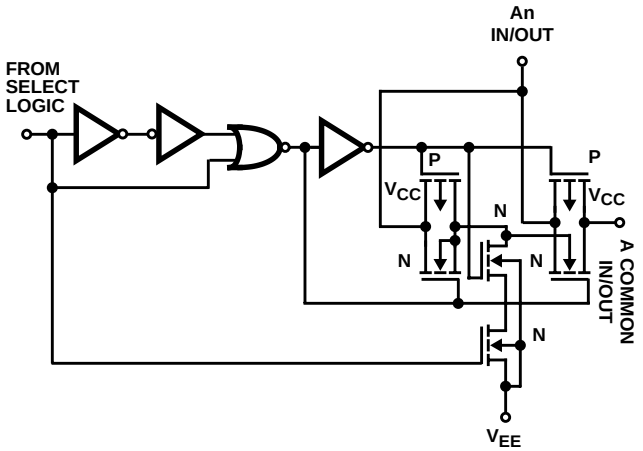
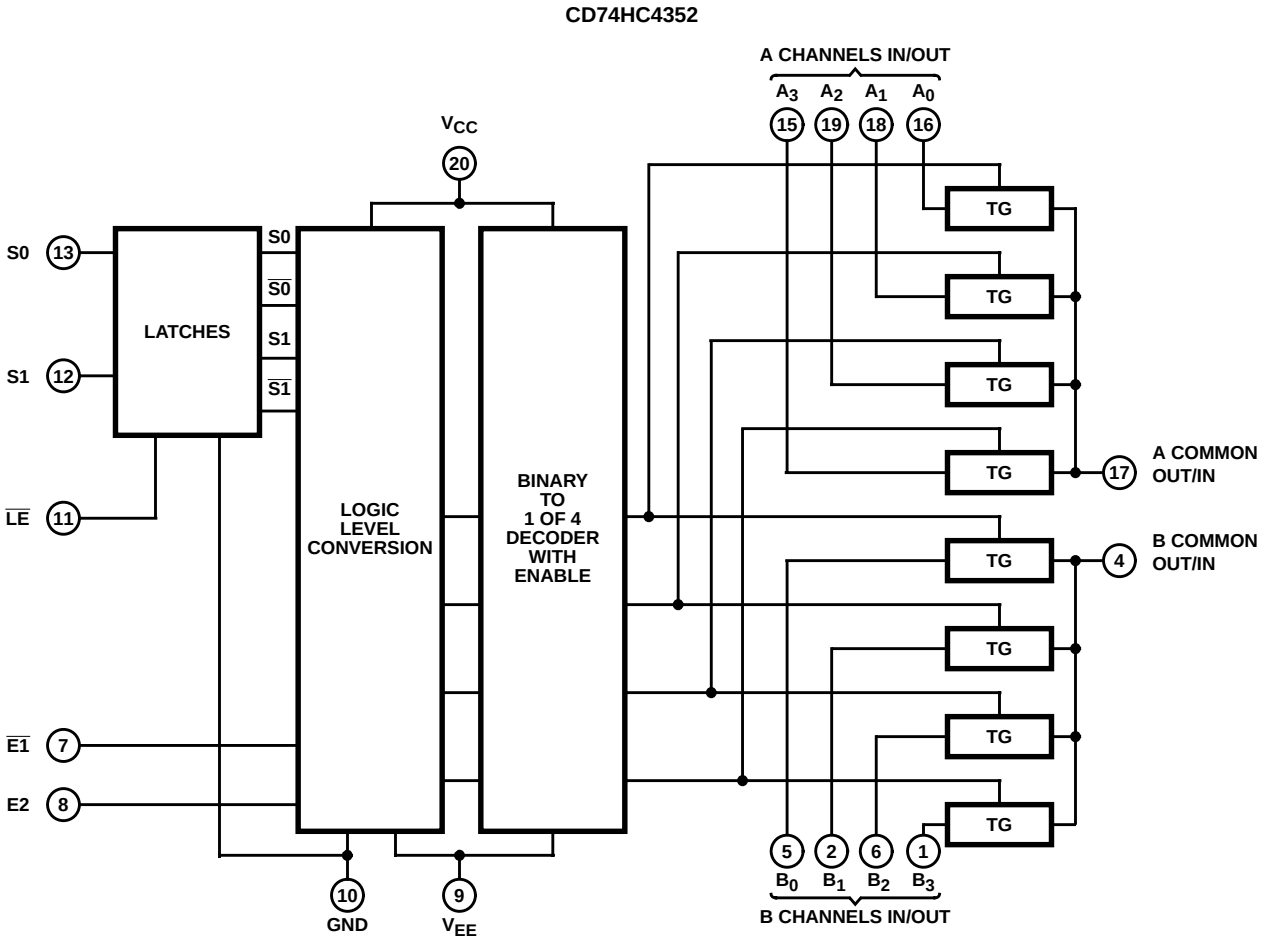


FIGURE 1. DETAIL OF ONE HC/HCT4351 SWITCH

Functional Diagram



TRUTH TABLE
CD74HC4352

INPUT STATES				(NOTE 4) "ON" SWITCHES
$\overline{E1}$	E2	S1	S0	$\overline{LE}$ = H
L	H	L	L	A_0, B_0
L	H	L	H	A_1, B_1
L	H	H	L	A_2, B_2
L	H	H	H	A_3, B_3
H	L	X	X	None

NOTE:

4. When Latch Enable is "Low" channel-select data is latched and switches cannot change state.
   H = High Voltage Level, L = Low Voltage Level, X = Don't Care

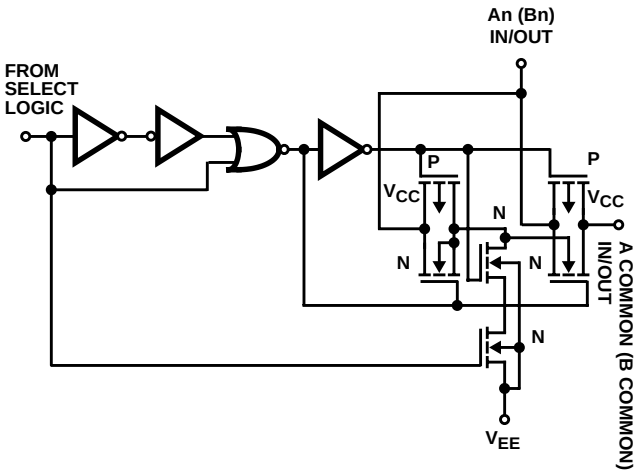


FIGURE 2. DETAIL OF ONE CD74HC4352 SWITCH

Absolute Maximum Ratings

DC Supply Voltage, V_{CC} . . . . . -0.5V to 7V
DC Supply Voltage, V_{CC} - V_{EE} . . . . . -0.5V to 10.5V
DC Supply Voltage, V_{EE} . . . . . 0.5V to -7V
DC Input Diode Current, I_{IK}
For V_I < -0.5V or V_I > V_{CC} 0.5V. . . . . ±20mA
DC Switch Diode Current, I_{OK}
For V_I < V_{EE} -0.5V or V_I < V_{CC} + 0.5V . . . . . ±25mA
DC Switch Current, I_{OK} (Note 5)
For V_I > V_{EE} -0.5V or V_I < V_{CC} + 0.5V . . . . . ±20mA
DC Output Diode Current, I_{OK}
For V_O < -0.5V or V_O > V_{CC} + 0.5V . . . . . ±20mA
DC Output Source or Sink Current per Output Pin, I_O
For V_O > -0.5V or V_O < V_{CC} + 0.5V . . . . . ±25mA
DC V_{CC} or Ground Current, I_{CC} . . . . . ±50mA

Operating Conditions

Temperature Range, T_A . . . . . -55^oC to 125^oC
Supply Voltage Range, V_{CC}
HC Types . . . . . 2V to 6V
HCT Types . . . . . 4.5V to 5.5V
Supply Voltage Range, V_{CC} - V_{EE}
HC, HCT Types (Figure 3) . . . . . 2V to 10V
Supply Voltage Range, V_{EE}
HC, HCT Types (Figure 4) . . . . . 0V to -6V
DC Input or Output Voltage, V_I . . . . . GND to V_{CC}
Analog Switch I/O Voltage, V_{IS} . . . . . V_{EE} (Min)
. . . . . V_{CC} (Max)
Input Rise and Fall Time, t_r, t_f
2V . . . . . 1000ns (Max)
4.5V. . . . . 500ns (Max)
6V . . . . . 400ns (Max)

Thermal Information

Thermal Resistance (Typical, Note 6)	θ_{JA} ($^oC/W$)
PDIP Package	125
SOIC Package	120

Maximum Junction Temperature . . . . . 150^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

5. In certain applications, the external load-resistor current may include both V_{CC} and signal-line components. To avoid drawing V_{CC} current when switch current flows into the transmission gate inputs, the voltage drop across the bidirectional switch must not exceed 0.6V (calculated from R_{ON} values shown in the DC Electrical Specifications table). No V_{CC} current will flow through R_L if the switch current flows into terminal 3 on the 'HC4351 and CD74HCT4351; terminals 3 and 13 on the CD74HC4352.
6. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Recommended Operating Area as a Function of Supply Voltage

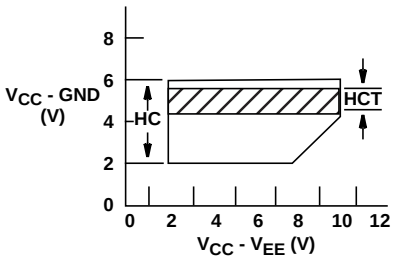


FIGURE 3.

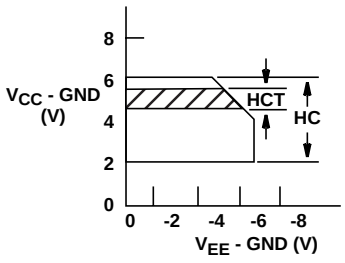


FIGURE 4.

DC Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS				25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
		V_I (V)	V_{IS} (V)	V_{EE} (V)	V_{CC} (V)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES													
High Level Input Voltage	V_{IH}	-	-	-	2	1.5	-	-	1.5	-	1.5	-	V
					4.5	3.15	-	-	3.15	-	3.15	-	V
					6	4.2	-	-	4.2	-	4.2	-	V
Low Level Input Voltage	V_{IL}	-	-	-	2	-	-	0.5	-	0.5	-	0.5	V
					4.5	-	-	1.35	-	1.35	-	1.35	V
					6	-	-	1.8	-	1.8	-	1.8	V
"ON" Resistance I_O = 1mA Figure 9	R_{ON}	V_{IH} or V_{IL}	V_{CC} or V_{EE}	0	4.5	-	70	160	-	200	-	240	Ω
				0	6	-	60	140	-	175	-	210	Ω
				-4.5	4.5	-	40	120	-	150	-	180	Ω
			V_{CC} to V_{EE}	0	4.5	-	90	180	-	225	-	270	Ω
				0	6	-	80	160	-	200	-	240	Ω
				-4.5	4.5	-	45	130	-	162	-	195	Ω
Maximum "ON" Resistance Between Any Two Channels	ΔR_{ON}	-	-	0	4.5	-	10	-	-	-	-	-	Ω
				0	6	-	8.5	-	-	-	-	-	Ω
				-4.5	4.5	-	5	-	-	-	-	-	Ω
Switch On/Off Leakage Current 4 Channels (4352)	I_{IZ}	V_{IH} or V_{IL}	For Switch OFF: When $V_{IS} = V_{CC}$ $V_{OS} = V_{EE}$; When $V_{IS} = V_{EE}$, $V_{OS} = V_{CC}$ For Switch ON: All Applicable Combinations of V_{IS} and V_{OS} Voltage Levels	0	6	-	-	±0.1	-	±1	-	±1	µA
				-5	5	-	-	±0.2	-	±2	-	±2	µA
Switch On/Off Leakage Current 8 Channels (4351)				0	6	-	-	±0.2	-	±2	-	±2	µA
				-5	5	-	-	±0.4	-	±4	-	±4	µA
Control Input Leakage Current	I_{IL}	V_{CC} or GND	-	0	6	-	-	±0.1	-	±1	-	±1	µA
Quiescent Device Current I_O = 0	I_{CC}	V_{CC} or GND	When $V_{IS} = V_{EE}$, $V_{OS} = V_{CC}$, When $V_{IS} = V_{CC}$, $V_{OS} = V_{EE}$	0	6	-	-	8	-	80	-	160	µA
				-5	5	-	-	16	-	160	-	320	µA

DC Electrical Specifications (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS				25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
		V_I (V)	V_{IS} (V)	V_{EE} (V)	V_{CC} (V)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HCT TYPES													
High Level Input Voltage	V_{IH}	-	-	-	4.5 to 5.5	2	-	-	2	-	2	-	V
Low Level Input Voltage	V_{IL}	-	-	-	4.5 to 5.5	-	-	0.8	-	0.8	-	0.8	V
"ON" Resistance I_O = 1mA Figure 9	R_{ON}	V_{IH} or V_{IL}	V_{CC} or V_{EE}	0	4.5	-	70	160	-	200	-	240	Ω
				-4.5	4.5	-	40	120	-	150	-	180	Ω
			V_{CC} to V_{EE}	0	4.5	-	90	180	-	225	-	270	Ω
				-4.5	4.5	-	45	130	-	162	-	195	Ω
Maximum "ON" Resistance Between Any Two Channels	ΔR_{ON}	-	-	0	4.5	-	10	-	-	-	-	-	Ω
				-4.5	4.5	-	5	-	-	-	-	-	Ω
Switch On/Off Leakage Current 4 Channels (4352)	I_{IZ}	V_{IH} or V_{IL}	For Switch OFF: When $V_{IS} = V_{CC}$ $V_{OS} = V_{EE}$; When $V_{IS} = V_{EE}$, $V_{OS} = V_{CC}$ For Switch ON: All Applicable Combinations of V_{IS} and V_{OS} Voltage Levels	0	6	-	-	±0.1	-	±1	-	±1	µA
				-5	5	-	-	±0.2	-	±2	-	±2	µA
Switch On/Off Leakage Current 8 Channels (4351)				0	6	-	-	±0.2	-	±2	-	±2	µA
				-5	5	-	-	±0.4	-	±4	-	±4	µA
Control Input Leakage Current	I_I	V_{CC} or GND	-	0	5.5	-	-	±0.1	-	±1	-	±1	µA
Quiescent Device Current I_O = 0	I_{CC}	Any Voltage Between V_{CC} and GND	When $V_{IS} = V_{EE}$, $V_{OS} = V_{CC}$, When $V_{IS} = V_{CC}$, $V_{OS} = V_{EE}$	0	5.5	-	-	8	-	80	-	160	µA
				-4.5	5.5	-	-	16	-	160	-	320	µA
Additional Quiescent Device Current Per Input Pin: 1 Unit Load	ΔI_{CC}	V_{CC} -2.1	-	-	4.5 to 5.5	-	100	360	-	450	-	490	µA

NOTE: For dual-supply systems theoretical worst case (V_I = 2.4V, V_{CC} = 5.5V) specification is 1.8mA.

HCT Input Loading Table

TYPE	INPUT	UNIT LOADS
All	$\overline{E1}$, E2, Sn	0.5
(4351, 4352)	$\overline{LE}$	1.5

NOTE: Unit Load is ΔI_{CC} limit specified in DC Electrical Table, e.g., 360µA max at 25°C.

Switching Specifications Input t_r, t_f = 6ns

PARAMETER	SYMBOL	TEST CONDITIONS	V_{EE} (V)	V_{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
					MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES												
Propagation Delay, Switch In to Switch Out	t_{PLH}, t_{PHL}	C_L = 50pF	0	2	-	-	35	-	45	-	55	ns
			0	4.5	-	-	7	-	9	-	11	ns
			0	6	-	-	6	-	8	-	9	ns
			-4.5	4.5	-	-	5	-	7	-	8	ns
Maximum Switch Turn “ON” Delay 4351 $\overline{E1}$, E2, $\overline{LE}$ to V_{OS}	t_{PZH}, t_{PZL}	C_L = 50pF	0	2	-	-	300	-	375	-	450	ns
			0	4.5	-	-	60	-	75	-	90	ns
			0	6	-	-	51	-	64	-	77	ns
			-4.5	4.5	-	-	55	-	69	-	83	ns
		C_L = 15pF	-	5	-	27	-	-	-	-	-	ns
Maximum Switch Turn “ON” Delay 4352 $\overline{E1}$, E2, $\overline{LE}$ to V_{OS}	t_{PZH}, t_{PZL}	C_L = 50pF	0	2	-	-	350	-	440	-	525	ns
			0	4.5	-	-	70	-	88	-	105	ns
			0	6	-	-	60	-	75	-	90	ns
			-4.5	4.5	-	-	60	-	75	-	90	ns
		C_L = 15pF	-	5	-	35	-	-	-	-	-	ns
Maximum Switch Turn “ON” Delay 4351 Sn to V_{OS}	t_{PZH}, t_{PZL}	C_L = 50pF	0	2	-	-	300	-	375	-	450	ns
			0	4.5	-	-	60	-	75	-	90	ns
			0	6	-	-	51	-	64	-	77	ns
			-4.5	4.5	-	-	50	-	63	-	75	ns
		C_L = 15pF	-	5	-	27	-	-	-	-	-	ns
Maximum Switch Turn “ON” Delay 4352 Sn to V_{OS}	t_{PZH}, t_{PZL}	C_L = 50pF	0	2	-	-	375	-	470	-	565	ns
			0	4.5	-	-	75	-	94	-	113	ns
			0	6	-	-	64	-	80	-	96	ns
			-4.5	4.5	-	-	55	-	69	-	83	ns
		C_L = 15pF	-	5	-	35	-	-	-	-	-	ns
Maximum Switch Turn “OFF” Delay 4351 $\overline{E1}$ to V_{OS}	t_{PHZ}, t_{PLZ}	C_L = 50pF	0	2	-	-	250	-	315	-	375	ns
			0	4.5	-	-	50	-	63	-	75	ns
			0	6	-	-	43	-	54	-	64	ns
			-4.5	4.5	-	-	40	-	50	-	60	ns
		C_L = 15pF	-	5	-	21	-	-	-	-	-	ns

Switching Specifications Input t_r, t_f = 6ns **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	V_{EE} (V)	V_{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
					MIN	TYP	MAX	MIN	MAX	MIN	MAX	
Maximum Switch Turn "OFF" Delay 4351 E2 to V_{OS}	t_{PHZ}, t_{PLZ}	C_L = 50pF	0	2	-	-	250	-	315	-	375	ns
			0	4.5	-	-	50	-	63	-	75	ns
			0	6	-	-	43	-	54	-	64	ns
			-4.5	4.5	-	-	40	-	50	-	60	ns
		C_L = 15pF	-	5	-	21	-	-	-	-	-	ns
Maximum Switch Turn "OFF" Delay 4351 $\overline{LE}$ to V_{OS}	t_{PHZ}, t_{PLZ}	C_L = 50pF	0	2	-	-	275	-	345	-	415	ns
			0	4.5	-	-	55	-	69	-	83	ns
			0	6	-	-	47	-	59	-	71	ns
			-4.5	4.5	-	-	45	-	56	-	68	ns
Maximum Switch Turn "OFF" Delay 4351 Sn to V_{OS}	t_{PHZ}, t_{PLZ}	C_L = 50pF	0	2	-	-	275	-	345	-	415	ns
			0	4.5	-	-	55	-	69	-	83	ns
			0	6	-	-	47	-	59	-	71	ns
			-4.5	4.5	-	-	48	-	60	-	71	ns
		C_L = 15pF	-	5	-	21	-	-	-	-	-	ns
Maximum Switch Turn "OFF" Delay 4352 $\overline{E1}$, E2, $\overline{LE}$ to V_{OS}	t_{PHZ}, t_{PLZ}	C_L = 50pF	0	2	-	-	275	-	345	-	415	ns
			0	4.5	-	-	55	-	69	-	83	ns
			0	6	-	-	47	-	59	-	71	ns
			-4.5	4.5	-	-	50	-	63	-	75	ns
		C_L = 15pF	-	5	-	21	-	-	-	-	-	ns
Setup Time 4351 Sn to $\overline{LE}$	t_{SU}	C_L = 50pF	0	2	-	-	60	-	75	-	90	ns
			0	4.5	-	-	12	-	15	-	18	ns
			0	6	-	-	10	-	13	-	15	ns
			-4.5	4.5	-	-	18	-	23	-	27	ns
Hold Time 4351 and 4352 Sn to $\overline{LE}$	t_H	C_L = 50pF	0	2	5	-	-	5	-	5	-	ns
			0	4.5	5	-	-	5	-	5	-	ns
			0	6	5	-	-	5	-	5	-	ns
			-4.5	4.5	5	-	-	5	-	5	-	ns
Pulse Width 4351 and 4352 $\overline{LE}$	t_W	C_L = 50pF	0	2	100	-	-	125	-	150	-	ns
			0	4.5	20	-	-	25	-	30	-	ns
			0	6	17	-	-	21	-	26	-	ns
			-4.5	4.5	25	-	-	31	-	38	-	ns
Input (Control) Capacitance	C_I	-	-	-	-	-	10	-	10	-	10	pF
Power Dissipation Capacitance (Notes 7, 8) 4351	C_{PD}	-	-	5	-	50	-	-	-	-	-	pF

Switching Specifications Input t_r, t_f = 6ns **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	V_{EE} (V)	V_{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
					MIN	TYP	MAX	MIN	MAX	MIN	MAX	
Power Dissipation Capacitance (Notes 7, 8) 4352	C_{PD}	-	-	5	-	74	-	-	-	-	-	pF
HCT TYPES												
Propagation Delay, Switch In to Switch Out	t_{PLH}, t_{PHL}	C_L = 50pF	0	4.5	-	-	7	-	9	-	11	ns
			-4.5	4.5	-	-	5	-	7	-	8	ns
Maximum Switch Turn “ON” Delay 4351 $\overline{E1}$, E2, $\overline{LE}$ to V_{OS}	t_{PZH}, t_{PZL}	C_L = 50pF	0	4.5	-	-	75	-	94	-	113	ns
			-4.5	4.5	-	-	60	-	75	-	90	ns
		C_L = 15pF	-	5	-	35	-	-	-	-	-	ns
Maximum Switch Turn “ON” Delay 4351 Sn to V_{OS}	t_{PZH}, t_{PZL}	C_L = 50pF	0	4.5	-	-	75	-	94	-	113	ns
			-4.5	4.5	-	-	60	-	75	-	90	ns
		C_L = 15pF	-	5	-	35	-	-	-	-	-	ns
Maximum Switch Turn “OFF” Delay 4351 $\overline{E1}$ to V_{OS}	t_{PHZ}, t_{PLZ}	C_L = 50pF	0	4.5	-	-	55	-	69	-	83	ns
			-4.5	4.5	-	-	40	-	50	-	60	ns
		C_L = 15pF	-	5	-	23	-	-	-	-	-	ns
Maximum Switch Turn “OFF” Delay 4351 E2 to V_{OS}	t_{PHZ}, t_{PLZ}	C_L = 50pF	0	4.5	-	-	60	-	75	-	90	ns
			-4.5	4.5	-	-	50	-	63	-	75	ns
		C_L = 15pF	-	5	-	23	-	-	-	-	-	ns
Maximum Switch Turn “OFF” Delay 4351 $\overline{LE}$ to V_{OS}	t_{PHZ}, t_{PLZ}	C_L = 50pF	0	4.5	-	-	60	-	75	-	90	ns
			-4.5	4.5	-	-	55	-	69	-	83	ns
Maximum Switch Turn “OFF” Delay 4351 Sn to V_{OS}	t_{PHZ}, t_{PLZ}	C_L = 50pF	0	4.5	-	-	65	-	81	-	98	ns
			-4.5	4.5	-	-	55	-	69	-	83	ns
		C_L = 15pF	-	5	-	23	-	-	-	-	-	ns
Setup Time 4351 Sn to $\overline{LE}$		C_L = 50pF	0	4.5	-	-	12	-	15	-	18	ns
			-4.5	4.5	-	-	14	-	18	-	21	ns
Hold Time 4351 and 4352 Sn to $\overline{LE}$		C_L = 50pF	0	4.5	5	-	-	5	-	5	-	ns
			-4.5	4.5	5	-	-	5	-	5	-	ns
Pulse Width 4351 $\overline{LE}$	t_W	C_L = 50pF	0	4.5	25	-	-	31	-	28	-	ns
			-4.5	4.5	25	-	-	31	-	38	-	ns
Input (Control) Capacitance	C_I	-	-	-	-	-	10	-	10	-	10	pF
Power Dissipation Capacitance (Notes 7, 8) 4351	C_{PD}	-	-	5	-	52	-	-	-	-	-	pF

NOTES:

7. C_{PD} is used to determine the dynamic power consumption, per package.
8. $P_D = C_{PD} V_{CC}^2 f_i + \Sigma (C_L + C_S) V_{CC}^2 f_o$ where f_i = input frequency, f_o = output frequency, C_L = output load capacitance, C_S = switch capacitance, V_{CC} = supply voltage.

Analog Channel Specifications $T_A = 25^oC$

PARAMETER	SYMBOL	TEST CONDITIONS	TYPE	V_{EE} (V)	V_{CC} (V)	HC/HCT	UNITS
Switch Input Capacitance	C_I		All	-	-	5	pF
Common Capacitance	C_{COM}		4351	-	-	25	pF
			4352	-	-	12	pF
Minimum Switch Frequency Response at -3dB (Figure 5, 7)	f_{MAX}	See Figure 11 Notes 9, 10	4351	-	-	145	MHz
			4352	-2.25	2.25	165	MHz
			4351	-	-	180	MHz
			4352	-4.5	4.5	185	MHz
Crosstalk Between Any Two Switches (Note 12)		See Figure 10 Notes 10, 11	4351	-	-	N/A	dB
			4352	-2.25	2.25	(TBE)	dB
			4351	-	-	N/A	dB
			4352	-4.5	4.5	(TBE)	dB
Sine-Wave Distortion		See Figure 12	All	-2.25	2.25	0.035	%
			All	-4.5	4.5	0.018	%
$\overline{E}$ or S to Switch Feedthrough Noise		See Figure 13 Notes 10, 11	4351	-	-	-	mV
			4352	-2.25	2.25	(TBE)	mV
			4351	-	-	-	mV
			4352	-4.5	4.5	(TBE)	mV
Switch “OFF” Signal Feedthrough (Figure 6, 8)		See Figure 14 Notes 10, 11	4351	-	-	-73	dB
			4352	-2.25	2.25	-65	dB
			4351	-	-	-75	dB
			4352	-4.5	4.5	-67	dB

NOTES:

9. Adjust input voltage to obtain 0dBm at V_{OS} for, f_{in} = 1MHz.
10. V_{IS} is centered at $(V_{CC} - V_{EE})/2$.
11. Adjust input for 0dBm.
12. Not applicable for ’HC4351 and CD74HCT4351.

Typical Performance Curves

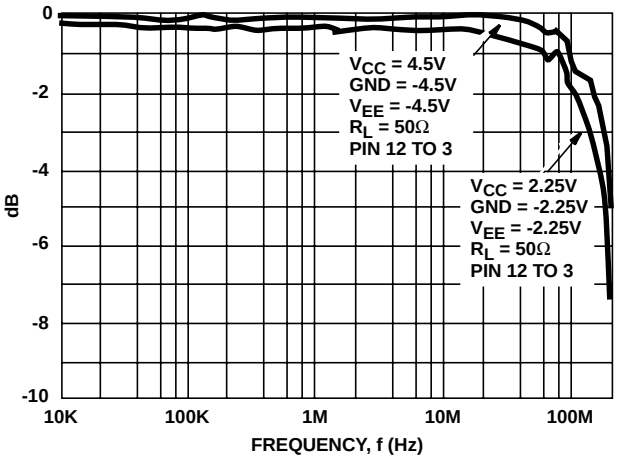


FIGURE 5. CHANNEL ON BANDWIDTH ('HC4351, CD74HCT4351)

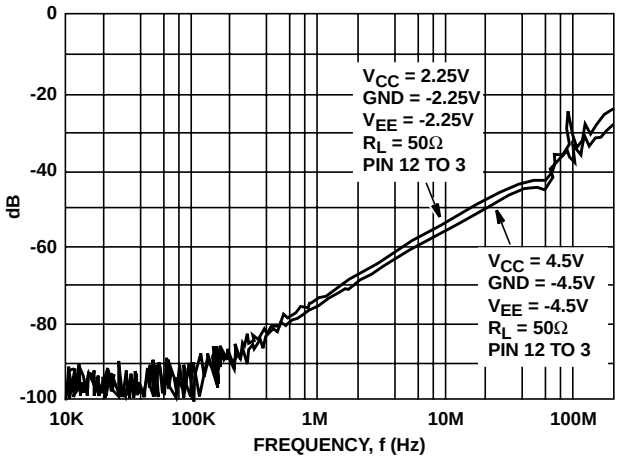


FIGURE 6. CHANNEL OFF FEEDTHROUGH ('HC4351, CD74HCT4351)

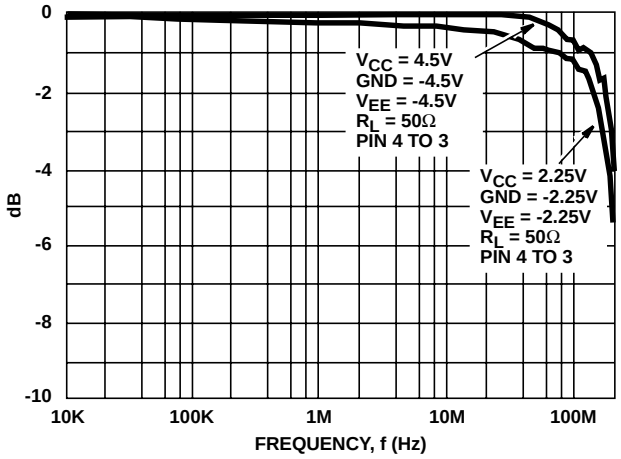


FIGURE 7. CHANNEL ON BANDWIDTH (CD74HC4352)

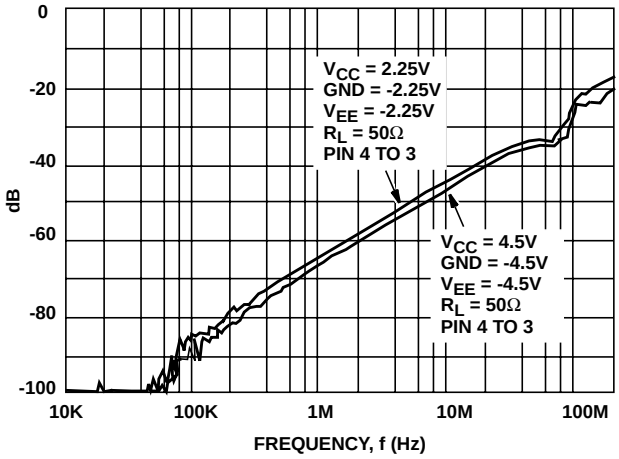


FIGURE 8. CHANNEL OFF FEEDTHROUGH (CD74HC4352)

Typical Performance Curves (Continued)

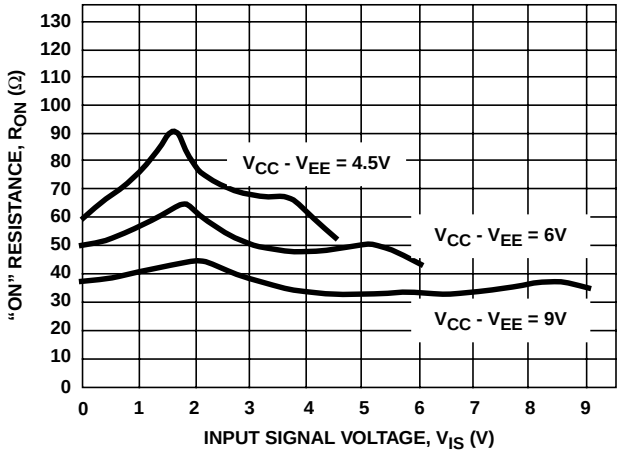
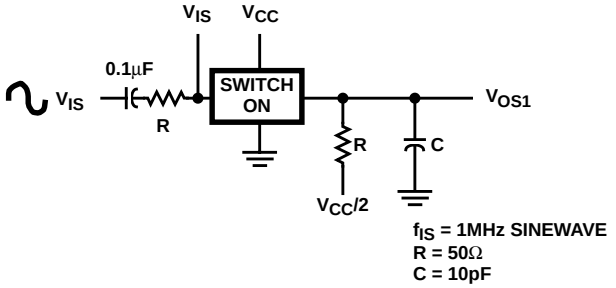


FIGURE 9. TYPICAL ON RESISTANCE vs INPUT SIGNAL VOLTAGE

Analog Test Circuits



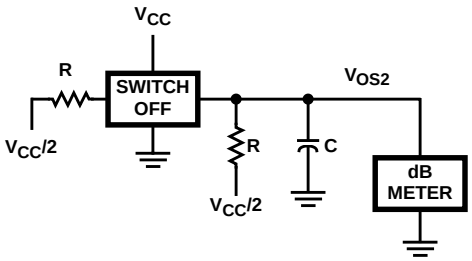


FIGURE 10. CROSSTALK BETWEEN TWO SWITCHES TEST CIRCUIT

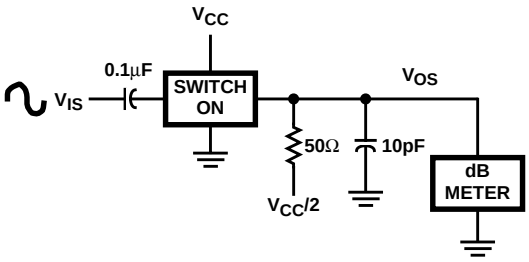


FIGURE 11. FREQUENCY RESPONSE TEST CIRCUIT

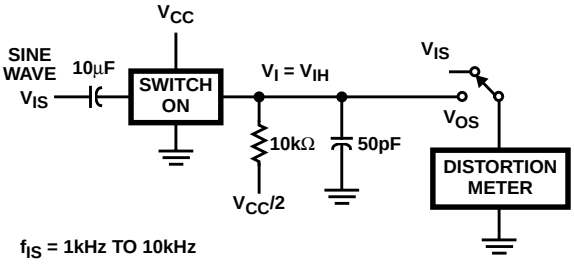


FIGURE 12. TOTAL HARMONIC DISTORTION TEST CIRCUIT

Analog Test Circuits (Continued)

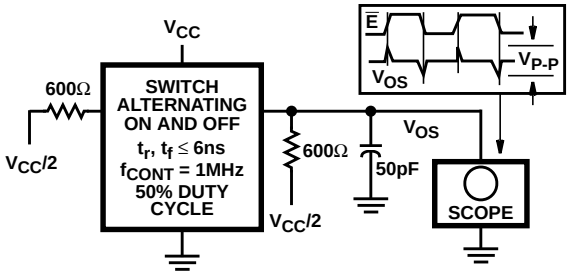


FIGURE 13. CONTROL-TO-SWITCH FEEDTHROUGH NOISE TEST CIRCUIT

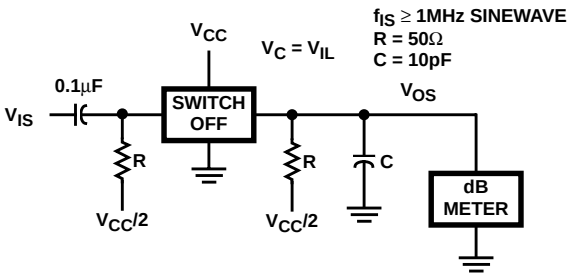
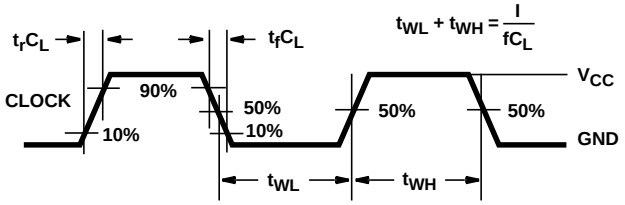


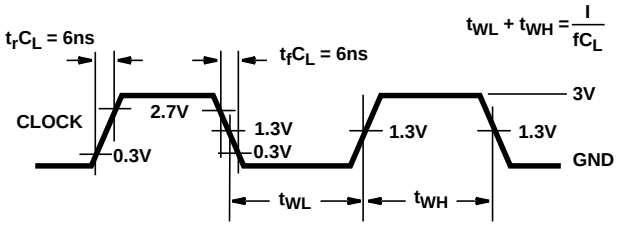
FIGURE 14. SWITCH OFF SIGNAL FEEDTHROUGH

Test Circuits and Waveforms



NOTE: Outputs should be switching from 10% V_{CC} to 90% V_{CC} in accordance with device truth table. For f_{MAX}, input duty cycle = 50%.

FIGURE 15. HC CLOCK PULSE RISE AND FALL TIMES AND PULSE WIDTH



NOTE: Outputs should be switching from 10% V_{CC} to 90% V_{CC} in accordance with device truth table. For f_{MAX}, input duty cycle = 50%.

FIGURE 16. HCT CLOCK PULSE RISE AND FALL TIMES AND PULSE WIDTH

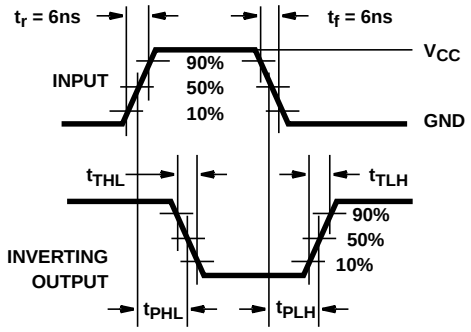


FIGURE 17. HC TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

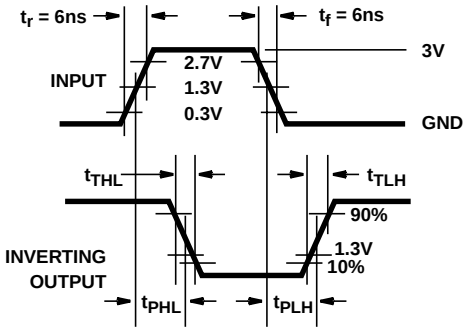


FIGURE 18. HCT TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

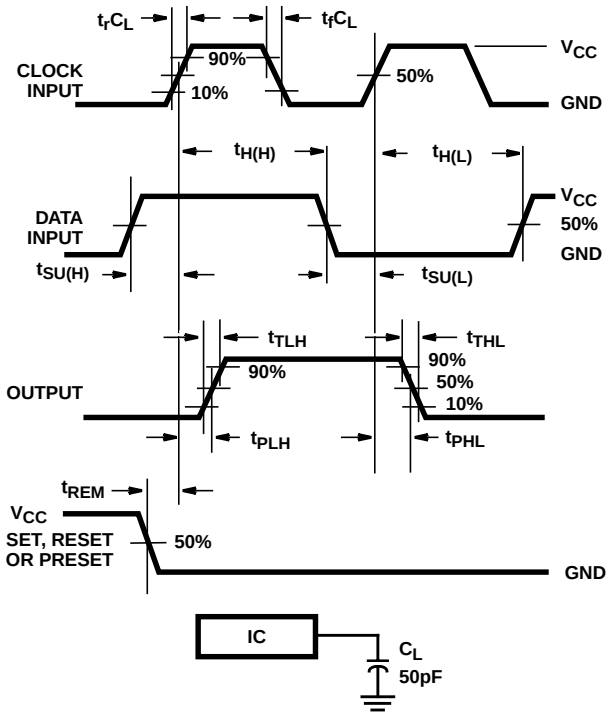


FIGURE 19. HC SETUP TIMES, HOLD TIMES, REMOVAL TIME, AND PROPAGATION DELAY TIMES FOR EDGE TRIGGERED SEQUENTIAL LOGIC CIRCUITS

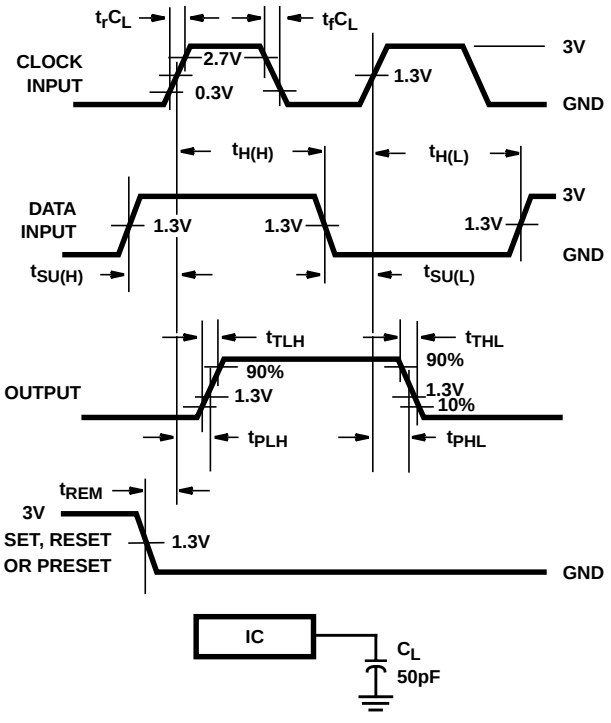


FIGURE 20. HCT SETUP TIMES, HOLD TIMES, REMOVAL TIME, AND PROPAGATION DELAY TIMES FOR EDGE TRIGGERED SEQUENTIAL LOGIC CIRCUITS

Test Circuits and Waveforms (Continued)

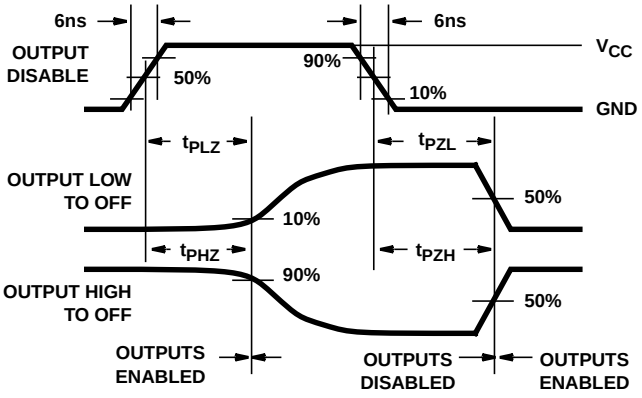


FIGURE 21. HC THREE-STATE PROPAGATION DELAY WAVEFORM

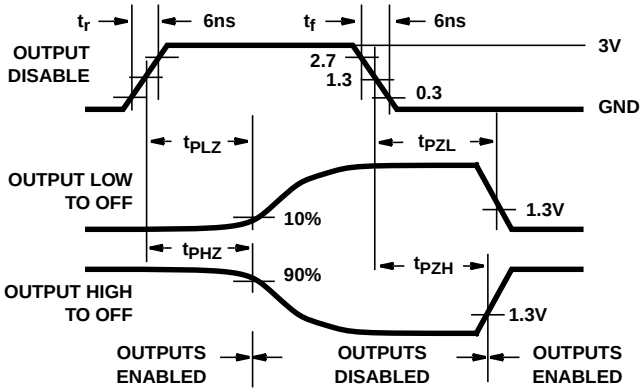
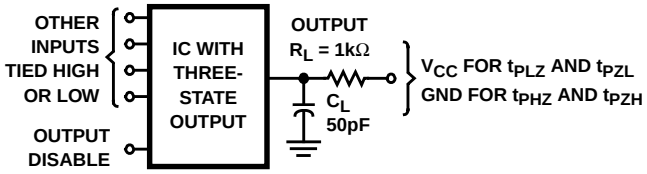


FIGURE 22. HCT THREE-STATE PROPAGATION DELAY WAVEFORM



NOTE: Open drain waveforms t_{PLZ} and t_{PZL} are the same as those for three-state shown on the left. The test circuit is Output R_L = 1kΩ to V_{CC}, C_L = 50pF.

FIGURE 23. HC AND HCT THREE-STATE PROPAGATION DELAY TEST CIRCUIT

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgment, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Customers are responsible for their applications using TI components.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.