

SN54HC393, SN74HC393 DUAL 4-BIT BINARY COUNTERS

SCLS143B – DECEMBER 1982 – REVISED MAY 1997

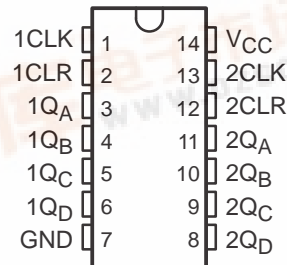
- Dual 4-Bit Binary Counters With Individual Clocks
- Direct Clear for Each 4-Bit Counter
- Can Significantly Improve System Densities by Reducing Counter Package Count by 50 Percent
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs

description

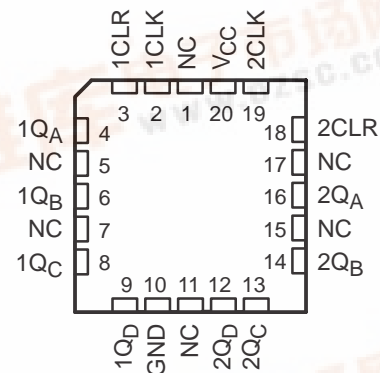
The 'HC393 contain eight flip-flops and additional gating to implement two individual 4-bit counters in a single package. The 'HC393 comprise two independent 4-bit binary counters, each having a clear (CLR) and a clock (CLK) input. N-bit binary counters can be implemented with each package, providing the capability of divide by 256. The 'HC393 have parallel outputs from each counter stage so that any submultiple of the input count frequency is available for system timing signals.

The SN54HC393 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74HC393 is characterized for operation from -40°C to 85°C .

SN54HC393 . . . J OR W PACKAGE
SN74HC393 . . . D, DB, OR N PACKAGE
(TOP VIEW)



SN54HC393 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

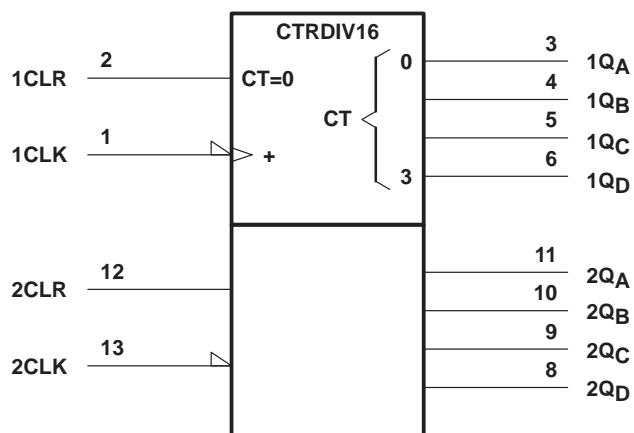
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FUNCTION TABLE COUNT SEQUENCE
(each counter)

COUNT	OUTPUTS			
	Q _D	Q _C	Q _B	Q _A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

logic symbol†

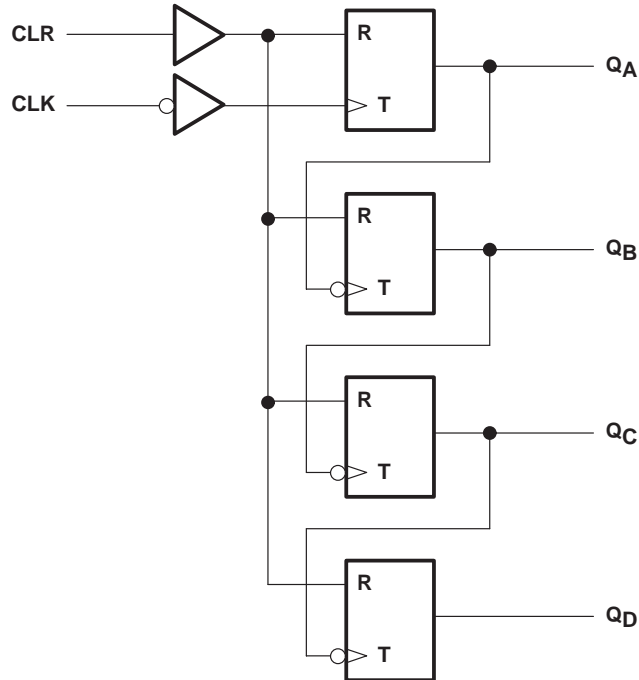


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the D, DB, J, N, and W packages.

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logic diagram, each counter (positive logic)



absolute maximum ratings over operating free-air temperature range†

Supply voltage range, V_{CC}	-0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1)	± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1)	± 20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 25 mA
Continuous current through V_{CC} or GND	± 50 mA
Package thermal impedance, θ_{JA} (see Note 2): D package	127°C/W
DB package	158°C/W
N package	78°C/W
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

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recommended operating conditions

		SN54HC393			SN74HC393			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	2	5	6	2	5	6	V
V _{IH}	High-level input voltage	V _{CC} = 2 V	1.5		1.5		V	
		V _{CC} = 4.5 V	3.15		3.15			
		V _{CC} = 6 V	4.2		4.2			
V _{IL}	Low-level input voltage	V _{CC} = 2 V	0	0.5	0	0.5	V	
		V _{CC} = 4.5 V	0	1.35	0	1.35		
		V _{CC} = 6 V	0	1.8	0	1.8		
V _I	Input voltage	0	V _{CC}		0	V _{CC}		V
V _O	Output voltage	0	V _{CC}		0	V _{CC}		V
t _t [†]	Input transition (rise and fall) time	V _{CC} = 2 V	0	1000	0	1000		ns
		V _{CC} = 4.5 V	0	500	0	500		
		V _{CC} = 6 V	0	400	0	400		
T _A	Operating free-air temperature	-55		125	-40		85	°C

[†] If this device is used in the threshold region (from V_{IL}max = 0.5 V to V_{IH}min = 1.5 V), there is a potential to go into the wrong state from induced grounding, causing double clocking. Operating with the inputs at t_t = 1000 ns and V_{CC} = 2 V does not damage the device; however, functionally, the CLK inputs are not ensured while in the shift, count, or toggle operating modes.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			SN54HC393		SN74HC393		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	V _I = V _{IH} or V _{IL}	I _{OH} = -20 μA	2 V	1.9	1.998	1.9	1.9		V	
			4.5 V	4.4	4.499	4.4	4.4			
		6 V	5.9	5.999	5.9	5.9				
		I _{OH} = -4 mA	4.5 V	3.98	4.3	3.7	3.84			
		I _{OH} = -5.2 mA	6 V	5.48	5.8	5.2	5.34			
V _{OL}	V _I = V _{IH} or V _{IL}	I _{OL} = 20 μA	2 V	0.002 0.1		0.1		0.1		V
			4.5 V	0.001 0.1		0.1		0.1		
			6 V	0.001 0.1		0.1		0.1		
		I _{OL} = 4 mA	4.5 V	0.17 0.26		0.4		0.33		
		I _{OL} = 5.2 mA	6 V	0.15 0.26		0.4		0.33		
I _I	V _I = V _{CC} or 0	6 V	±0.1 ±100		±1000		±1000		nA	
I _{CC}	V _I = V _{CC} or 0, I _O = 0	6 V	8		160		80		μA	
C _i		2 V to 6 V	3 10		10		10		pF	

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timing requirements over recommended operating free-air temperature range (unless otherwise noted)

		V _{CC}	T _A = 25°C		SN54HC393		SN74HC393		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency	2 V	0	6	0	4.2	0	5	MHz
		4.5 V	0	31	0	21	0	25	
		6 V	0	36	0	25	0	28	
t _w	Pulse duration	CLK high or low	2 V	80	120	100	ns		
			4.5 V	16	24	20			
			6 V	14	20	18			
		CLR high	2 V	80	120	100			
			4.5 V	16	24	20			
			6 V	14	20	18			
t _{su}	Setup time, CLR inactive	2 V	25	25	25	ns			
		4.5 V	5	5	5				
		6 V	5	5	5				

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC}	T _A = 25°C			SN54HC393		SN74HC393		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f _{max}	CLK	Q _A	2 V	6	10	4.2	5	MHz			
			4.5 V	31	50	21	25				
			6 V	36	60	25	28				
t _{pd}	CLK	Q _A	2 V	50	120	180	150	ns			
			4.5 V	15	24	36	30				
			6 V	13	20	31	26				
		Q _B	2 V	72	190	285	240				
			4.5 V	22	38	57	47				
			6 V	18	32	48	40				
		Q _C	2 V	91	240	360	300				
			4.5 V	28	48	72	60				
			6 V	22	41	61	51				
		Q _D	2 V	100	290	430	360				
			4.5 V	32	58	87	72				
			6 V	24	50	74	62				
t _{PHL}	CLR	Any	2 V	45	165	250	205	ns			
			4.5 V	17	33	49	41				
			6 V	14	28	42	35				
t _t		Any	2 V	28	75	110	95	ns			
			4.5 V	8	15	22	19				
			6 V	6	13	19	16				

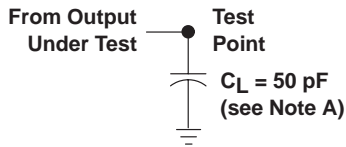
operating characteristics, T_A = 25°C

PARAMETER	TEST CONDITIONS	TYP	UNIT
C _{pd} Power dissipation capacitance per counter	No load	40	pF

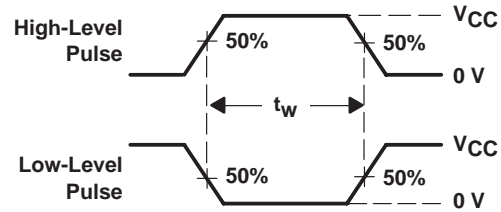
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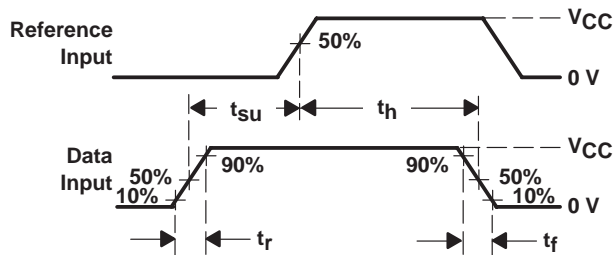
PARAMETER MEASUREMENT INFORMATION



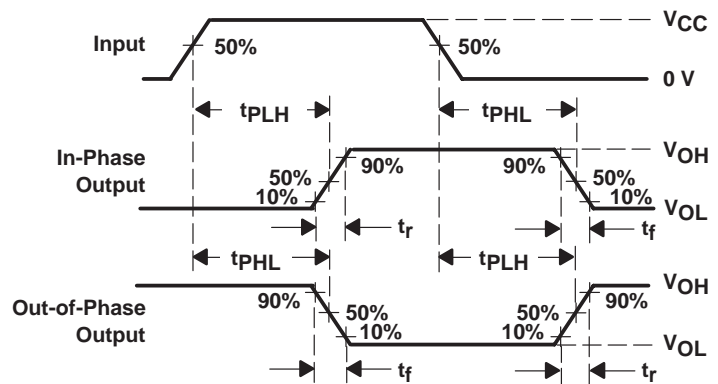
LOAD CIRCUIT



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
SETUP AND HOLD AND INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES

- NOTES:
- C_L includes probe and test-fixture capacitance.
 - Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r = 6 \text{ ns}$, $t_f = 6 \text{ ns}$.
 - For clock inputs, f_{max} is measured when the input duty cycle is 50%.
 - The outputs are measured one at a time with one input transition per measurement.
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

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