

SCLS167

SN54HC7266, SN74HC7266 QUADRUPLE 2-INPUT EXCLUSIVE-NOR GATES

D2804, MARCH 1984—REVISED SEPTEMBER 1987

- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability
- Totem-Pole Version of HC266

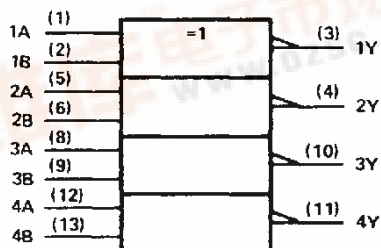
description

These devices are composed of four independent 2-input exclusive-NOR gates. They perform the Boolean functions:

$$Y = A \oplus B = \overline{A}B + A\overline{B} \text{ in positive logic.}$$

The SN54HC7266 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74HC7266 is characterized for operation from -40°C to 85°C .

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

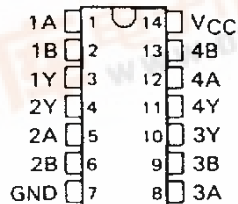
Pin numbers shown are for J or N packages.

logic symbol (each gate, positive logic)



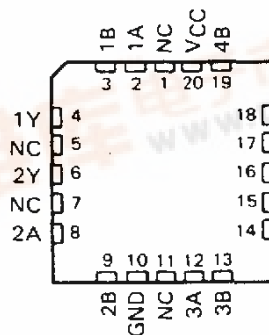
SN54HC7266 ... J PACKAGE SN74HC7266 ... D OR N PACKAGE

(TOP VIEW)



SN54HC7266 ... FK PACKAGE

(TOP VIEW)



NC—No internal connection

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	H

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absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC}	-0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	± 20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 25 mA
Continuous current through V_{CC} or GND pins	± 50 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package	300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: D or N package	260°C
Storage temperature range	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54HC7266			SN74HC7266			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage		2	5	6	2	5	6	V
V _{IH}	High-level input voltage	V _{CC} = 2 V	1.5			1.5			V
		V _{CC} = 4.5 V	3.15			3.15			
		V _{CC} = 6 V	4.2			4.2			
V _{IL}	Low-level input voltage	V _{CC} = 2 V	0		0.3	0		0.3	V
		V _{CC} = 4.5 V	0		0.9	0		0.9	
		V _{CC} = 6 V	0		1.2	0		1.2	
V _I	Input voltage		0		V _{CC}	0		V _{CC}	V
V _O	Output voltage		0		V _{CC}	0		V _{CC}	V
t _t	Input transition (rise and fall) times	V _{CC} = 2 V	0		1000	0		1000	ns
		V _{CC} = 4.5 V	0		500	0		500	
		V _{CC} = 6 V	0		400	0		400	
T _A	Operating free-air temperature		-55		125	-40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25 °C			SN54HC7266		SN74HC7266		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	V _I = V _{IH} or V _{IL} , I _{OH} = -20 μA	2 V	1.9	1.998		1.9		1.9		V
		4.5 V	4.4	4.499		4.4		4.4		
		6 V	5.9	5.999		5.9		5.9		
	V _I = V _{IH} or V _{IL} , I _{OH} = -4 mA	4.5 V	3.98	4.30		3.7		3.84		
	V _I = V _{IH} or V _{IL} , I _{OH} = -5.2 mA	6 V	5.48	5.80		5.2		5.34		
V _{OL}	V _I = V _{IH} or V _{IL} , I _{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
		4.5 V		0.001	0.1		0.1		0.1	
		6 V		0.001	0.1		0.1		0.1	
	V _I = V _{IH} or V _{IL} , I _{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
	V _I = V _{IH} or V _{IL} , I _{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I _I	V _I = V _{CC} or 0	6 V	±0.1 ±100			±1000		±1000		nA
I _{CC}	V _I = V _{CC} or 0, I _O = 0	6 V	2			40		20		μA
C _i		2 to 6 V	3 10			10		10		pF

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switching characteristics over recommended operating free-air temperature range (unless otherwise noted), $C_L = 50$ pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	$T_A = 25^\circ\text{C}$			SN54HC7266		SN74HC7266		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	Y	2 V		40	100		150		125	ns
			4.5 V		12	20		30		25	
			6 V		10	17		25		21	
t_t		Y	2 V		28	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

C_{pd}	Power dissipation capacitance per gate	No load, $T_A = 25^\circ\text{C}$	35 pF typ
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NOTE 1: Load circuits and voltage waveforms are shown in Section 1.

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