

SN54AHCT245 SN74AHCT245 OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCLS233I – OCTOBER 1995 – REVISED JANUARY 2000

- **EPIC™ (Enhanced-Performance Implanted CMOS) Process**
- **Inputs Are TTL-Voltage Compatible**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), Thin Very Small-Outline (DGV), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) DIPs**

description

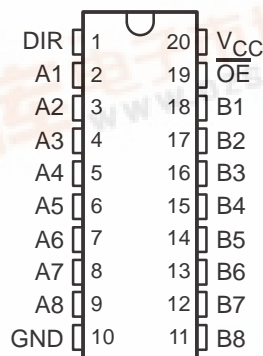
These octal bus transceivers are designed for asynchronous two-way communication between data buses. The control-function implementation minimizes external timing requirements.

The 'AHCT245 devices allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending upon the logic level at the direction-control (DIR) input. The output-enable (\overline{OE}) input can be used to disable the device so that the buses are effectively isolated.

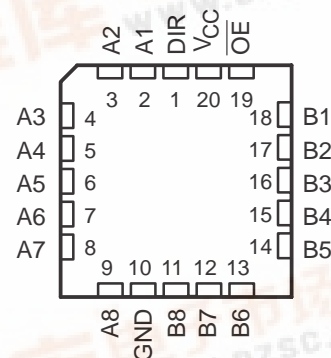
To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54AHCT245 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74AHCT245 is characterized for operation from -40°C to 85°C .

SN54AHCT245 . . . J OR W PACKAGE
SN74AHCT245 . . . DB, DGV, DW, N, OR PW PACKAGE
(TOP VIEW)



SN54AHCT245 . . . FK PACKAGE
(TOP VIEW)



FUNCTION TABLE
(each transceiver)

INPUTS		OPERATION
\overline{OE}	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

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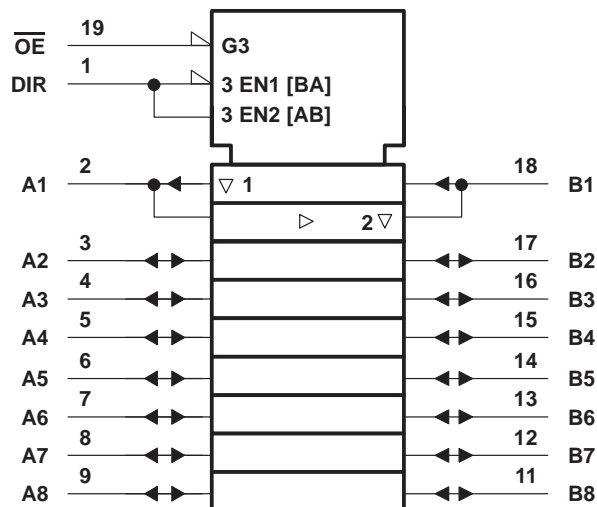
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OCTAL BUS TRANSCEIVERS

WITH 3-STATE OUTPUTS

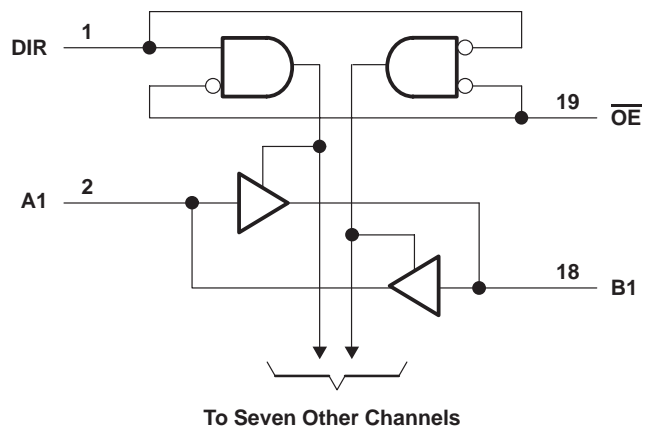
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



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Supply voltage range, V_{CC}	-0.5 V to 7 V
Input voltage range, V_I (see Note 1)	-0.5 V to 7 V
Output voltage range, V_O (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	-20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	± 20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 25 mA
Continuous current through V_{CC} or GND	± 75 mA
Package thermal impedance, θ_{JA} (see Note 2):		
DB package	70°C/W
DGV package	92°C/W
DW package	58°C/W
N package	69°C/W
PW package	83°C/W
Storage temperature range, T_{Stg}	-65°C to 150°C

NOTES:

1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51.

		SN54AHCT245		SN74AHCT245		UNIT
		MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V _{IH}	High-level input voltage	2		2		V
V _{IL}	Low-level input voltage		0.8		0.8	V
V _I	Input voltage	0	5.5	0	5.5	V
V _O	Output voltage	0	V _{CC}	0	V _{CC}	V
I _{OH}	High-level output current		−8		−8	mA
I _{OL}	Low-level output current		8		8	mA
Δt/Δv	Input transition rise or fall rate		20		20	ns/V
T _A	Operating free-air temperature	−55	125	−40	85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			SN54AHCT245		SN74AHCT245		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	I _{OH} = -50 µA	4.5 V	4.4	4.5		4.4		4.4		V
	I _{OH} = -8 mA		3.94			3.8		3.8		
V _{OL}	I _{OL} = 50 µA	4.5 V			0.1		0.1		0.1	V
	I _{OL} = 8 mA				0.36		0.44		0.44	
I _I	$\overline{\text{OE}}$ or DIR	V _I = V _{CC} or GND	0 V to 5.5 V			±0.1		±1*		µA
I _{OZ}	A or B inputs†	V _O = V _{CC} or GND	5.5 V			±0.25		±2.5		µA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V	4			40		40		µA
ΔI _{CC} ‡	One input at 3.4 V, Other inputs at V _{CC} or GND	5.5 V	1.35			1.5		1.5		mA
C _i	$\overline{\text{OE}}$ or DIR	V _I = V _{CC} or GND	5 V			2.5		10		pF
C _{io}	A or B inputs	V _I = V _{CC} or GND	5 V			4				pF

* On products compliant to MIL-PRF-38535, this parameter is not production tested at V_{CC} = 0 V.

† For I/O ports, the parameter I_{OZ} includes the input leakage current.

‡ This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C			SN54AHCT245		SN74AHCT245		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	A or B	B or A	C _L = 15 pF	4.5**	7.7**		1**	10**	1	8.5	ns
t _{PHL}				4.5**	7.7**		1**	10**	1	8.5	
t _{PZH}	$\overline{\text{OE}}$	A or B	C _L = 15 pF	8.9**	13.8**		1**	16**	1	15	ns
t _{PZL}				8.9**	13.8**		1**	16**	1	15	
t _{PHZ}	$\overline{\text{OE}}$	A or B	C _L = 15 pF	9.2**	14.4**		1**	16.5**	1	15.5	ns
t _{PLZ}				9.2**	14.4**		1**	16.5**	1	15.5	
t _{PLH}	A or B	B or A	C _L = 50 pF	5.3	8.7		1	11	1	9.5	ns
t _{PHL}				5.3	8.7		1	11	1	9.5	
t _{PZH}	$\overline{\text{OE}}$	A or B	C _L = 50 pF	9.7	14.8		1	17	1	16	ns
t _{PZL}				9.7	14.8		1	17	1	16	
t _{PHZ}	$\overline{\text{OE}}$	A or B	C _L = 50 pF	10	15.4		1	17.5	1	16.5	ns
t _{PLZ}				10	15.4		1	17.5	1	16.5	
t _{sk(o)}			C _L = 50 pF			1***				1	ns

** On products compliant to MIL-PRF-38535, this parameter is not production tested.

*** On products compliant to MIL-PRF-38535, this parameter does not apply.

noise characteristics, V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C (see Note 4)

PARAMETER	SN74AHCT245			UNIT
	MIN	TYP	MAX	
V _{OH(V)} Quiet output, minimum dynamic V _{OH}		4		V
V _{IH(D)} High-level dynamic input voltage	2			V
V _{IL(D)} Low-level dynamic input voltage			0.8	V

NOTE 4: Characteristics are for surface-mount packages only.

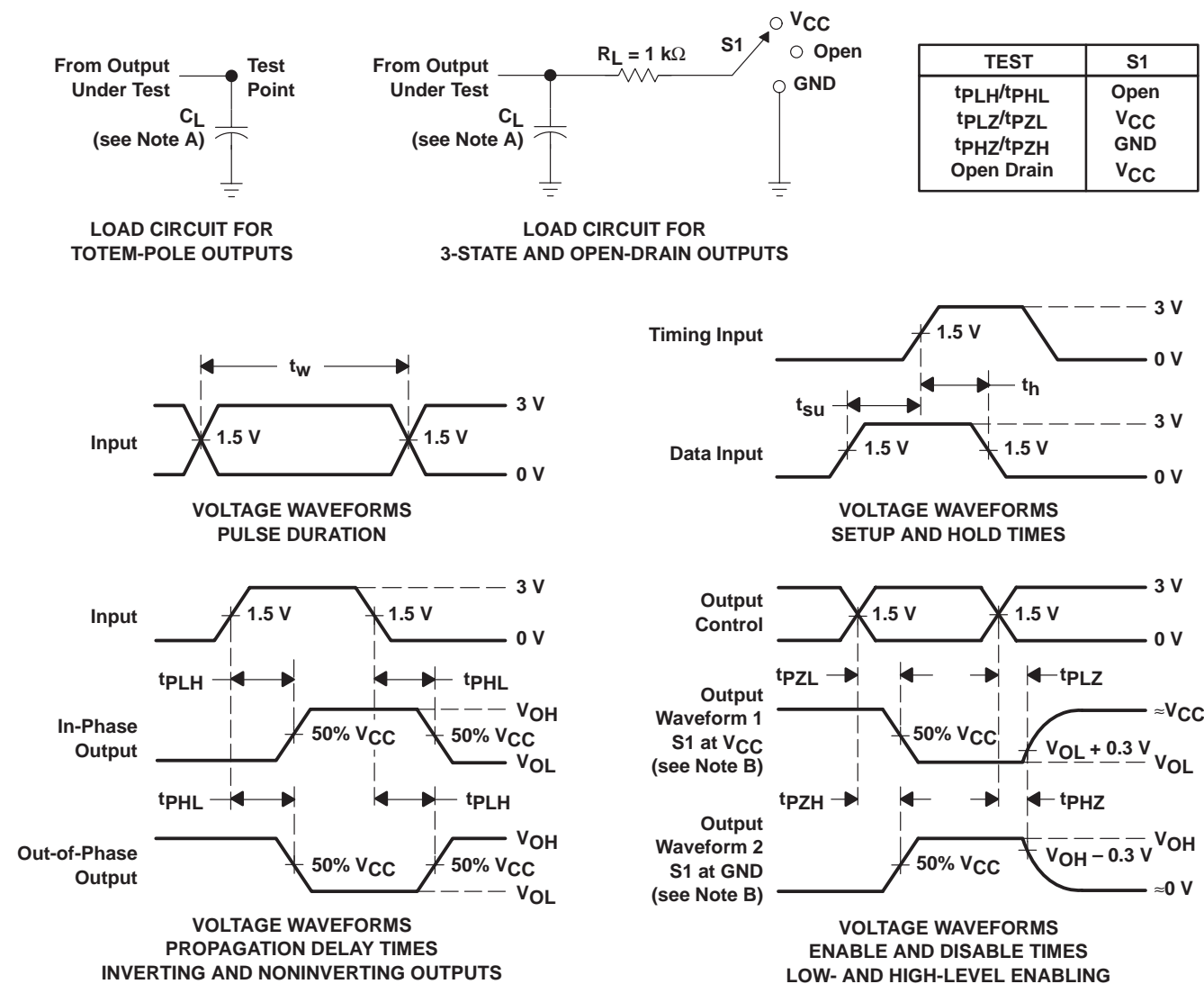
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operating characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
C_{pd} Power dissipation capacitance	No load, $f = 1\text{ MHz}$	13	pF

PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 3\text{ ns}$, $t_f \leq 3\text{ ns}$.
 - D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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