查询SN54AHCT14供应商

捷多邦,专业PCB打样SN54AH@顶4,出SN74AHCT14 HEX SCHMITT-TRIGGER INVERTERS

SCLS246M - OCTOBER 1995 - REVISED JANUARY 2000

- EPIC[™] (Enhanced-Performance Implanted CMOS) Process
- Inputs Are TTL-Voltage Compatible
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Very Small-Outline (DGV), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) DIPs

description

The 'AHCT14 devices contain six independent inverters. These devices perform the Boolean function $Y = \overline{A}$.

Each circuit functions as an independent inverter, but because of the Schmitt action, the inverters have different input threshold levels for positive-going (V_{T+}) and for negative-going (V_{T-}) signals.

The SN54AHCT14 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74AHCT14 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE (each inverter)									
INPUT A	OUTPUT Y								
Н	L								
L	н								

	A		
	Λ	Λ	
-	1 mail		

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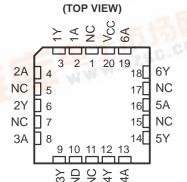


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SN54AHCT14 ... J OR W PACKAGE SN74AHCT14 ... D, DB, DGV, N, OR PW PACKAGE (TOP VIEW)

_				_
1A 🛛		~	14	Vcc
1Y [2		13	V _{CC} 6A
2A [12	6Y
2Y [4		11	5A
3A [5		10	5Y
3Y [6] 4A
gnd [7		8] 4Y

SN54AHCT14 ... FK PACKAGE

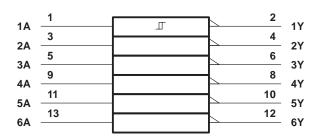


NC – No internal connection

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logic symbol[†]



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the D, DB, DGV, J, N, PW, and W packages.

logic diagram, each inverter (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[‡]

PW package 113°C/W
Storage temperature range, T _{stg}

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 3)

		SN54A	HCT14	SN74A	UNIT	
		MIN	MAX	MIN	MAX	UNIT
VCC	Supply voltage	4.5	5.5	4.5	5.5	V
VI	Input voltage	0	5.5	0	5.5	V
Vo	Output voltage	0	VCC	0	VCC	V
IOH	High-level output current		-8		-8	mA
IOL	Low-level output current		8		8	mA
Т _А	Operating free-air temperature	-55	125	-40	85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	Vaa	T _A = 25°C			SN54AHCT14		SN74AHCT14		UNIT
PARAMETER	TEST CONDITIONS	Vcc	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
V _{T+}		4.5 V	0.9		1.9	0.9	1.9	0.9	1.9	V
Positive-going input threshold voltage		5.5 V	1		2.1	1	2.1	1	2.1	V
V _T -		4.5 V	0.5		1.5	0.5	1.5	0.5	1.5	V
Negative-going input threshold voltage		5.5 V	0.6		1.7	0.6	1.7	0.6	1.7	v
ΔV _T		4.5 V	0.4		1.4	0.4	1.4	0.4	1.4	V
Hysteresis (V _{T+} – V _{T–})		5.5 V	0.4		1.5	0.4	1.5	0.4	1.5	v
Vou	I _{OH} = -50 μA	4.5 V	4.4	4.5		4.4		4.4		V
Vон	I _{OH} = -8 mA	4.5 V	3.94			3.8		3.8		V
Ver	I _{OL} = 50 μA	4.5 V			0.1		0.1		0.1	V
VOL	I _{OL} = 8 mA	4.5 V			0.36		0.44		0.44	v
lj	$V_{I} = V_{CC} \text{ or } GND$	0 V to 5.5 V			±0.1		±1*		±1	μA
ICC	$V_{I} = V_{CC} \text{ or } GND, \qquad I_{O} = 0$	5.5 V			2		20		20	μA
ΔI_{CC}^{\dagger}	One input at 3.4 V, Other inputs at V _{CC} or GND	5.5 V			1.35		1.5		1.5	mA
Ci	V _I = V _{CC} or GND	5 V		2	10				10	pF

* On products compliant to MIL-PRF-38535, this parameter is not production tested at $V_{CC} = 0 V$.

[†] This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

switching characteristics over recommended operating free-air temperature range V_{CC} = 5 V \pm 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM	то	LOAD	Т	_ = 25°C	;	SN54AI	HCT14	SN74A	HCT14	UNIT
PARAMETER	(INPUT)	(OUTPUT)	CAPACITANCE	MIN	TYP	MAX	MIN	MAX	MIN	MAX	
^t PLH	۵	V	C: 45 pF		4**	7**	1**	8**	1	8	
^t PHL	A	Ť	C _L = 15 pF		4**	7**	1**	8**	1	8	ns
^t PLH	٨	v	$C_{\rm L} = 50 \rm pE$		5.5	8	1	9	1	9	20
^t PHL	A	T	C _L = 50 pF		5.5	8	1	9	1	9	ns

** On products compliant to MIL-PRF-38535, this parameter is not production tested.

noise characteristics, V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C (see Note 4)

	PARAMETER	SN7	UNIT		
	FARAINETER	MIN			UNIT
VOL(P)	Quiet output, maximum dynamic V _{OL}		0.9		V
VOL(V)	Quiet output, minimum dynamic V _{OL}		-0.7		V
VOH(V)	Quiet output, minimum dynamic V _{OH}	4.3		V	
V _{IH(D)}	High-level dynamic input voltage	2.1			V
V _{IL(D)}	Low-level dynamic input voltage			0.5	V

NOTE 4: Characteristics are for surface-mount packages only.

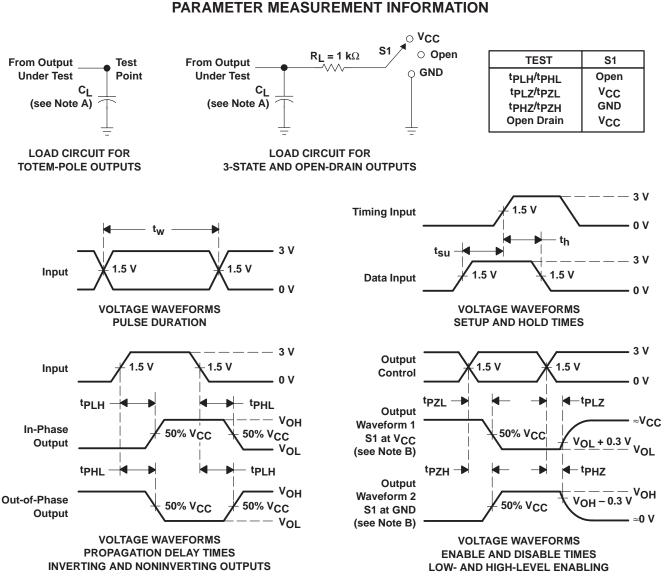
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS	TYP	UNIT
C _{pd} Power dissipation capacitance	No load, f = 1 MHz	12	pF



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NOTES: A. CL includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

C. All input pulses are supplied by generators having the following characteristics: $PRR \le 1$ MHz, $Z_{O} = 50 \Omega$, $t_{f} \le 3$ ns, $t_{f} \le 3$ ns.

D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms



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