

SN54AHCT132 SN74AHCT132 QUADRUPLE POSITIVE-NAND GATES WITH SCHMITT-TRIGGER INPUTS

SCLS366F – MAY 1997 – REVISED JANUARY 2000

- **EPIC™** (Enhanced-Performance Implanted CMOS) Process
- Inputs Are TTL-Voltage Compatible
- Operation From Very Slow Input Transitions
- Temperature-Compensated Threshold Levels
- High Noise Immunity
- Same Pinouts as 'AHCT00
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Very Small-Outline (DGV), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) DIPs

description

The 'AHCT132 devices are quadruple positive-NAND gates.

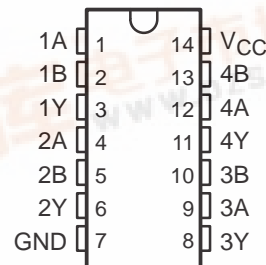
These devices perform the Boolean function $Y = \overline{A \bullet B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

Each circuit functions as a NAND gate, but because of the Schmitt action, it has different input threshold levels for positive- and negative-going signals.

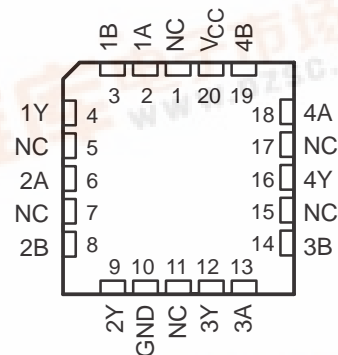
These circuits are temperature compensated and can be triggered from the slowest of input ramps and still give clean jitter-free output signals.

The SN54AHCT132 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74AHCT132 is characterized for operation from -40°C to 85°C .

SN54AHCT132 ... J OR W PACKAGE
SN74AHCT132 ... D, DB, DGV, N, OR PW PACKAGE
(TOP VIEW)



SN54AHCT132 ... FK PACKAGE
(TOP VIEW)



NC – No internal connection

FUNCTION TABLE
(each gate)

INPUTS		OUTPUT Y
A	B	
H	H	L
L	X	H
X	L	H

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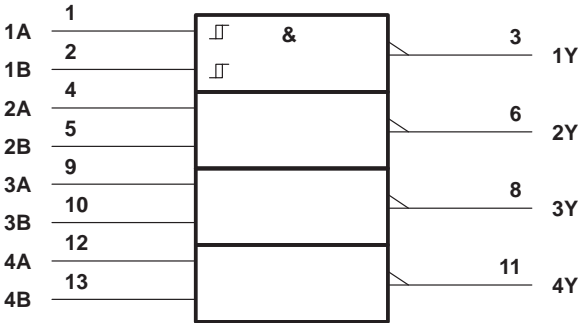
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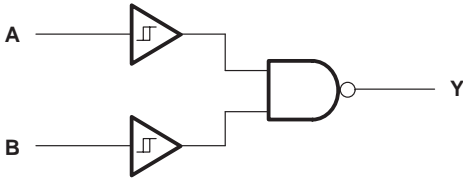
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
 Pin numbers shown are for the D, DB, DGV, J, N, PW, and W packages.

logic diagram, each gate (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Output voltage range, V_O (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±25 mA
Continuous current through V_{CC} or GND	±50 mA
Package thermal impedance, θ_{JA} (see Note 2):	
D package	86°C/W
DB package	96°C/W
DGV package	127°C/W
N package	80°C/W
PW package	113°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
 2. The package thermal impedance is calculated in accordance with JESD 51.

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recommended operating conditions (see Note 3)

		SN54AHCT132		SN74AHCT132		UNIT
		MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V _I	Input voltage	0	5.5	0	5.5	V
V _O	Output voltage	0	V _{CC}	0	V _{CC}	V
I _{OH}	High-level output current		–8		–8	mA
I _{OL}	Low-level output current		8		8	mA
T _A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			SN54AHCT132		SN74AHCT132		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{T+} Positive-going input threshold voltage		4.5 V	0.9		1.9	0.9	1.9	0.9	1.9	V
		5.5 V	1		2.1	1	2.1	1	2.1	
V _{T–} Negative-going input threshold voltage		4.5 V	0.5		1.5	0.5	1.5	0.5	1.5	V
		5.5 V	0.6		1.7	0.6	1.7	0.6	1.7	
ΔV _T Hysteresis (V _{T+} – V _{T–})		4.5 V	0.3		1.4	0.3	1.4	0.3	1.4	V
		5.5 V	0.3		1.5	0.3	1.5	0.3	1.5	
V _{OH}	I _{OH} = –50 μA	4.5 V	4.4	4.5		4.4		4.4		V
	I _{OH} = –8 mA		3.94			3.8		3.8		
V _{OL}	I _{OL} = 50 μA	4.5 V			0.1		0.1		0.1	V
	I _{OL} = 8 mA				0.36		0.5		0.44	
I _I	V _I = V _{CC} or GND	0 V to 5.5 V			±0.1		±1*		±1	μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V			2		20		20	μA
ΔI _{CC} †	One input at 3.4 V, Other inputs at V _{CC} or GND	5.5 V			1.35		1.5		1.5	mA
C _i	V _I = V _{CC} or GND	5 V		2	10				10	pF

* On products compliant to MIL-PRF-38535, this parameter is not production tested at V_{CC} = 0 V.

† This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

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switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54AHCT132		SN74AHCT132		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	$C_L = 15\text{ pF}$		5.5*	8*	1*	9*	1	9	ns
t_{PHL}					4.5*	6*	1*	7*	1	7	
t_{PLH}	A or B	Y	$C_L = 50\text{ pF}$		6.5	9	1	10	1	10	ns
t_{PHL}					5.5	7	1	8	1	8	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

noise characteristics, $V_{CC} = 5\text{ V}$, $C_L = 50\text{ pF}$, $T_A = 25^\circ\text{C}$ (see Note 4)

PARAMETER		SN74AHCT132			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.5	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		-0.28	-0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		5		V
$V_{IH(D)}$	High-level dynamic input voltage		2		V
$V_{IL(D)}$	Low-level dynamic input voltage			0.8	V

NOTE 4: Characteristics are for surface-mount packages only.

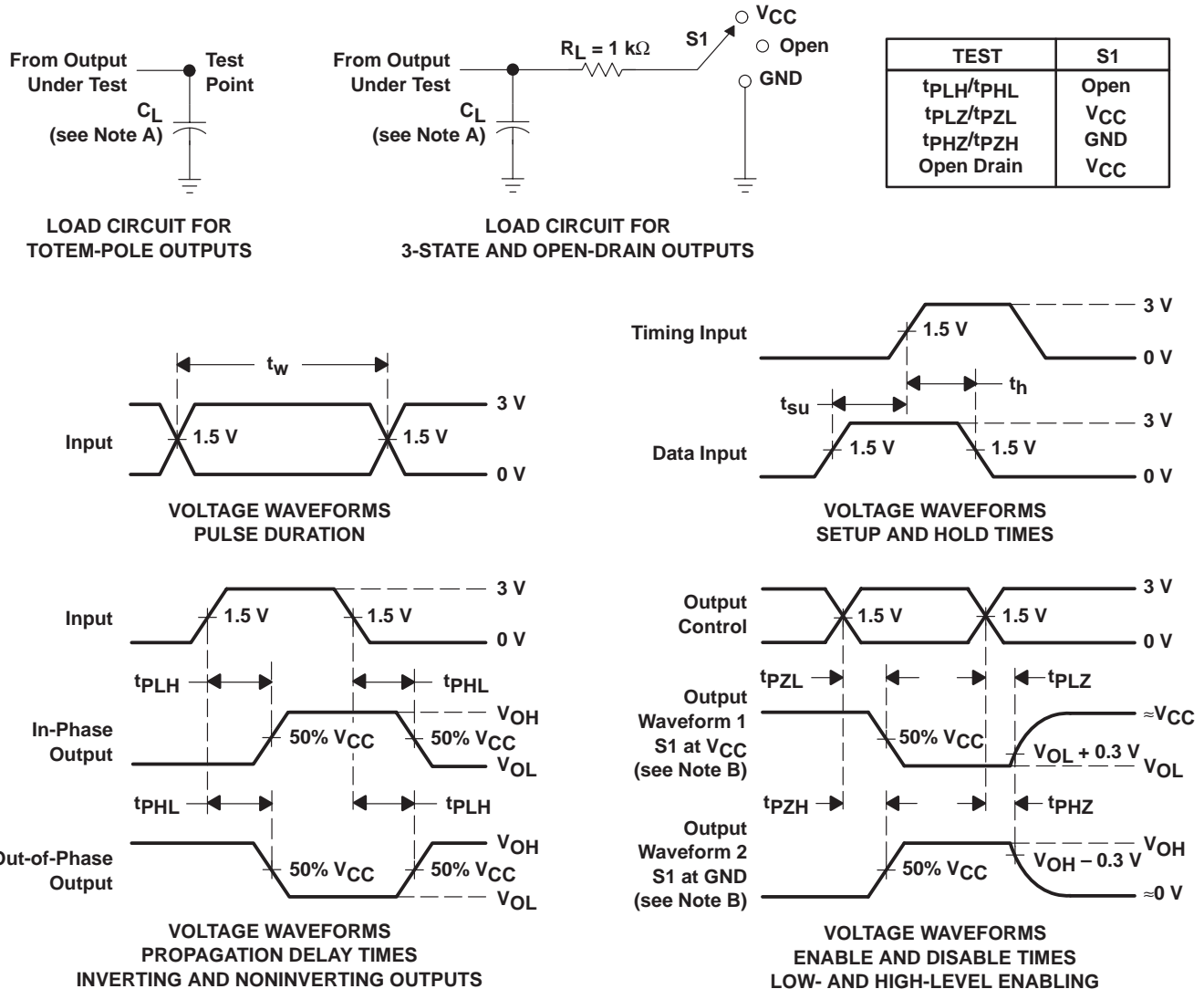
operating characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load, $f = 1\text{ MHz}$	15	pF

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PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 3\text{ ns}$, $t_f \leq 3\text{ ns}$.
 - D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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