

# SN54LV244A, SN74LV244A OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SCLS383C – SEPTEMBER 1997 – REVISED MAY 2000

- **EPIC™** (Enhanced-Performance Implanted CMOS) Process
- Typical  $V_{OLP}$  (Output Ground Bounce)  $<0.8$  V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- Typical  $V_{OHV}$  (Output  $V_{OH}$  Undershoot)  $>2.3$  V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- 2-V to 5.5-V  $V_{CC}$  Operation
- Support Mixed-Mode Voltage Operation on All Ports
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ( $C = 200$  pF,  $R = 0$ )
- Package Options Include Plastic Small-Outline (DW, NS), Shrink Small-Outline (DB), Thin Very Small-Outline (DGV), and Thin Shrink Small-Outline (PW) Packages, Ceramic Flat (W) Packages, Chip Carriers (FK), and DIPs (J)

## description

These octal buffers/line drivers are designed for 2-V to 5.5-V  $V_{CC}$  operation.

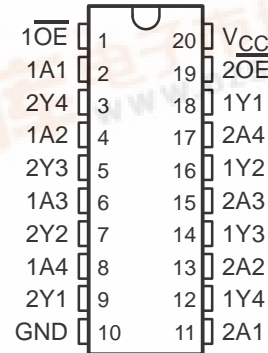
The 'LV244A devices are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

These devices are organized as two 4-bit line drivers with separate output-enable ( $\overline{OE}$ ) inputs. When  $\overline{OE}$  is low, the device passes data from the A inputs to the Y outputs. When  $\overline{OE}$  is high, the outputs are in the high-impedance state.

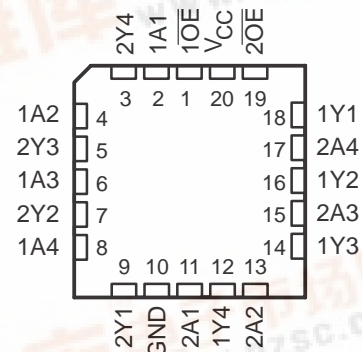
To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54LV244A is characterized for operation over the full military temperature range of  $-55^\circ\text{C}$  to  $125^\circ\text{C}$ . The SN74LV244A is characterized for operation from  $-40^\circ\text{C}$  to  $85^\circ\text{C}$ .

SN54LV244A ... J OR W PACKAGE  
SN74LV244A ... DB, DGV, DW, NS, OR PW PACKAGE  
(TOP VIEW)



SN54LV244A ... FK PACKAGE  
(TOP VIEW)



FUNCTION TABLE  
(each buffer)

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

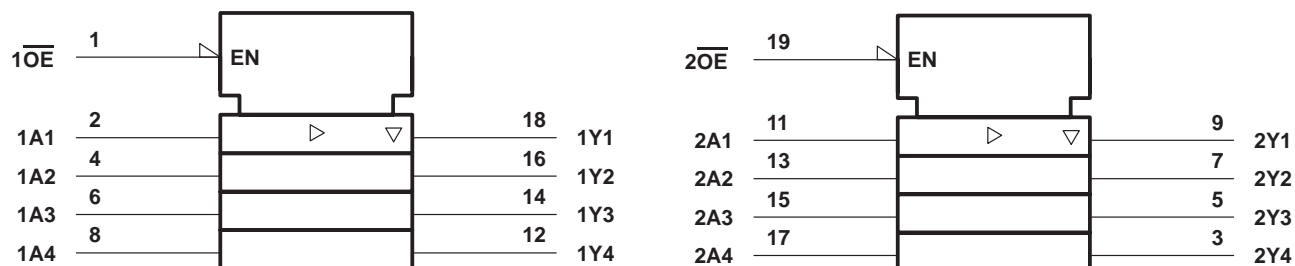
EPIC is a trademark of Texas Instruments.

UNLESS OTHERWISE NOTED this document contains PRODUCTION DATA information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

# SN54LV244A, SN74LV244A OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

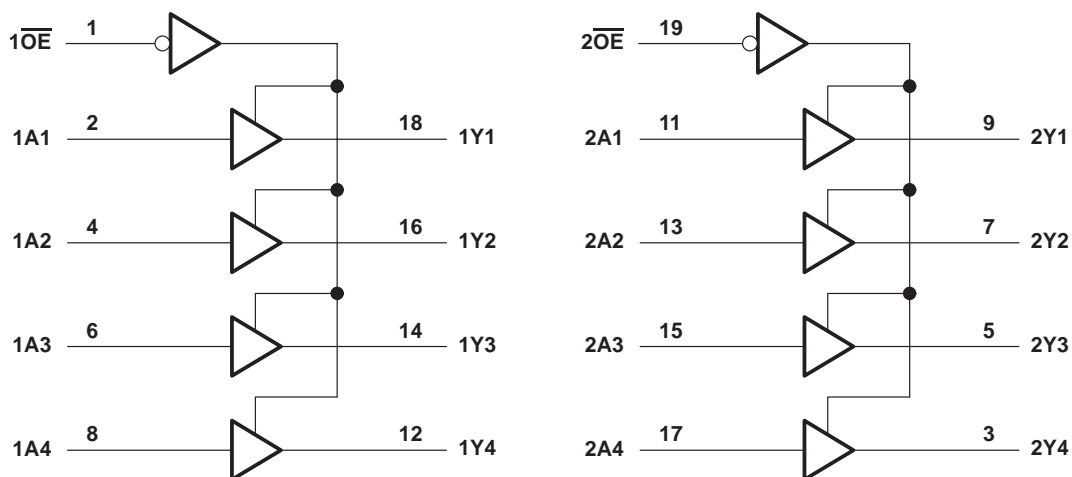
SCLS383C – SEPTEMBER 1997 – REVISED MAY 2000

## logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)



## SCLS383C – SEPTEMBER 1997 – REVISED MAY 2000

# SN54LV244A, SN74LV244A

## OCTAL BUFFERS/DRIVERS

### WITH 3-STATE OUTPUTS

SCLS383C – SEPTEMBER 1997 – REVISED MAY 2000

#### recommended operating conditions (see Note 4)

			SN54LV244A		SN74LV244A		UNIT
			MIN	MAX	MIN	MAX	
V <sub>CC</sub>	Supply voltage		2	5.5	2	5.5	V
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 2 V	1.5		1.5		V
		V <sub>CC</sub> = 2.3 V to 2.7 V	V <sub>CC</sub> × 0.7		V <sub>CC</sub> × 0.7		
		V <sub>CC</sub> = 3 V to 3.6 V	V <sub>CC</sub> × 0.7		V <sub>CC</sub> × 0.7		
		V <sub>CC</sub> = 4.5 V to 5.5 V	V <sub>CC</sub> × 0.7		V <sub>CC</sub> × 0.7		
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 2 V	0.5		0.5		V
		V <sub>CC</sub> = 2.3 V to 2.7 V	V <sub>CC</sub> × 0.3		V <sub>CC</sub> × 0.3		
		V <sub>CC</sub> = 3 V to 3.6 V	V <sub>CC</sub> × 0.3		V <sub>CC</sub> × 0.3		
		V <sub>CC</sub> = 4.5 V to 5.5 V	V <sub>CC</sub> × 0.3		V <sub>CC</sub> × 0.3		
V <sub>I</sub>	Input voltage		0	5.5	0	5.5	V
V <sub>O</sub>	Output voltage	High or low state	0	V <sub>CC</sub>	0	V <sub>CC</sub>	V
		3-state	0	5.5	0	5.5	
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 2 V	−50		−50		μA
		V <sub>CC</sub> = 2.3 V to 2.7 V	−2		−2		mA
		V <sub>CC</sub> = 3 V to 3.6 V	−8		−8		
		V <sub>CC</sub> = 4.5 V to 5.5 V	−16		−16		
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 2 V	50		50		μA
		V <sub>CC</sub> = 2.3 V to 2.7 V	2		2		mA
		V <sub>CC</sub> = 3 V to 3.6 V	8		8		
		V <sub>CC</sub> = 4.5 V to 5.5 V	16		16		
Δt/Δv	Input transition rise or fall rate	V <sub>CC</sub> = 2.3 V to 2.7 V	0	200	0	200	ns/V
		V <sub>CC</sub> = 3 V to 3.6 V	0	100	0	100	
		V <sub>CC</sub> = 4.5 V to 5.5 V	0	20	0	20	
T <sub>A</sub>	Operating free-air temperature		−55	125	−40	85	°C

NOTE 4: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

# SN54LV244A, SN74LV244A OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SCLS383C – SEPTEMBER 1997 – REVISED MAY 2000

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	SN54LV244A			SN74LV244A			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V <sub>OH</sub>	I <sub>OH</sub> = -50 μA	2 V to 5.5 V	V <sub>CC</sub> -0.1			V <sub>CC</sub> -0.1			V
	I <sub>OH</sub> = -2 mA	2.3 V	2			2			
	I <sub>OH</sub> = -8 mA	3 V	2.48			2.48			
	I <sub>OH</sub> = -16 mA	4.5 V	3.8			3.8			
V <sub>OL</sub>	I <sub>OL</sub> = 50 μA	2 V to 5.5 V	0.1			0.1			V
	I <sub>OL</sub> = 2 mA	2.3 V	0.4			0.4			
	I <sub>OL</sub> = 8 mA	3 V	0.44			0.44			
	I <sub>OL</sub> = 16 mA	4.5 V	0.55			0.55			
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	0 V to 5.5 V	±1			±1			μA
I <sub>OZ</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	5.5 V	±5			±5			μA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V	20			20			μA
I <sub>off</sub>	V <sub>I</sub> or V <sub>O</sub> = 0 to 5.5 V	0 V	5			5			μA
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	3.3 V	2.3			2.3			pF

**switching characteristics over recommended operating free-air temperature range, V<sub>CC</sub> = 2.5 V ± 0.2 V (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T <sub>A</sub> = 25°C			SN54LV244A		SN74LV244A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t <sub>pd</sub>	A	Y	C <sub>L</sub> = 15 pF	7.5*	12.5*	1*	15*	1	15	ns	
t <sub>en</sub>	$\overline{\text{OE}}$	Y		8.9*	14.6*	1*	17*	1	17		
t <sub>dis</sub>	$\overline{\text{OE}}$	Y		9.1*	14.1*	1*	16*	1	16		
t <sub>pd</sub>	A	Y	C <sub>L</sub> = 50 pF	9.5	15.3	1	18	1	18	ns	
t <sub>en</sub>	$\overline{\text{OE}}$	Y		10.8	17.8	1	21	1	21		
t <sub>dis</sub>	$\overline{\text{OE}}$	Y		13.4	19.2	1	21	1	21		
t <sub>sk(o)</sub>				2					2		

\* On products compliant to MIL-PRF-38535, this parameter is not production tested.

**switching characteristics over recommended operating free-air temperature range, V<sub>CC</sub> = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T <sub>A</sub> = 25°C			SN54LV244A		SN74LV244A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t <sub>pd</sub>	A	Y	C <sub>L</sub> = 15 pF		5.4*	8.4*	1*	10*	1	10	ns
t <sub>en</sub>	$\overline{\text{OE}}$	Y			6.3*	10.6*	1*	12.5*	1	12.5	
t <sub>dis</sub>	$\overline{\text{OE}}$	Y			7.6*	11.7*	1*	13*	1	13	
t <sub>pd</sub>	A	Y	C <sub>L</sub> = 50 pF		6.8	11.9	1	13.5	1	13.5	ns
t <sub>en</sub>	$\overline{\text{OE}}$	Y			7.8	14.1	1	16	1	16	
t <sub>dis</sub>	$\overline{\text{OE}}$	Y			11	16	1	18	1	18	
t <sub>sk(o)</sub>						1.5				1.5	

\* On products compliant to MIL-PRF-38535, this parameter is not production tested.

# SN54LV244A, SN74LV244A

## OCTAL BUFFERS/DRIVERS

### WITH 3-STATE OUTPUTS

SCLS383C – SEPTEMBER 1997 – REVISED MAY 2000

switching characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LV244A		SN74LV244A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$t_{pd}$	A	Y	$C_L = 15\text{ pF}$	3.9*	5.5*		1*	6.5*	1	6.5	ns
$t_{en}$	$\overline{OE}$	Y		4.5*	7.3*		1*	8.5*	1	8.5	
$t_{dis}$	$\overline{OE}$	Y		6.5*	12.2*		1*	13.5*	1	13.5	
$t_{pd}$	A	Y	$C_L = 50\text{ pF}$	4.9	7.5		1	8.5	1	8.5	ns
$t_{en}$	$\overline{OE}$	Y		5.6	9.3		1	10.5	1	10.5	
$t_{dis}$	$\overline{OE}$	Y		8.8	14.2		1	15.5	1	15.5	
$t_{sk(o)}$					1					1	

\* On products compliant to MIL-PRF-38535, this parameter is not production tested.

noise characteristics,  $V_{CC} = 3.3\text{ V}$ ,  $C_L = 50\text{ pF}$ ,  $T_A = 25^\circ\text{C}$  (see Note 5)

PARAMETER		SN74LV244A			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic $V_{OL}$		0.55		V
$V_{OL(V)}$	Quiet output, minimum dynamic $V_{OL}$		−0.5		V
$V_{OH(V)}$	Quiet output, minimum dynamic $V_{OH}$		2.9		V
$V_{IH(D)}$	High-level dynamic input voltage		2.31		V
$V_{IL(D)}$	Low-level dynamic input voltage			0.99	V

NOTE 5: Characteristics are for surface-mount packages only.

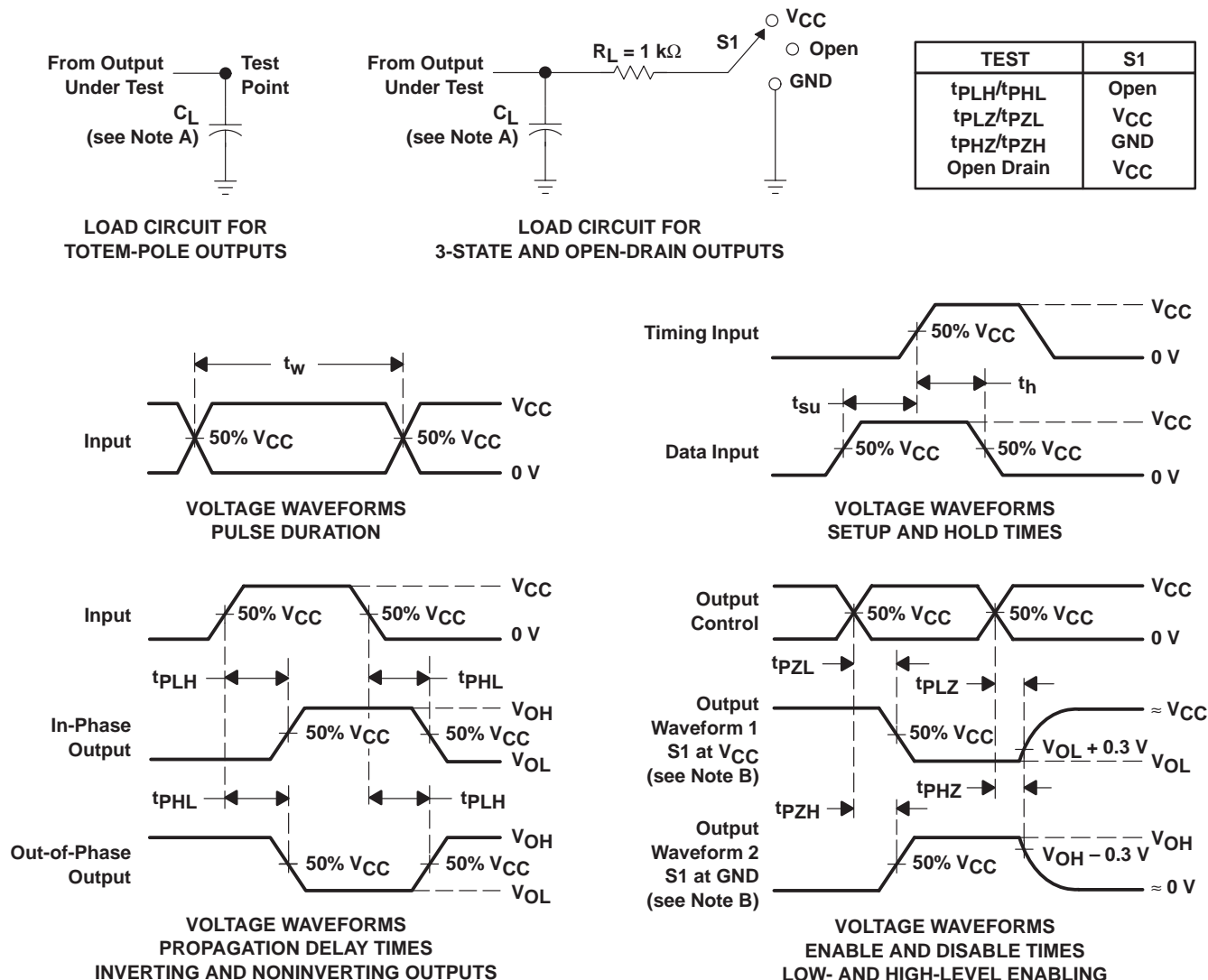
operating characteristics,  $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	$V_{CC}$	TYP	UNIT
$C_{pd}$	Power dissipation capacitance	$C_L = 50\text{ pF}$ , $f = 10\text{ MHz}$	3.3 V	14	pF
			5 V	16	

# SN54LV244A, SN74LV244A OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SCLS383C – SEPTEMBER 1997 – REVISED MAY 2000

## PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 3\text{ ns}$ ,  $t_f \leq 3\text{ ns}$ .
  - D. The outputs are measured one at a time with one input transition per measurement.
  - E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - G.  $t_{PHL}$  and  $t_{PLH}$  are the same as  $t_{pd}$ .

Figure 1. Load Circuit and Voltage Waveforms

## **IMPORTANT NOTICE**

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgment, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Customers are responsible for their applications using TI components.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.