

- **EPIC™ (Enhanced-Performance Implanted CMOS) Process**
- **Typical V_{OLP} (Output Ground Bounce) $<0.8\text{ V}$ at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$**
- **Typical V_{OHV} (Output V_{OH} Undershoot) $>2.3\text{ V}$ at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$**
- **2-V to 5.5-V V_{CC} Operation**
- **Support Mixed-Mode Voltage Operation on All Ports**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ($C = 200\text{ pF}$, $R = 0$)**
- **Package Options Include Plastic Small-Outline (D, NS), Shrink Small-Outline (DB), Thin Very Small-Outline (DGV), and Thin Shrink Small-Outline (PW) Packages, Ceramic Flat (W) Packages, Chip Carriers (FK), and DIPs (J)**

description

These quadruple 2-input positive-OR gates are designed for 2-V to 5.5-V V_{CC} operation.

The 'LV32A devices perform the Boolean function $Y = A + B$ or $Y = \overline{A} \bullet \overline{B}$ in positive logic.

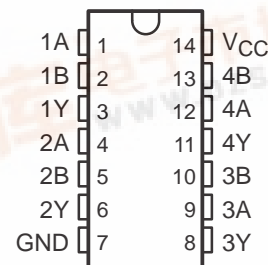
The SN54LV32A is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LV32A is characterized for operation from -40°C to 85°C .

FUNCTION TABLE
(each gate)

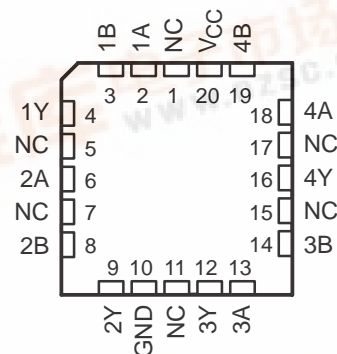
INPUTS		OUTPUT Y
A	B	
H	X	H
X	H	H
L	L	L

SN54LV32A . . . J OR W PACKAGE

SN74LV32A . . . D, DB, DGV, NS, OR PW PACKAGE
(TOP VIEW)



**SN54LV32A . . . FK PACKAGE
(TOP VIEW)**



NC – No internal connection



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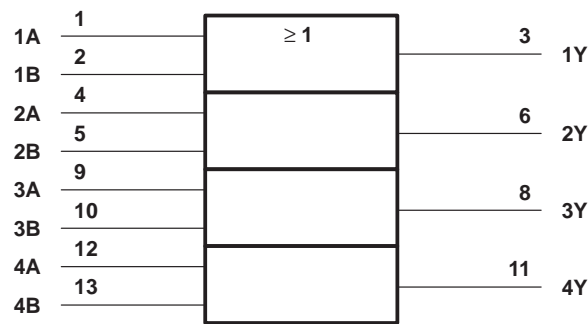
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SN54LV32A, SN74LV32A

QUADRUPLE 2-INPUT POSITIVE-OR GATES

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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, DGV, J, NS, PW, and W packages.

logic diagram, each gate (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	–0.5 V to 7 V
Output voltage range, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±25 mA
Continuous current through V_{CC} or GND	±50 mA
Package thermal impedance, θ_{JA} (see Note 3):	
D package	86°C/W
DB package	96°C/W
DGV package	127°C/W
N package	80°C/W
PW package	113°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
 2. This value is limited to 5.5 V maximum.
 3. The package thermal impedance is calculated in accordance with JESD 51.

SN54LV32A, SN74LV32A QUADRUPLE 2-INPUT POSITIVE-OR GATES

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recommended operating conditions (see Note 4)

			SN54LV32A		SN74LV32A		UNIT
			MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage		2	5.5	2	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 2 V	1.5		1.5		V
		V _{CC} = 2.3 V to 2.7 V	V _{CC} × 0.7		V _{CC} × 0.7		
		V _{CC} = 3 V to 3.6 V	V _{CC} × 0.7		V _{CC} × 0.7		
		V _{CC} = 4.5 V to 5.5 V	V _{CC} × 0.7		V _{CC} × 0.7		
V _{IL}	Low-level input voltage	V _{CC} = 2 V		0.5		0.5	V
		V _{CC} = 2.3 V to 2.7 V		V _{CC} × 0.3		V _{CC} × 0.3	
		V _{CC} = 3 V to 3.6 V		V _{CC} × 0.3		V _{CC} × 0.3	
		V _{CC} = 4.5 V to 5.5 V		V _{CC} × 0.3		V _{CC} × 0.3	
V _I	Input voltage		0	5.5	0	5.5	V
V _O	Output voltage		0	V _{CC}	0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 2 V		–50		–50	μA
		V _{CC} = 2.3 V to 2.7 V		–2		–2	
		V _{CC} = 3 V to 3.6 V		–6		–6	
		V _{CC} = 4.5 V to 5.5 V		–12		–12	
I _{OL}	Low-level output current	V _{CC} = 2 V		50		50	μA
		V _{CC} = 2.3 V to 2.7 V		2		2	
		V _{CC} = 3 V to 3.6 V		6		6	
		V _{CC} = 4.5 V to 5.5 V		12		12	
Δt/Δv	Input transition rise or fall rate	V _{CC} = 2.3 V to 2.7 V	0	200	0	200	ns/V
		V _{CC} = 3 V to 3.6 V	0	100	0	100	
		V _{CC} = 4.5 V to 5.5 V	0	20	0	20	
T _A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	SN54LV32A			SN74LV32A			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V _{OH}	I _{OH} = –50 μA	2 V to 5.5 V	V _{CC} –0.1			V _{CC} –0.1			V
	I _{OH} = –2 mA	2.3 V	2			2			
	I _{OH} = –6 mA	3 V	2.48			2.48			
	I _{OH} = –12 mA	4.5 V	3.8			3.8			
V _{OL}	I _{OL} = 50 μA	2 V to 5.5 V			0.1			0.1	V
	I _{OL} = 2 mA	2.3 V			0.4			0.4	
	I _{OL} = 6 mA	3 V			0.44			0.44	
	I _{OL} = 12 mA	4.5 V			0.55			0.55	
I _I	V _I = V _{CC} or GND	0 V to 5.5 V			±1			±1	μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V			20			20	μA
I _{off}	V _I or V _O = 0 to 5.5 V	0 V			5			5	μA
C _i	V _I = V _{CC} or GND	3.3 V		3.3			3.3		pF
		5 V		3.3			3.3		

SN54LV32A, SN74LV32A

QUADRUPLE 2-INPUT POSITIVE-OR GATES

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**switching characteristics over recommended operating free-air temperature range,
V_{CC} = 2.5 V ± 0.2 V (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C			SN54LV32A		SN74LV32A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A or B	Y	C _L = 15 pF		7.1*	12.8*	1*	16*	1	15	ns
t _{pd}	A or B	Y	C _L = 50 pF		9.6	16.2	1	20	1	19	ns

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

**switching characteristics over recommended operating free-air temperature range,
V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C			SN54LV32A		SN74LV32A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A or B	Y	C _L = 15 pF		5*	7.9*	1*	9.5*	1	9.5	ns
t _{pd}	A or B	Y	C _L = 50 pF		6.9	11.4	1	13	1	13	ns

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

**switching characteristics over recommended operating free-air temperature range,
V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C			SN54LV32A		SN74LV32A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A or B	Y	C _L = 15 pF		3.6*	5.5*	1*	6.5*	1	6.5	ns
t _{pd}	A or B	Y	C _L = 50 pF		4.9	7.5	1	8.5	1	8.5	ns

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

noise characteristics, V_{CC} = 3.3 V, C_L = 50 pF, T_A = 25°C (see Note 5)

PARAMETER				SN74LV32A			UNIT
				MIN	TYP	MAX	
V _{OL(P)}	Quiet output, maximum dynamic V _{OL}				0.2	0.8	V
V _{OL(V)}	Quiet output, minimum dynamic V _{OL}				−0.1	−0.8	V
V _{OH(V)}	Quiet output, minimum dynamic V _{OH}				3.1		V
V _{IH(D)}	High-level dynamic input voltage				2.31		V
V _{IL(D)}	Low-level dynamic input voltage					0.99	V

NOTE 5: Characteristics are for surface-mount packages only.

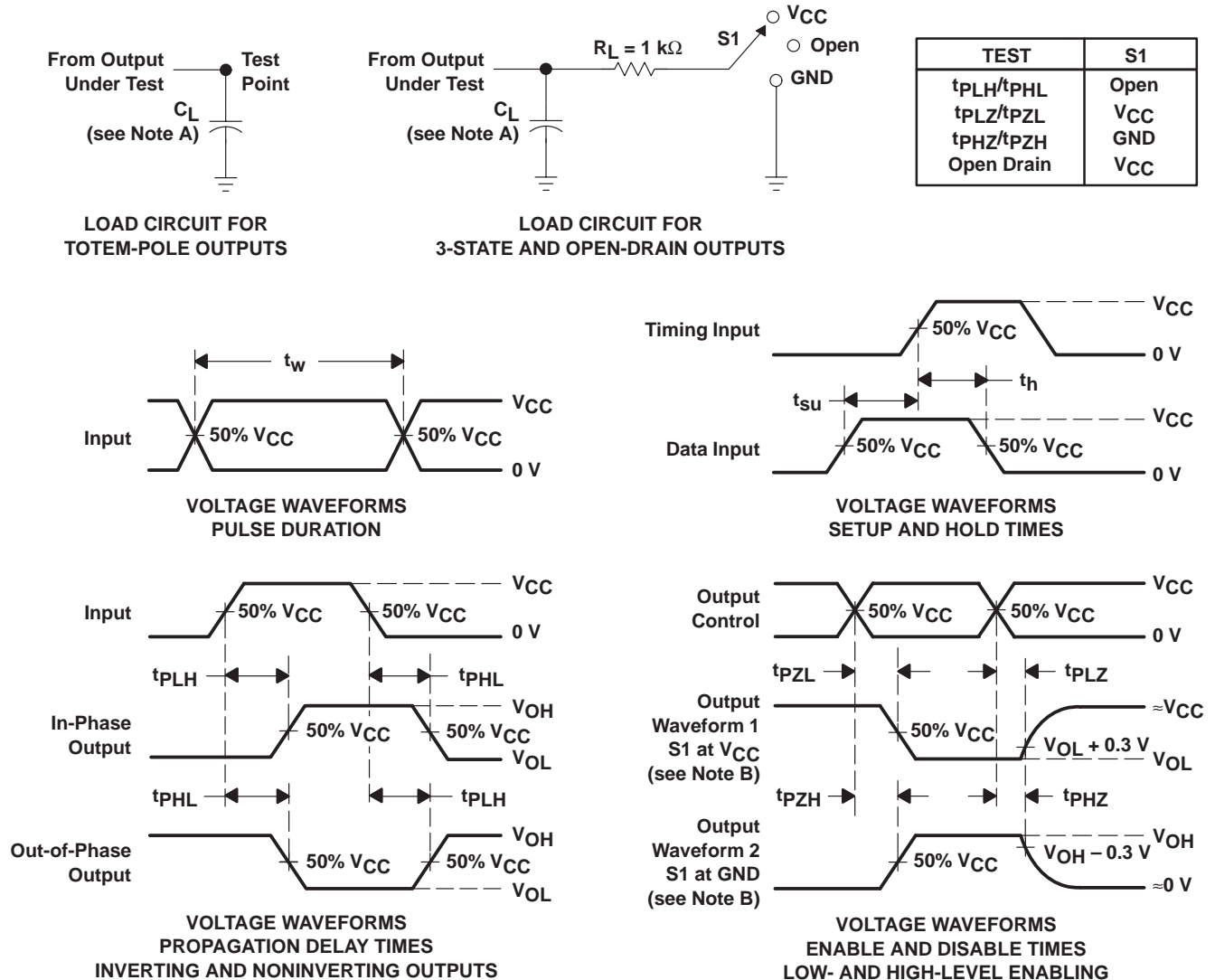
operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS		V _{CC}	TYP	UNIT
C _{pd}	Power dissipation capacitance	C _L = 50 pF, f = 10 MHz		3.3 V	9.5	pF
				5 V	11.5	

SN54LV32A, SN74LV32A QUADRUPLE 2-INPUT POSITIVE-OR GATES

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PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 3\text{ ns}$, $t_f \leq 3\text{ ns}$.
 - D. The outputs are measured one at a time with one input transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PHL} and t_{PLH} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

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