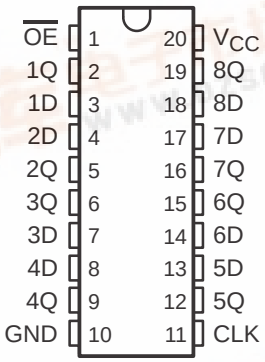
SN54LV374A, SN74LV374A
OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

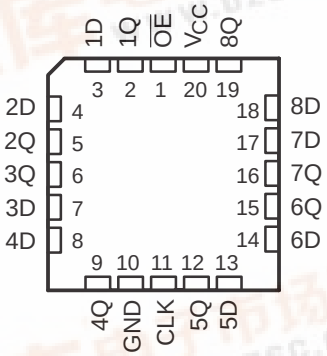
SCLS408B – APRIL 1998 – REVISED MAY 2000

- *EPIC*™ (Enhanced-Performance Implanted CMOS) Process
- Typical V_{OLP} (Output Ground Bounce) <0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot) >2.3 V at V_{CC} = 3.3 V, T_A = 25°C
- 2-V to 5.5-V V_{CC} Operation
- Support Mixed-Mode Voltage Operation on All Ports
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Package Options Include Plastic Small-Outline (DW, NS), Shrink Small-Outline (DB), Thin Very Small-Outline (DGV), and Thin Shrink Small-Outline (PW) Packages, Ceramic Flat (W) Packages, Chip Carriers (FK), and DIPs (J)

SN54LV374A . . . J OR W PACKAGE
SN74LV374A . . . DB, DGV, DW, NS, OR PW PACKAGE
(TOP VIEW)



SN54LV374A . . . FK PACKAGE
(TOP VIEW)



description

The ’LV374A devices are octal edge-triggered D-type flip-flops designed for 2-V to 5.5-V V_{CC} operation.

These devices feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

On the positive transition of the clock (CLK) input, the Q outputs are set to the logic levels set up at the data (D) inputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components.

$\overline{OE}$ does not affect internal operations of the latch. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54LV374A is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LV374A is characterized for operation from –40°C to 85°C.

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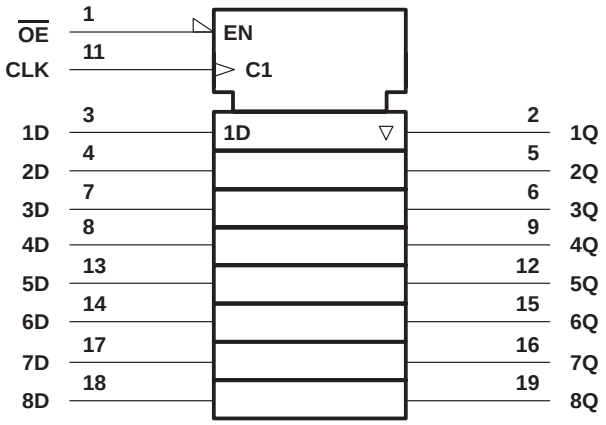
FUNCTION TABLE
(each flip-flop)

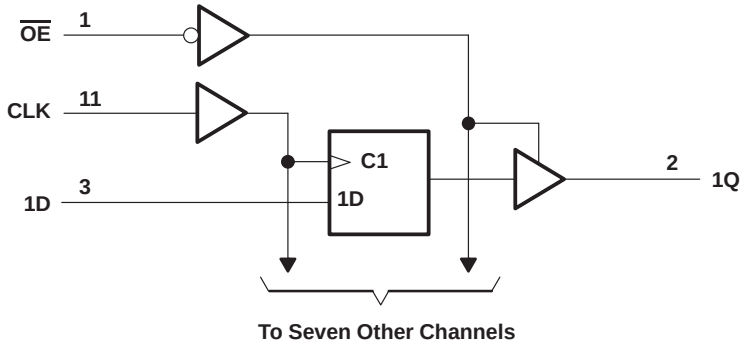
INPUTS			OUTPUT
$\overline{OE}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	–0.5 V to 7 V
Output voltage range, V_O (see Notes 1 and 2)	–0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC})	±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC})	±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC})	±35 mA
Continuous current through V_{CC} or GND	±70 mA
Package thermal impedance, θ_{JA} (see Note 3): DB package	70°C/W
DGV package	92°C/W
DW package	58°C/W
NS package	60°C/W
PW package	83°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. This value is limited to 5.5 V maximum.
3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

			SN54LV374A		SN74LV374A		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2	5.5	2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		1.5		V
		V_{CC} = 2.3 V to 2.7 V	$V_{CC} \times 0.7$		$V_{CC} \times 0.7$		
		V_{CC} = 3 V to 3.6 V	$V_{CC} \times 0.7$		$V_{CC} \times 0.7$		
		V_{CC} = 4.5 V to 5.5 V	$V_{CC} \times 0.7$		$V_{CC} \times 0.7$		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5		0.5	V
		V_{CC} = 2.3 V to 2.7 V		$V_{CC} \times 0.3$		$V_{CC} \times 0.3$	
		V_{CC} = 3 V to 3.6 V		$V_{CC} \times 0.3$		$V_{CC} \times 0.3$	
		V_{CC} = 4.5 V to 5.5 V		$V_{CC} \times 0.3$		$V_{CC} \times 0.3$	
V_I	Input voltage		0	5.5	0	5.5	V
V_O	Output voltage	High or low state	0	V_{CC}	0	V_{CC}	V
		3-state	0	5.5	0	5.5	
I_{OH}	High-level output current	V_{CC} = 2 V		–50		–50	μA
		V_{CC} = 2.3 V to 2.7 V		–2		–2	mA
		V_{CC} = 3 V to 3.6 V		–8		–8	
		V_{CC} = 4.5 V to 5.5 V		–16		–16	
I_{OL}	Low-level output current	V_{CC} = 2 V		50		50	μA
		V_{CC} = 2.3 V to 2.7 V		2		2	mA
		V_{CC} = 3 V to 3.6 V		8		8	
		V_{CC} = 4.5 V to 5.5 V		16		16	
$\Delta t/\Delta v$	Input transition rise or fall rate	V_{CC} = 2.3 V to 2.7 V	0	200	0	200	ns/V
		V_{CC} = 3 V to 3.6 V	0	100	0	100	
		V_{CC} = 4.5 V to 5.5 V	0	20	0	20	
T_A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	SN54LV374A			SN74LV374A			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OH}	I_{OH} = –50 μA	2 V to 5.5 V	V_{CC}–0.1			V_{CC}–0.1			V
	I_{OH} = –2 mA	2.3 V	2			2			
	I_{OH} = –8 mA	3 V	2.48			2.48			
	I_{OH} = –16 mA	4.5 V	3.8			3.8			
V_{OL}	I_{OL} = 50 μA	2 V to 5.5 V			0.1			0.1	V
	I_{OL} = 2 mA	2.3 V			0.4			0.4	
	I_{OL} = 8 mA	3 V			0.44			0.44	
	I_{OL} = 16 mA	4.5 V			0.55			0.55	
I_I	$V_I = V_{CC}$ or GND	0 V to 5.5 V			±1			±1	μA
I_{OZ}	$V_O = V_{CC}$ or GND	5.5 V			±5			±5	μA
I_{CC}	$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			20			20	μA
I_{off}	V_I or V_O = 0 to 5.5 V	0 V			5			5	μA
C_i	$V_I = V_{CC}$ or GND	3.3 V		2.9			2.9		pF

timing requirements over recommended operating free-air temperature range, V_{CC} = 2.5 V ± 0.2 V (unless otherwise noted) (see Figure 1)

		T_A = 25°C		SN54LV374A		SN74LV374A		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, CLK high or low	6		7		7		ns
t_{su}	Setup time, data before CLK↑	5		5.5		5.5		ns
t_h	Hold time, data after CLK↑	2.5		2.5		2.5		ns

timing requirements over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

		T_A = 25°C		SN54LV374A		SN74LV374A		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, CLK high or low	5		5.5		5.5		ns
t_{su}	Setup time, data before CLK↑	4.5		4.5		4.5		ns
t_h	Hold time, data after CLK↑	2		2		2		ns

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

		T_A = 25°C		SN54LV374A		SN74LV374A		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, CLK high or low	5		5		5		ns
t_{su}	Setup time, data before CLK↑	3		3		3		ns
t_h	Hold time, data after CLK↑	2		2		2		ns

switching characteristics over recommended operating free-air temperature range, V_{CC} = 2.5 V ± 0.2 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			SN54LV374A		SN74LV374A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			C_L = 15 pF	60*	105*		50*		50		MHz
			C_L = 50 pF	50	85		40		40		
t_{pd}	CLK	Q	C_L = 15 pF		9.7*	16.3*	1*	19*	1	19	ns
t_{en}	$\overline{OE}$	Q			8.9*	15.9*	1*	19*	1	19	
t_{dis}	$\overline{OE}$	Q			6.3*	12.6*	1*	15*	1	15	
t_{pd}	CLK	Q	C_L = 50 pF		11.8	19.3	1	23	1	23	ns
t_{en}	$\overline{OE}$	Q			10.9	18.8	1	22	1	22	
t_{dis}	$\overline{OE}$	Q			8.2	17.3	1	19	1	19	
$t_{sk(o)}$						2				2	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			SN54LV374A		SN74LV374A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			C_L = 15 pF	80*	150*		70*		70		MHz
			C_L = 50 pF	55	110		50		50		
t_{pd}	CLK	Q	C_L = 15 pF		6.8*	12.7*	1*	15*	1	15	ns
t_{en}	$\overline{OE}$	Q			6.3*	11*	1*	13*	1	13	
t_{dis}	$\overline{OE}$	Q			4.7*	10.5*	1*	12.5*	1	12.5	
t_{pd}	CLK	Q	C_L = 50 pF		8.3	16.2	1	18.5	1	18.5	ns
t_{en}	$\overline{OE}$	Q			7.7	14.5	1	16.5	1	16.5	
t_{dis}	$\overline{OE}$	Q			5.9	14	1	16	1	16	
$t_{sk(o)}$						1.5				1.5	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			SN54LV374A		SN74LV374A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			C_L = 15 pF	130*	205*		110*		110		MHz
			C_L = 50 pF	85	170		75		75		
t_{pd}	CLK	Q	C_L = 15 pF		4.9*	8.1*	1*	9.5*	1	9.5	ns
t_{en}	$\overline{OE}$	Q			4.6*	7.6*	1*	9*	1	9	
t_{dis}	$\overline{OE}$	Q			3.4*	6.8*	1*	8*	1	8	
t_{pd}	CLK	Q	C_L = 50 pF		5.9	10.1	1	11.5	1	11.5	ns
t_{en}	$\overline{OE}$	Q			5.5	9.6	1	11	1	11	
t_{dis}	$\overline{OE}$	Q			4	8.8	1	10	1	10	
$t_{sk(o)}$						1				1	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

noise characteristics, V_{CC} = 3.3 V, C_L = 50 pF, T_A = 25°C (see Note 5)

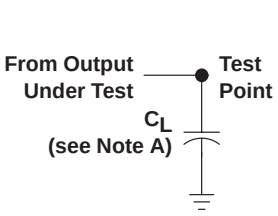
PARAMETER		SN74LV374A			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.6	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		–0.5	–0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		2.9		V
$V_{IH(D)}$	High-level dynamic input voltage	2.31			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.99	V

NOTE 5: Characteristics are for surface-mount packages only.

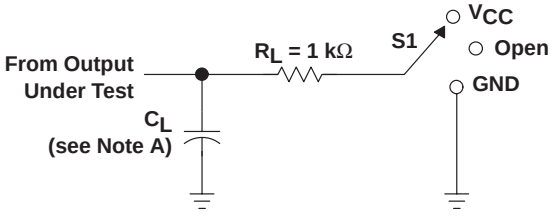
operating characteristics, T_A = 25°C

PARAMETER			TEST CONDITIONS		V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	Outputs enabled	C_L = 50 pF,	f = 10 MHz	3.3 V	21.1	pF
					5 V	22.8	

PARAMETER MEASUREMENT INFORMATION

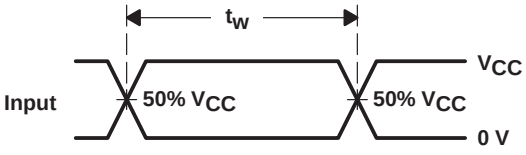


LOAD CIRCUIT FOR
TOTEM-POLE OUTPUTS

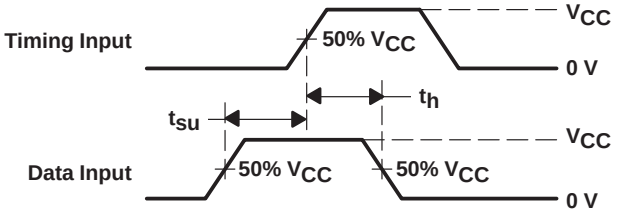


LOAD CIRCUIT FOR
3-STATE AND OPEN-DRAIN OUTPUTS

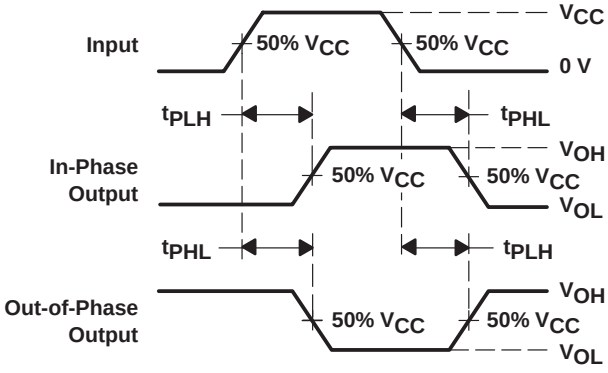
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND
Open Drain	V_{CC}



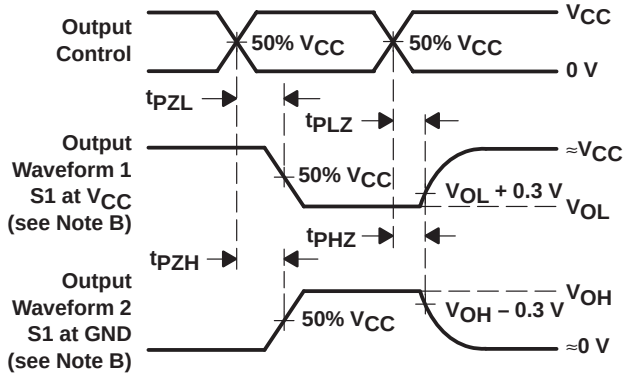
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 3 ns, t_f ≤ 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PHL} and t_{PLH} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

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