

- **EPIC™ (Enhanced-Performance Implanted CMOS) Process**
- **2-V to 5.5-V V_{CC} Operation**
- **Support Mixed-Mode Voltage Operation on All Ports**
- **Schmitt-Trigger Circuitry on \bar{A} , B, and \bar{CLR} Inputs for Slow Input Transition Rates**
- **Edge Triggered From Active-High or Active-Low Gated Logic Inputs**
- **Overriding Clear Terminates Output Pulse**
- **Glitch-Free Power-Up Reset on Outputs**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)
- **Package Options Include Plastic Small-Outline (D, NS), Shrink Small-Outline (DB), Thin Very Small-Outline (DGV), and Thin Shrink Small-Outline (PW) Packages, Ceramic Flat (W) Packages, Chip Carriers (FK), and DIPs (J)**

description

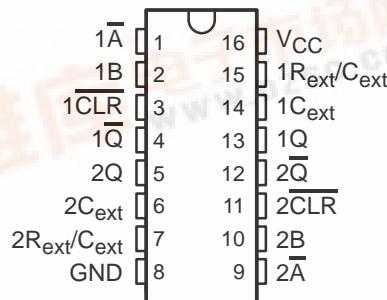
The 'LV221A devices are dual multivibrators designed for 2-V to 5.5-V V_{CC} operation. Each multivibrator has a negative-transition-triggered (\bar{A}) input and a positive-transition-triggered (B) input, either of which can be used as an inhibit input.

These edge-triggered multivibrators feature output pulse-duration control by three methods. In the first method, the \bar{A} input is low and the B input goes high. In the second method, the B input is high and the \bar{A} input goes low. In the third method, the \bar{A} input is low, the B input is high, and the clear (\bar{CLR}) input goes high.

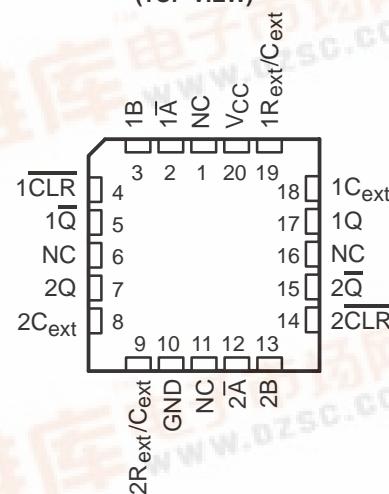
The output pulse duration is programmable by selecting external resistance and capacitance values. The external timing capacitor must be connected between C_{ext} and R_{ext}/C_{ext} (positive) and an external resistor connected between R_{ext}/C_{ext} and V_{CC} . To obtain variable pulse durations, connect an external variable resistor between R_{ext}/C_{ext} and V_{CC} . The output pulse duration can also be reduced by taking \bar{CLR} low.

Pulse triggering occurs at a particular voltage level and is not directly related to the transition time of the input pulse. The \bar{A} , B, and \bar{CLR} inputs have Schmitt triggers with sufficient hysteresis to handle slow input transition rates with jitter-free triggering at the outputs.

SN54LV221A...J OR W PACKAGE
SN74LV221A...D, DB, DGV, NS, OR PW PACKAGE
(TOP VIEW)



SN54LV221A...FK PACKAGE
(TOP VIEW)



NC – No internal connection



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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description (continued)

Once triggered, the outputs are independent of further transitions of the \bar{A} and B inputs and are a function of the timing components, or the output pulses can be terminated by the overriding clear. Input pulses may be of any duration relative to the output pulse. Output pulse duration can be varied by choosing the appropriate timing components. Output rise and fall times are TTL compatible and independent of pulse duration. Typical triggering and clearing sequences are illustrated in the input/output timing diagram.

The variance in output pulse duration from device to device typically is less than $\pm 0.5\%$ for given external timing components. An example of this distribution for the 'LV221A is shown in Figure 8. Variations in output pulse duration versus supply voltage and temperature are shown in Figure 5.

During power up, Q outputs are in the high state, and \bar{Q} outputs are in the low state. The outputs are glitch free without applying a reset pulse.

Pin assignments are identical to those of the 'AHC123A and 'AHCT123A devices, so the 'LV221A can be substituted for those devices not using the retrigger feature.

The SN54LV221A is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LV221A is characterized for operation from -40°C to 85°C .

For additional application information on multivibrators, see the application report *Designing With The SN74AHC123A and SN74AHCT123A*, literature number SCLA014.

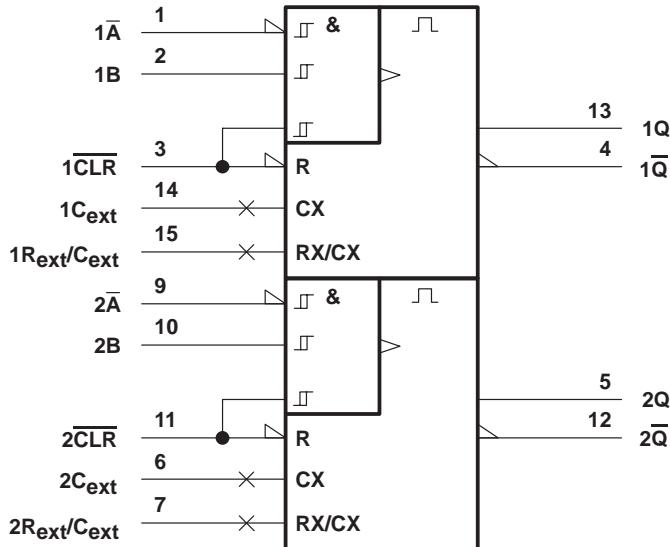
FUNCTION TABLE
(each multivibrator)

INPUTS			OUTPUTS		FUNCTION
CLR	\bar{A}	B	Q	\bar{Q}	
L	X	X	L	H	Reset
H	H	X	L	H	Inhibit
H	X	L	L	H	Inhibit
H	L	\uparrow	$\uparrow\!\!\!\uparrow$	$\uparrow\!\!\!\uparrow$	Outputs enabled
H	\downarrow	H	$\uparrow\!\!\!\uparrow$	$\uparrow\!\!\!\uparrow$	Outputs enabled
$\uparrow\!\!\!\uparrow$	L	H	$\uparrow\!\!\!\uparrow$	$\uparrow\!\!\!\uparrow$	Outputs enabled

[†]This condition is true only if the output of the latch formed by the NAND gate has been conditioned to the logic 1 state prior to CLR going high. This latch is conditioned by taking either A high or B low while CLR is inactive (high).

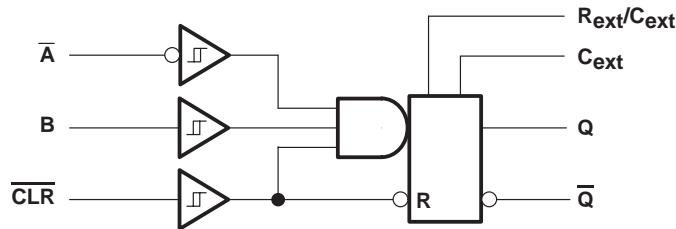
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
 Pin numbers shown are for the D, DB, DGV, J, NS, PW, and W packages.

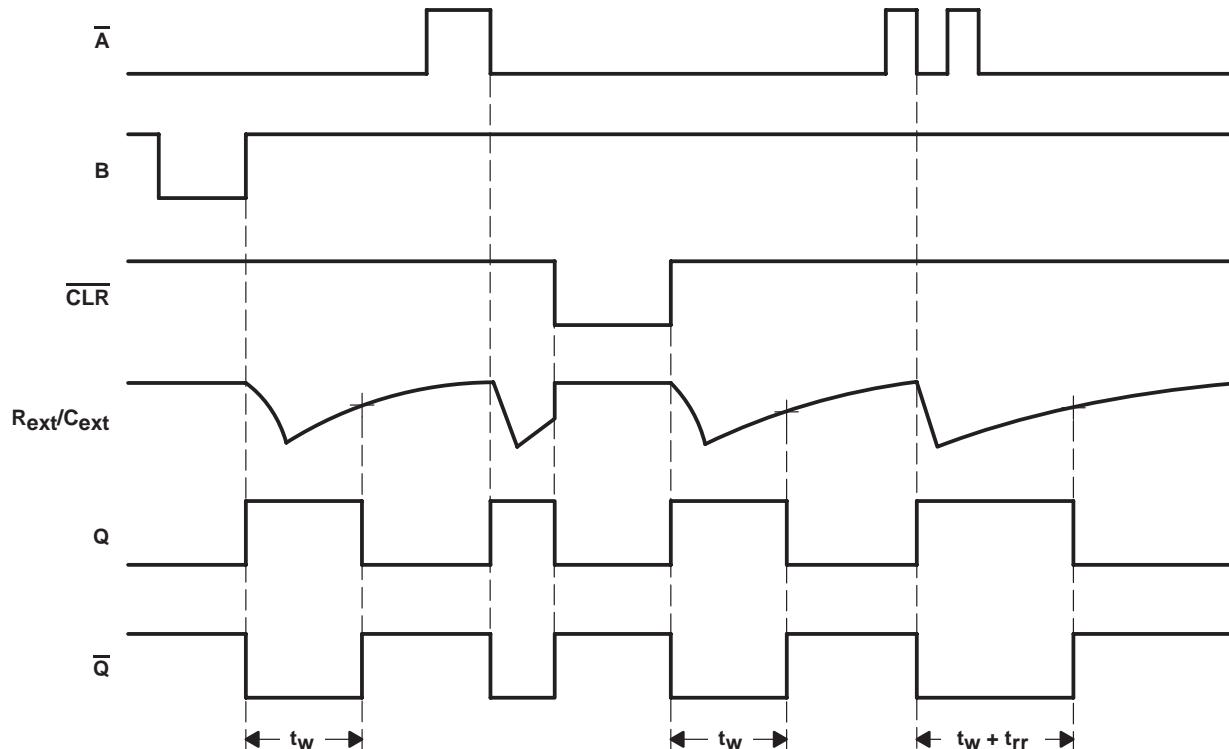
logic diagram, each multivibrator (positive logic)



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input/output timing diagram



absolute maximum ratings over operating free-air temperature (unless otherwise noted)[†]

Supply voltage range, V_{CC}	-0.5 V to 7 V
Input voltage range, V_I (see Note 1)	-0.5 V to 7 V
Output voltage range in high or low state, V_O (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Output voltage range in power-off state, V_O (see Note 1)	-0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$)	-20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	± 50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 25 mA
Continuous current through V_{CC} or GND	± 50 mA
Package thermal impedance, θ_{JA} (see Note 3):	
D package	73°C/W
DB package	82°C/W
DGV package	120°C/W
NS package	64°C/W
PW package	108°C/W
Storage temperature range, T_{stg}	-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
 2. This value is limited to 5.5 V maximum.
 3. The package thermal impedance is calculated in accordance with JESD 51.

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recommended operating conditions (see Note 4)

		SN54LV221A		SN74LV221A		UNIT
		MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage	2	5.5	2	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 2 V	1.5	1.5	1.5	V
		V _{CC} = 2.3 V to 2.7 V	V _{CC} × 0.7	V _{CC} × 0.7	V _{CC} × 0.7	
		V _{CC} = 3 V to 3.6 V	V _{CC} × 0.7	V _{CC} × 0.7	V _{CC} × 0.7	
		V _{CC} = 4.5 V to 5.5 V	V _{CC} × 0.7	V _{CC} × 0.7	V _{CC} × 0.7	
V _{IL}	Low-level input voltage	V _{CC} = 2 V	0.5	0.5	0.5	V
		V _{CC} = 2.3 V to 2.7 V	V _{CC} × 0.3	V _{CC} × 0.3	V _{CC} × 0.3	
		V _{CC} = 3 V to 3.6 V	V _{CC} × 0.3	V _{CC} × 0.3	V _{CC} × 0.3	
		V _{CC} = 4.5 V to 5.5 V	V _{CC} × 0.3	V _{CC} × 0.3	V _{CC} × 0.3	
V _I	Input voltage	0	5.5	0	5.5	V
V _O	Output voltage	0	V _{CC}	0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 2 V	-50	-50	-50	μA
		V _{CC} = 2.3 V to 2.7 V	-2	-2	-2	mA
		V _{CC} = 3 V to 3.6 V	-6	-6	-6	
		V _{CC} = 4.5 V to 5.5 V	-12	-12	-12	
I _{OL}	Low-level output current	V _{CC} = 2 V	50	50	50	μA
		V _{CC} = 2.3 V to 2.7 V	2	2	2	mA
		V _{CC} = 3 V to 3.6 V	6	6	6	
		V _{CC} = 4.5 V to 5.5 V	12	12	12	
R _{ext}	External timing resistance	V _{CC} = 2 V	5k	5k	5k	Ω
		V _{CC} ≥ 3 V	1k	1k	1k	
C _{ext}	External timing capacitance	No restriction		No restriction		pF
Δt/ΔV _{CC}	Power-up ramp rate	1		1		ms/V
T _A	Operating free-air temperature	-55	125	-40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	SN54LV221A			SN74LV221A			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V _{OH}	I _{OH} = -50 µA	2 V to 5.5 V	V _{CC} –0.1			V _{CC} –0.1			V
	I _{OH} = -2 mA	2.3 V	2			2			
	I _{OH} = -6 mA	3 V	2.48			2.48			
	I _{OH} = -12 mA	4.5 V	3.8			3.8			
V _{OL}	I _{OL} = 50 µA	2 V to 5.5 V		0.1		0.1			V
	I _{OL} = 2 mA	2.3 V		0.4		0.4			
	I _{OL} = 6 mA	3 V		0.44		0.44			
	I _{OL} = 12 mA	4.5 V		0.55		0.55			
I _I	R _{ext} /C _{ext} †	V _I = V _{CC} or GND	2 V to 5.5 V		±2.5		±2.5		µA
	A, B, and CLR	V _I = V _{CC} or GND	0 V		±1		±1		
			5.5 V		±1		±1		
I _{CC}	Quiescent	V _I = V _{CC} or GND, I _O = 0	5.5 V		20		20		µA
I _{CC}	Active state (per circuit)	V _I = V _{CC} or GND, R _{ext} /C _{ext} = 0.5 V _{CC}	2.3 V		220		220		µA
			3 V		280		280		
			4.5 V		650		650		
			5.5 V		975		975		
I _{off}		V _I or V _O = 0 to 5.5 V	0 V				5		µA
C _i		V _I = V _{CC} or GND	3.3 V		1.9		1.9		pF
			5 V		1.9		1.9		

† This test is performed with the terminal in the off-state condition.

timing requirements over recommended operating free-air temperature range, V_{CC} = 2.5 V ± 0.2 V (unless otherwise noted) (see Figure 1)

	TEST CONDITIONS	T _A = 25°C			SN54LV221A		SN74LV221A		UNIT
		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _w	Pulse duration	CLR A or B trigger		6		6.5		6.5	ns
				6		6.5		6.5	

timing requirements over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

	TEST CONDITIONS	T _A = 25°C			SN54LV221A		SN74LV221A		UNIT
		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _w	Pulse duration	CLR A or B trigger		5		5		5	ns
				5		5		5	

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

	TEST CONDITIONS	T _A = 25°C			SN54LV221A		SN74LV221A		UNIT
		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _w	Pulse duration	CLR A or B trigger		5		5		5	ns
				5		5		5	

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switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	$T_A = 25^\circ\text{C}$			SN54LV221A		SN74LV221A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	\bar{A} or B	Q or \bar{Q}	$C_L = 15 \text{ pF}$	14.6*	31.4*	37*	1*	37*	1	37	ns
	\bar{CLR}	Q or \bar{Q}		13.2*	25*	29.5*	1*	29.5*	1	29.5	
	CLR trigger	Q or \bar{Q}		15.2*	33.4*	39*	1*	39*	1	39	
t_{pd}	\bar{A} or B	Q or \bar{Q}	$C_L = 50 \text{ pF}$	16.7	36	42	1	42	1	42	ns
	\bar{CLR}	Q or \bar{Q}		15	32.8	34.5	1	34.5	1	34.5	
	CLR trigger	Q or \bar{Q}		17.4	38	44	1	44	1	44	
t_w^\dagger		Q or \bar{Q}	$C_L = 50 \text{ pF}$, $C_{ext} = 28 \text{ pF}$, $R_{ext} = 2 \text{ k}\Omega$	203	260	320			320	ns	μs
			$C_L = 50 \text{ pF}$, $C_{ext} = 0.01 \mu\text{F}$, $R_{ext} = 10 \text{ k}\Omega$	90	100	110	90	110	90	110	
			$C_L = 50 \text{ pF}$, $C_{ext} = 0.1 \mu\text{F}$, $R_{ext} = 10 \text{ k}\Omega$	0.9	1	1.1	0.9	1.1	0.9	1.1	
Δt_w^\ddagger			$C_L = 50 \text{ pF}$	± 1							%

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† t_w = Duration of pulse at Q and \bar{Q} outputs

‡ Δt_w = Output pulse duration variation (Q and \bar{Q}) between circuits in same package

switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	$T_A = 25^\circ\text{C}$			SN54LV221A		SN74LV221A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	\bar{A} or B	Q or \bar{Q}	$C_L = 15 \text{ pF}$	10.2*	20.6*	24*	1*	24*	1	24	ns
	\bar{CLR}	Q or \bar{Q}		9.3*	15.8*	18.5*	1*	18.5*	1	18.5	
	CLR trigger	Q or \bar{Q}		10.6*	22.4*	26*	1*	26*	1	26	
t_{pd}	\bar{A} or B	Q or \bar{Q}	$C_L = 50 \text{ pF}$	11.8	24.1	27.5	1	27.5	1	27.5	ns
	\bar{CLR}	Q or \bar{Q}		10.6	19.3	22	1	22	1	22	
	CLR trigger	Q or \bar{Q}		12.3	25.9	29.5	1	29.5	1	29.5	
t_w^\dagger		Q or \bar{Q}	$C_L = 50 \text{ pF}$, $C_{ext} = 28 \text{ pF}$, $R_{ext} = 2 \text{ k}\Omega$	186	240	300			300	ns	μs
			$C_L = 50 \text{ pF}$, $C_{ext} = 0.01 \mu\text{F}$, $R_{ext} = 10 \text{ k}\Omega$	90	100	110	90	110	90	110	
			$C_L = 50 \text{ pF}$, $C_{ext} = 0.1 \mu\text{F}$, $R_{ext} = 10 \text{ k}\Omega$	0.9	1	1.1	0.9	1.1	0.9	1.1	
Δt_w^\ddagger			$C_L = 50 \text{ pF}$	± 1							%

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† t_w = Duration of pulse at Q and \bar{Q} outputs

‡ Δt_w = Output pulse duration variation (Q and \bar{Q}) between circuits in same package

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switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	$T_A = 25^\circ\text{C}$			SN54LV221A		SN74LV221A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	\overline{A} or B	Q or \overline{Q}	$C_L = 15 \text{ pF}$	7.1*	12*	1*	14*	1	14	1	ns
	\overline{CLR}	Q or \overline{Q}		6.5*	9.4*	1*	11*	1	11	1	
	CLR trigger	Q or \overline{Q}		7.3*	12.9*	1*	15*	1	15	1	
t_{pd}	\overline{A} or B	Q or \overline{Q}	$C_L = 50 \text{ pF}$	8.2	14	1	16	1	16	1	ns
	\overline{CLR}	Q or \overline{Q}		7.4	11.4	1	13	1	13	1	
	CLR trigger	Q or \overline{Q}		8.6	14.9	1	17	1	17	1	
t_w [†]		Q or \overline{Q}	$C_L = 50 \text{ pF}$, $C_{ext} = 28 \text{ pF}$, $R_{ext} = 2 \text{ k}\Omega$	171	200		240		240	ns	
			$C_L = 50 \text{ pF}$, $C_{ext} = 0.01 \mu\text{F}$, $R_{ext} = 10 \text{ k}\Omega$	90	100	110	90	110	90	110	μs
			$C_L = 50 \text{ pF}$, $C_{ext} = 0.1 \mu\text{F}$, $R_{ext} = 10 \text{ k}\Omega$	0.9	1	1.1	0.9	1.1	0.9	1.1	ms
Δt_w [‡]			$C_L = 50 \text{ pF}$	± 1							%

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† t_w = Duration of pulse at Q and \overline{Q} outputs

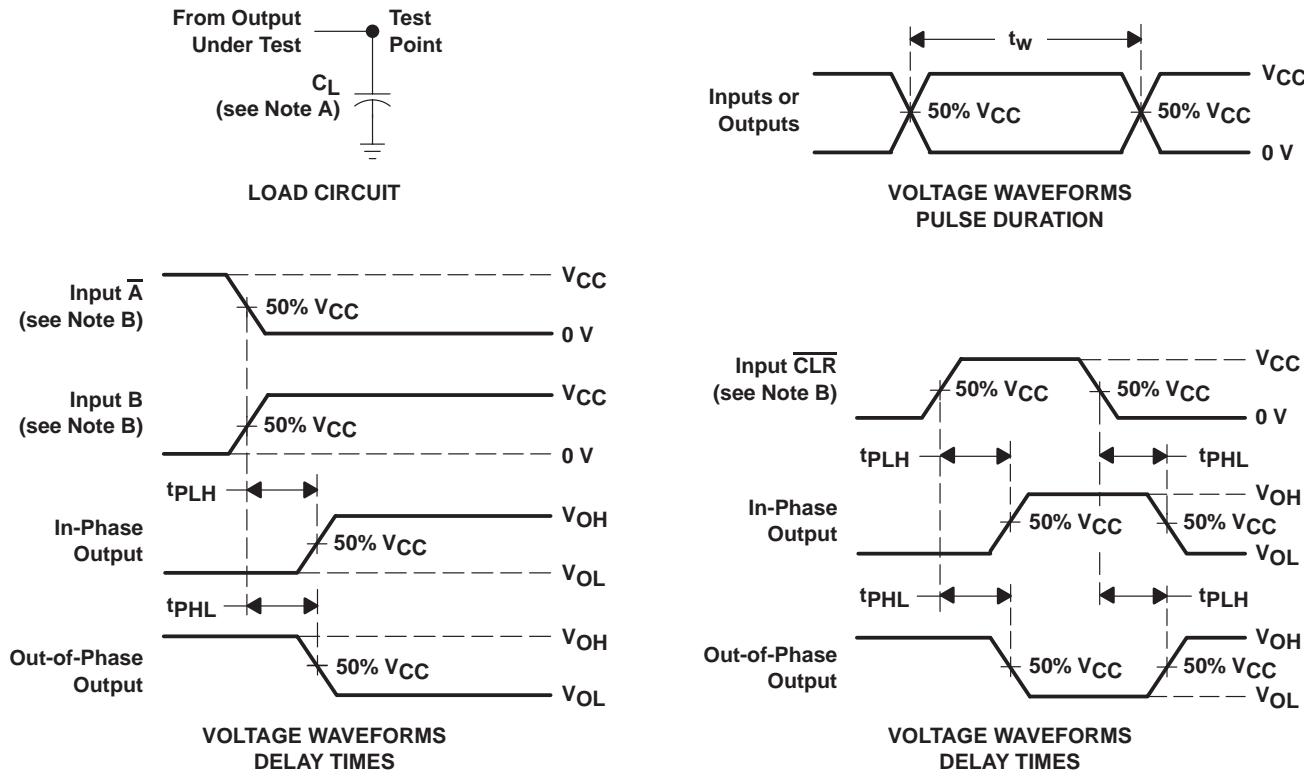
‡ Δt_w = Output pulse duration variation (Q and \overline{Q}) between circuits in same package

operating characteristics, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd} Power dissipation capacitance	$C_L = 50 \text{ pF}$, $f = 10 \text{ MHz}$	3.3 V	50	pF
		5 V	51	

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PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.
 B. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, $Z_O = 50 \Omega$, $t_r = 3$ ns, $t_f = 3$ ns.
 C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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APPLICATION INFORMATION

caution in use

To prevent malfunctions due to noise, connect a high-frequency capacitor between V_{CC} and GND, and keep the wiring between the external components and C_{ext} and R_{ext}/C_{ext} terminals as short as possible.

power-down considerations

Large values of C_{ext} can cause problems when powering down the 'LV221A because of the amount of energy stored in the capacitor. When a system containing this device is powered down, the capacitor can discharge from V_{CC} through the protection diodes at pin 2 or pin 14. Current through the input protection diodes must be limited to 30 mA; therefore, the turn-off time of the V_{CC} power supply must not be faster than $t = V_{CC} \times C_{ext}/30$ mA. For example, if $V_{CC} = 5$ V and $C_{ext} = 15$ pF, the V_{CC} supply must turn off no faster than $t = (5\text{ V}) \times (15\text{ pF})/30\text{ mA} = 2.5$ ms. Usually, this is not a problem because power supplies are heavily filtered and cannot discharge at this rate. When a more rapid decrease of V_{CC} to zero occurs, the 'LV221A can sustain damage. To avoid this possibility, use external clamping diodes.

output pulse duration

The output pulse duration, t_w , is determined primarily by the values of the external capacitance (C_T) and timing resistance (R_T). The timing components are connected as shown in Figure 2.

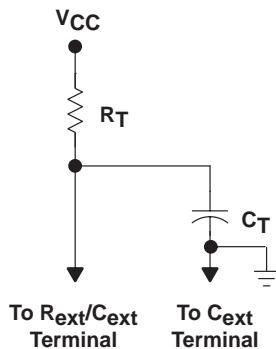


Figure 2. Timing-Component Connections

The pulse duration is given by:

$$t_w = K \times R_T \times C_T \quad (1)$$

if C_T is ≥ 1000 pF, $K = 1.0$

or

if C_T is < 1000 pF, K can be determined from Figure 7

where:

t_w = pulse duration in ns

R_T = external timing resistance in k Ω

C_T = external capacitance in pF

K = multiplier factor

Equation 1 and Figure 3 or 4 can be used to determine values for pulse duration, external resistance, and external capacitance.

APPLICATION INFORMATION[†]

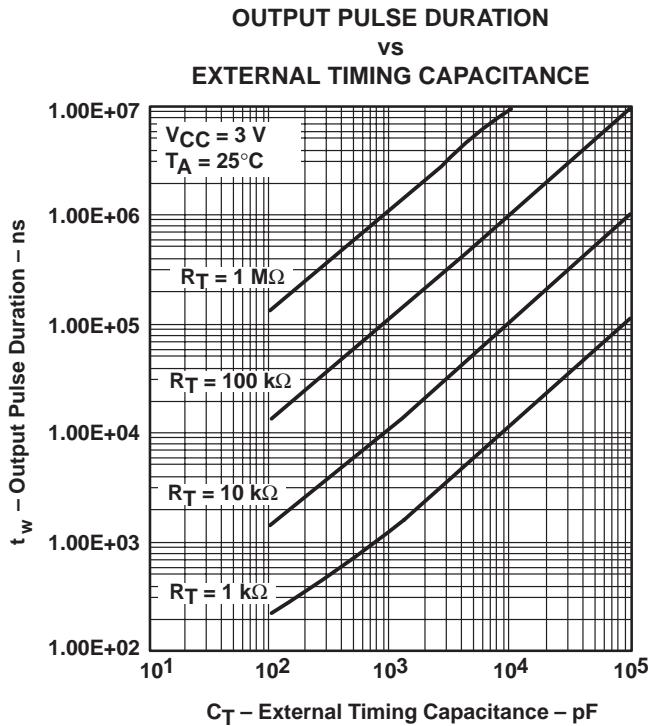


Figure 3

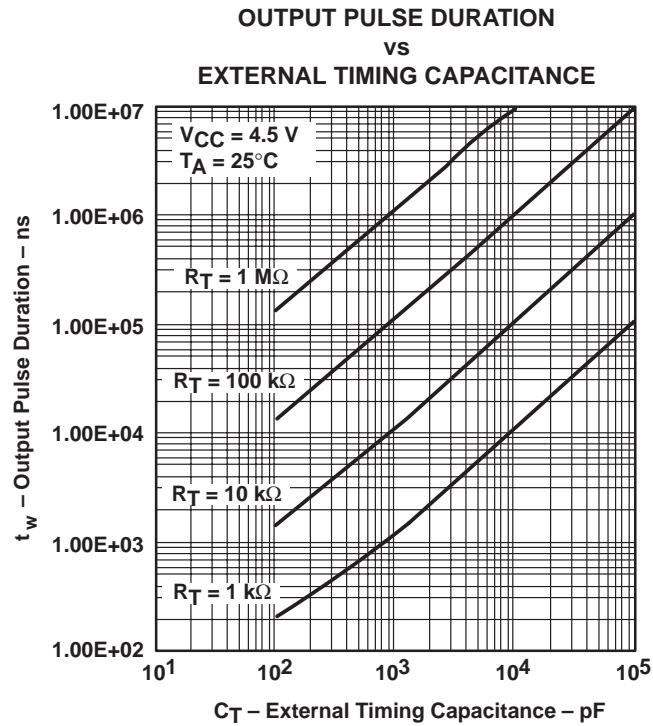


Figure 4

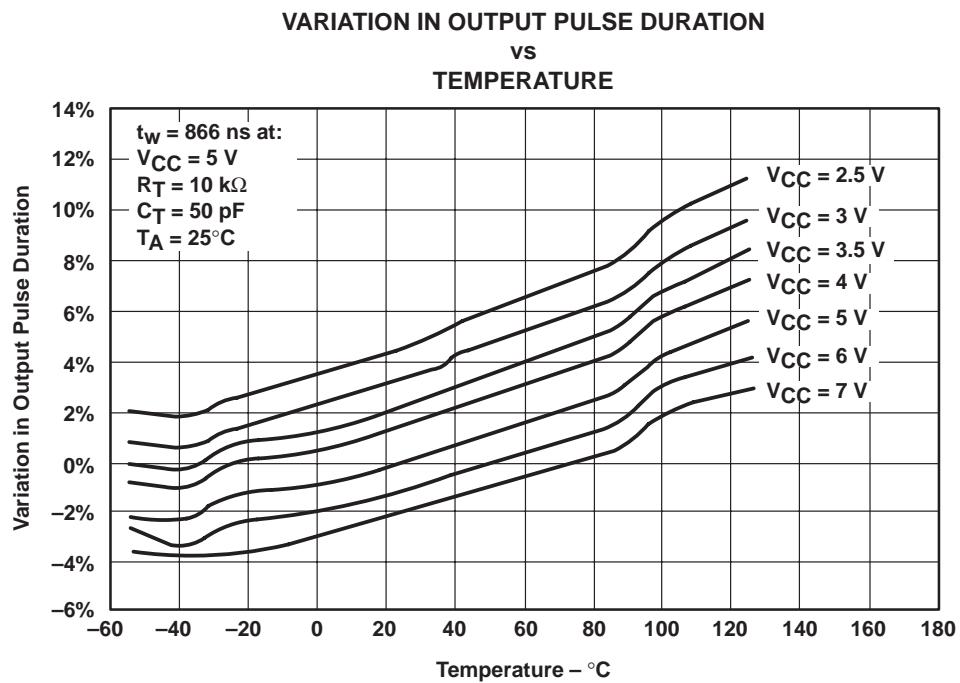


Figure 5

[†] Operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied.

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APPLICATION INFORMATION[†]

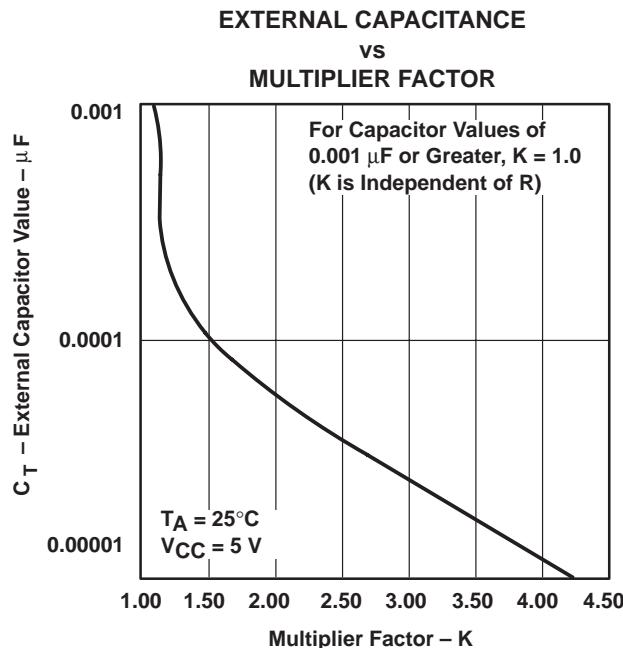


Figure 6

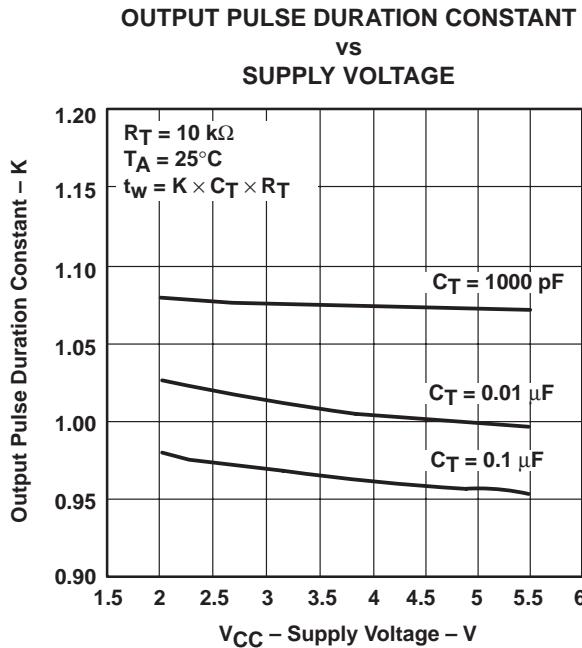


Figure 7

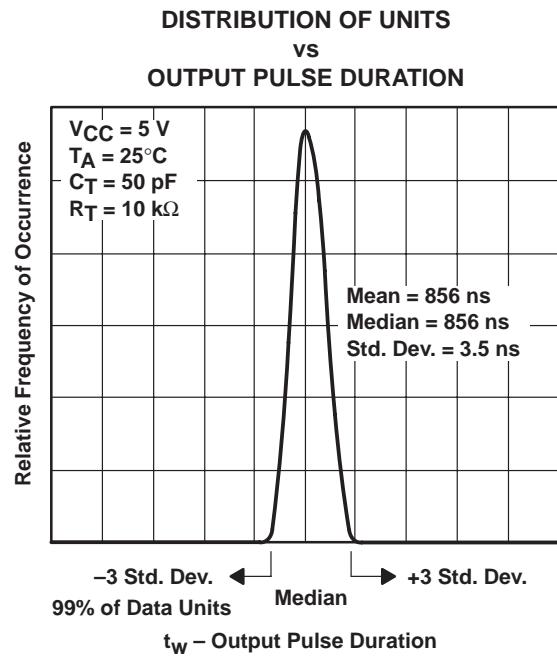


Figure 8

[†] Operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied.

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