

SN54ALS193 SN74ALS193A SYNCHRONOUS 4-BIT UP/DOWN BINARY COUNTERS WITH DUAL CLOCK AND CLEAR

SDAS211B – DECEMBER 1982 – REVISED DECEMBER 1994

- Look-Ahead Circuitry Enhances Cascaded Counters
- Fully Synchronous in Count Modes
- Parallel Asynchronous Load for Modulo-N Count Lengths
- Asynchronous Clear
- Package Options Include Plastic Small-Outline (D) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs

description

The SN54ALS193 and SN74ALS193A are synchronous, reversible, 4-bit up/down binary counters. Synchronous counting operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple-clock) counters.

The outputs of the four flip-flops are triggered on a low-to-high-level transition of either count/clock (UP or DOWN) input. The direction of the count is determined by which count input is pulsed while the other count input is high.

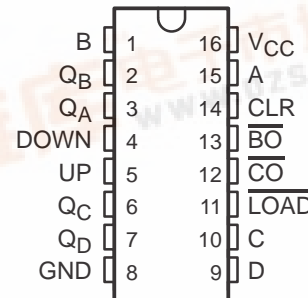
All four counters are fully programmable; that is, each output may be preset to either level by placing a low on the load (\overline{LOAD}) input and entering the desired data at the data inputs. The output changes to agree with the data inputs independently of the count pulses. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

A high level applied to the clear (CLR) input forces all outputs to the low level. The clear function is independent of the count and \overline{LOAD} inputs. The UP, DOWN, and \overline{LOAD} inputs are buffered to lower the drive requirement, which significantly reduces the loading on, or current required by, clock drivers, etc., for long parallel words.

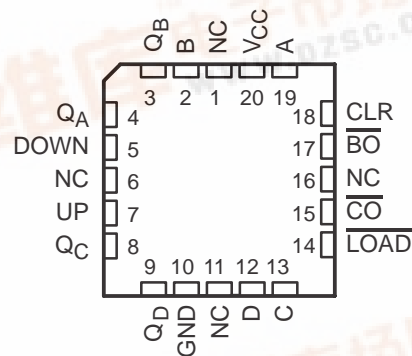
These counters are designed to be cascaded without the need for external circuitry. The borrow (\overline{BO}) output produces a low-level pulse while the count is zero (all Q outputs low) and the DOWN input is low. Similarly, the carry (\overline{CO}) output produces a low-level pulse while the count is 9 or 15 (all Q outputs high) and the UP input is low. The counters can then be easily cascaded by feeding \overline{BO} and \overline{CO} to the count-down and count-up inputs, respectively, of the succeeding counter.

The SN54ALS193 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ALS193A is characterized for operation from 0°C to 70°C .

SN54ALS193 ... J PACKAGE
SN74ALS193A ... D OR N PACKAGE
(TOP VIEW)



SN54ALS193 ... FK PACKAGE
(TOP VIEW)

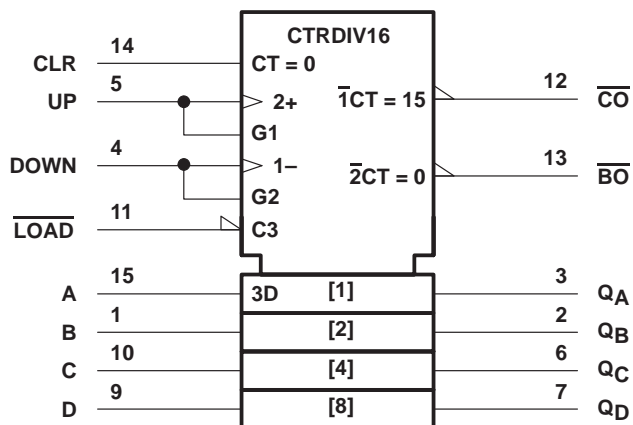


NC – No internal connection

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logic symbol†

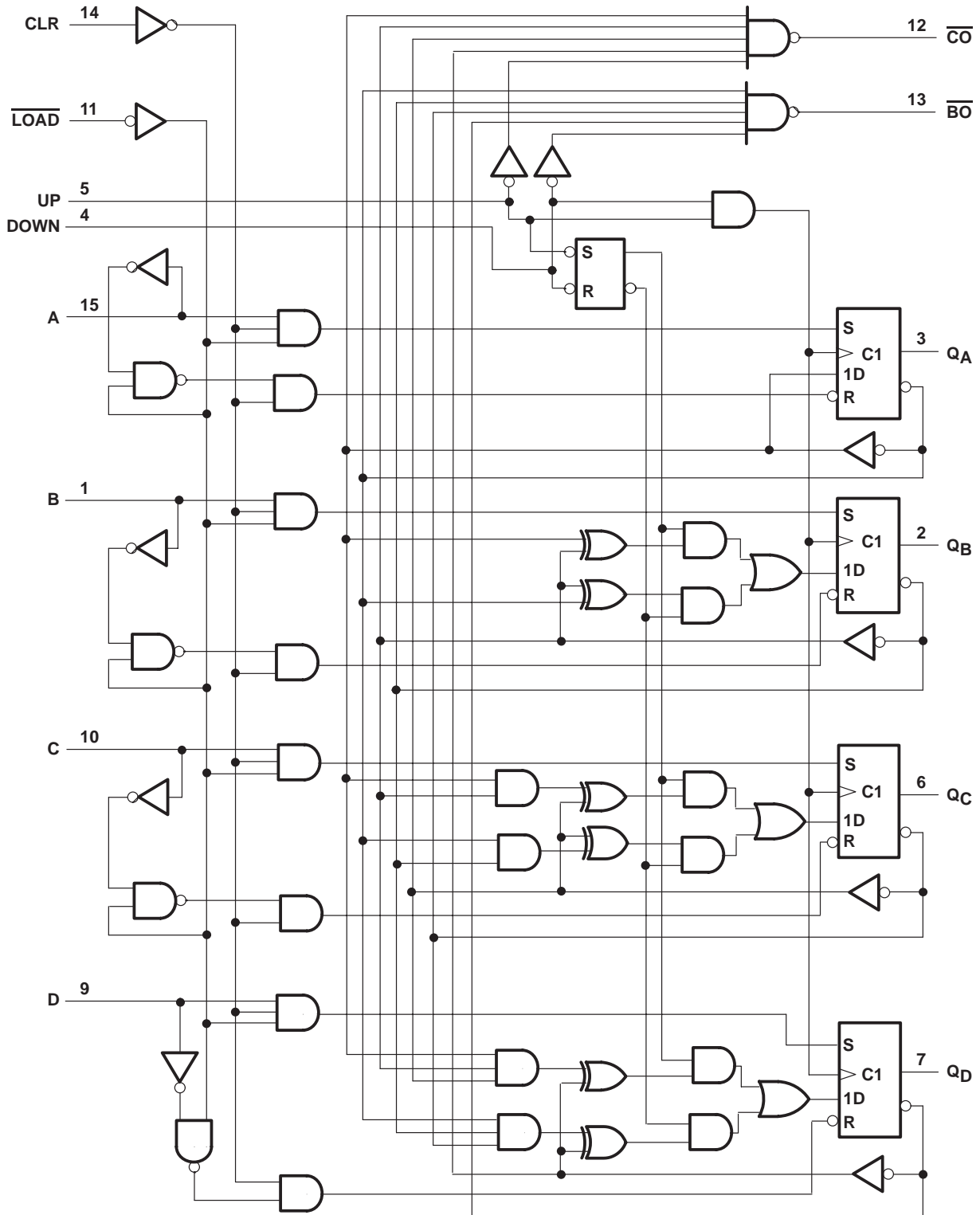


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
 Pin numbers shown are for the D, J, and N packages.

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logic diagram (positive logic)



Pin numbers shown are for the D, J, and N packages.

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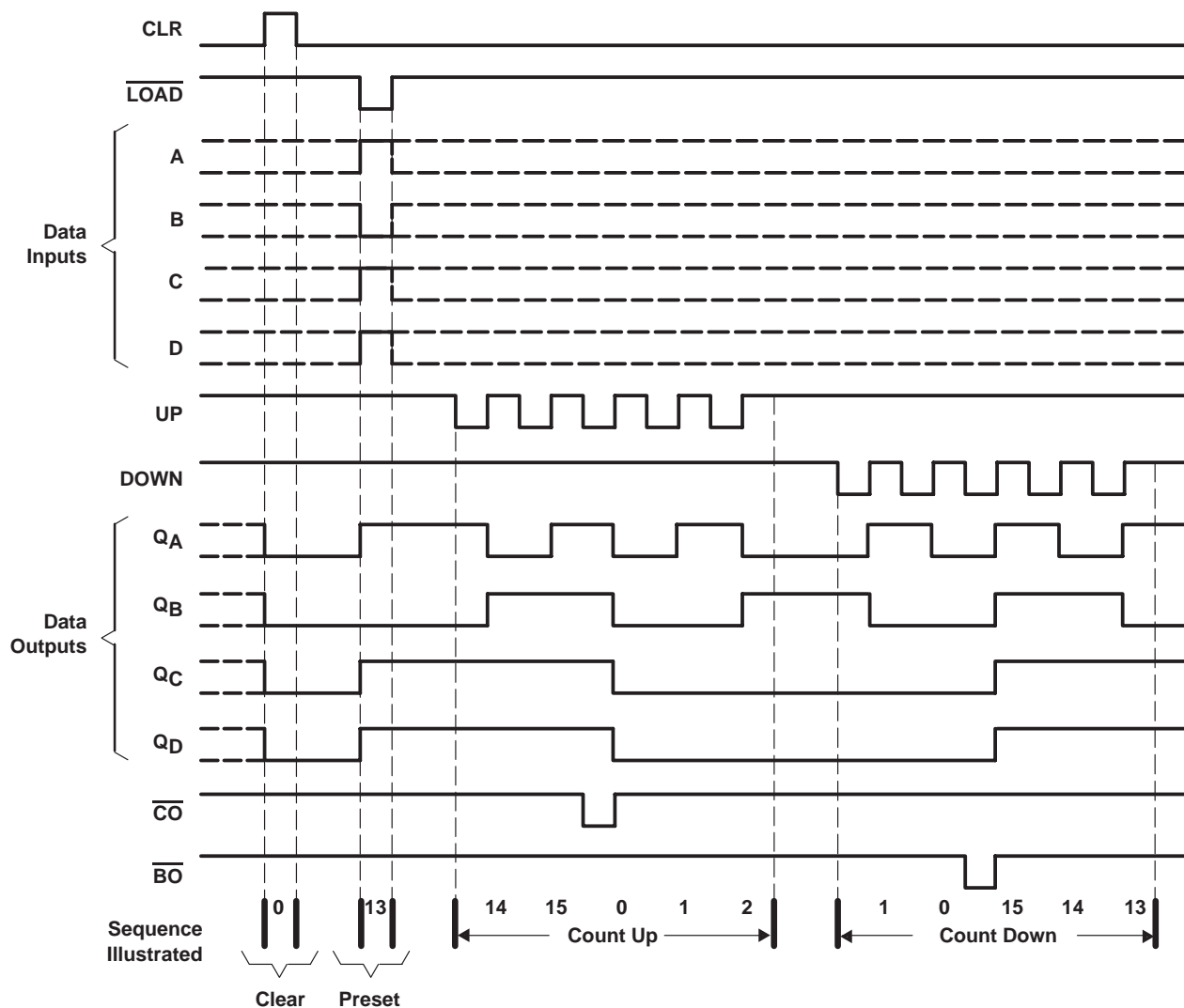
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typical clear, load, and count sequence

Illustrated below is the following sequence:

1. Clear outputs to zero
2. Load (preset) to binary 13
3. Count up to 14, 15 (carry), 0, 1, and 2
4. Count down to 1, 0 (borrow), 15, 14, and 13



NOTES: A. Clear overrides load, data, and count inputs.

B. When counting up, count-down input must be high; when counting down, count-up input must be high.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

| | |
|----------------------------------------------------------|----------------|
| Supply voltage, V_{CC} | 7 V |
| Input voltage, V_I | 7 V |
| Operating free-air temperature range, T_A : SN54ALS193 | –55°C to 125°C |
| SN74ALS193A | 0°C to 70°C |
| Storage temperature range | –65°C to 150°C |

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

| | | SN54ALS193 | | | SN74ALS193A | | | UNIT |
|--------------------|--------------------------------|---------------------------------|-----|------|-------------|-----|------|------|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| V _{CC} | Supply voltage | 4.5 | 5 | 5.5 | 4.5 | 5 | 5.5 | V |
| V _{IH} | High-level input voltage | 2 | | | 2 | | | V |
| V _{IL} | Low-level input voltage | | | 0.7 | | | 0.8 | V |
| I _{OH} | High-level output current | | | −0.4 | | | −0.4 | mA |
| I _{OL} | Low-level output current | | | 4 | | | 8 | mA |
| f _{clock} | Clock frequency | 0 | | 20 | 0 | | 30 | MHz |
| t _w | Pulse duration | CLR high | | 10 | 10 | | ns | |
| | | LOAD low | | 25 | 20 | | | |
| | | UP or DOWN high or low | | 30 | 16.5 | | | |
| t _{su} | Setup time | Data before LOAD↑ | | 25 | 20 | | ns | |
| | | CLR inactive before UP or DOWN | | 20 | 20 | | | |
| | | LOAD inactive before UP or DOWN | | 20 | 20 | | | |
| t _h | Hold time | Data after LOAD↑ | | 5 | 5 | | ns | |
| | | UP high after DOWN↑ | | 0 | 0 | | | |
| | | DOWN high after UP↑ | | 0 | 0 | | | |
| T _A | Operating free-air temperature | −55 | | 125 | 0 | | 70 | °C |

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | SN54ALS193 | | | SN74ALS193A | | | UNIT |
|-----------------|------------|--------------------------------------------|---------------------------|--------------|------------------|------|--------------|------------------|------|------|
| | | | | MIN | TYP [‡] | MAX | MIN | TYP [‡] | MAX | |
| V_{IK} | | $V_{CC} = 4.5\text{ V}$, | $I_I = -18\text{ mA}$ | | | –1.5 | | | –1.5 | V |
| V_{OH} | | $V_{CC} = 4.5\text{ V to } 5.5\text{ V}$, | $I_{OH} = -0.4\text{ mA}$ | $V_{CC} - 2$ | | | $V_{CC} - 2$ | | | V |
| V_{OL} | | $V_{CC} = 4.5\text{ V}$ | $I_{OL} = 4\text{ mA}$ | | 0.25 | 0.4 | | 0.25 | 0.4 | V |
| | | | $I_{OL} = 8\text{ mA}$ | | | | | 0.35 | 0.5 | |
| I_I | | $V_{CC} = 5.5\text{ V}$, | $V_I = 7\text{ V}$ | | | 0.1 | | 0.35 | 0.1 | mA |
| I_{IH} | | $V_{CC} = 5.5\text{ V}$, | $V_I = 2.7\text{ V}$ | | | 20 | | | 20 | μA |
| I_{IL} | UP or DOWN | $V_{CC} = 5.5\text{ V}$, | $V_I = 0.4\text{ V}$ | | | –0.2 | | | –0.2 | mA |
| | All others | | | | | –0.1 | | | –0.1 | |
| $I_{O\text{§}}$ | | $V_{CC} = 5.5\text{ V}$, | $V_O = 2.25\text{ V}$ | –20 | | –112 | –30 | | –112 | mA |
| I_{CC} | | $V_{CC} = 5.5\text{ V}$, | See Note 1 | | 12 | 22 | | 12 | 22 | mA |

[‡] All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

[§] The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS} .

NOTE 1: I_{CC} is measured with the clear and load inputs grounded and all other inputs at 4.5 V.

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switching characteristics (see Figure 1)

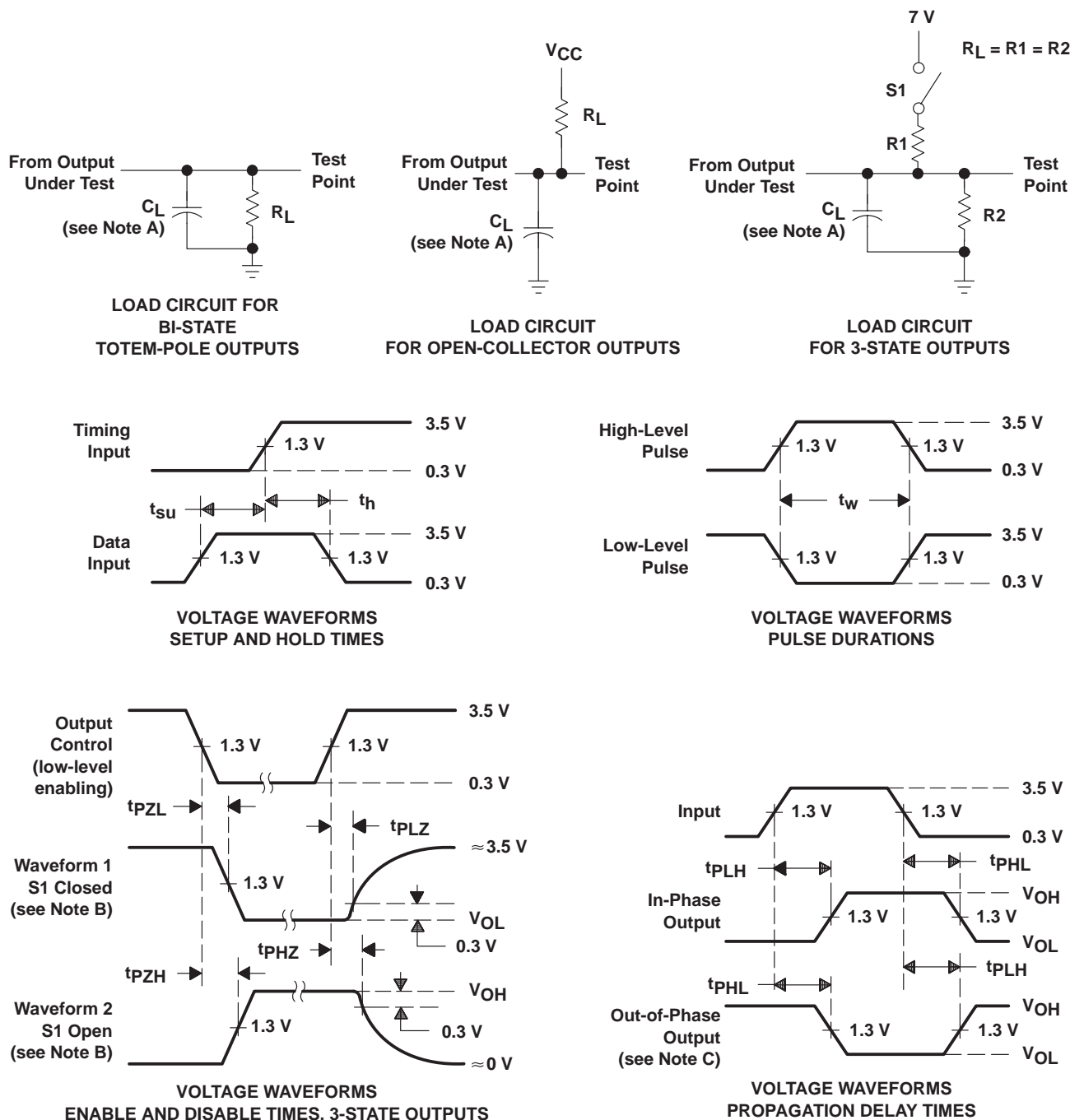
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R1 = R2 = 500 Ω, T _A = MIN to MAX† | | | | UNIT |
|------------------|--------------------------|------------------------|------------------------------------------------------------------------------------------------------------------|-----|-------------|-----|------|
| | | | SN54ALS193 | | SN74ALS193A | | |
| | | | MIN | MAX | MIN | MAX | |
| f _{max} | | | 25 | | 30 | | MHz |
| t _{PLH} | UP | $\overline{\text{CO}}$ | 3 | 20 | 3 | 16 | ns |
| t _{PHL} | | | 3 | 21 | 5 | 18 | |
| t _{PLH} | DOWN | $\overline{\text{BO}}$ | 4 | 20 | 4 | 16 | ns |
| t _{PHL} | | | 5 | 22 | 5 | 18 | |
| t _{PLH} | UP or DOWN | Any Q | 4 | 27 | 3 | 19 | ns |
| t _{PHL} | | | 4 | 23 | 4 | 17 | |
| t _{PLH} | $\overline{\text{LOAD}}$ | Any Q | 8 | 38 | 7 | 30 | ns |
| t _{PHL} | | | 8 | 37 | 8 | 28 | |
| t _{PHL} | CLR | Any Q | 5 | 20 | 5 | 17 | ns |

† For conditions shown MIN or MAX, use the appropriate value specified under recommended operating conditions.

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PARAMETER MEASUREMENT INFORMATION SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - When measuring propagation delay items of 3-state outputs, switch S1 is open.
 - All input pulses have the following characteristics: $PRR \leq 1$ MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.
 - The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

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