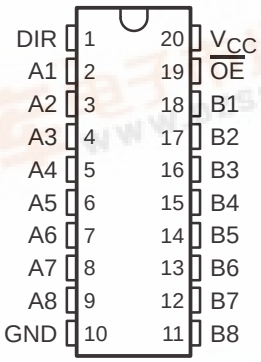
# SN74ALS1640A, SN74ALS1645A
# OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SDAS246B – DECEMBER 1982 – REVISED FEBRUARY 1997

- **Bidirectional Bus Transceivers in High-Density 20-Pin Packages**
- **Lower-Power Versions of SN74ALS640B and SN74ALS645A**
- **Package Options Include Plastic Small-Outline (DW) Packages and Standard Plastic (N) 300-mil DIPs**

**DW OR N PACKAGE**
**(TOP VIEW)**




## description

These octal bus transceivers are designed for asynchronous two-way communication between data buses. These devices transmit data from the A bus to the B bus or from the B bus to the A bus, depending on the level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input can be used to disable the device so that the buses are effectively isolated. The SN74ALS1640A features inverting logic, while the SN74ALS1645A features noninverting logic.

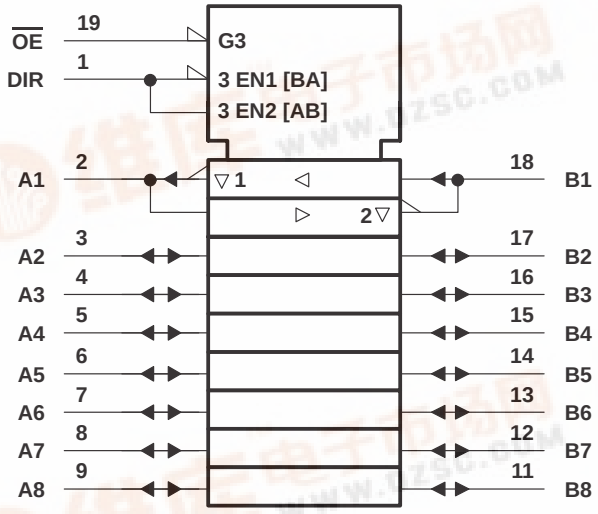
The SN74ALS1640A and SN74ALS1645A are characterized for operation from 0°C to 70°C.

**FUNCTION TABLE**

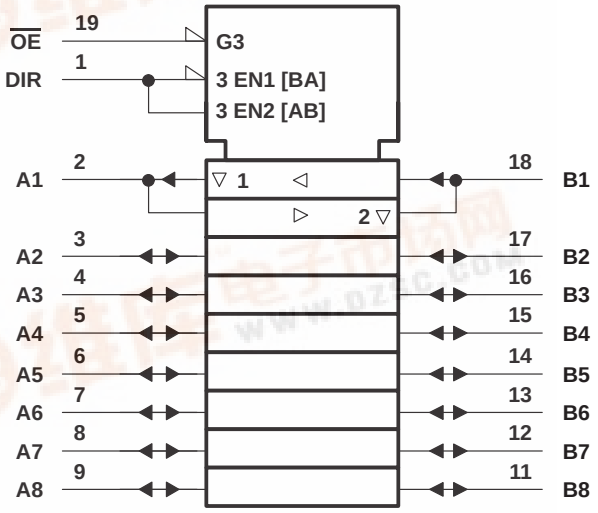
| INPUTS | | OPERATION | |
|---|---|---|---|
| $\overline{OE}$ | DIR | SN74ALS1640A | SN74ALS1645A |
| L | L | $\overline{B}$ data to A bus | B data to A bus |
| L | H | $\overline{A}$ data to B bus | A data to B bus |
| H | X | Isolation | Isolation |

## logic symbols†

**SN74ALS1640A**




**SN74ALS1645A**




† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

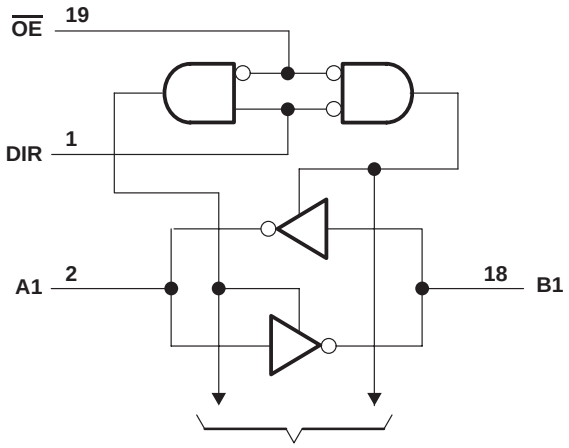
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



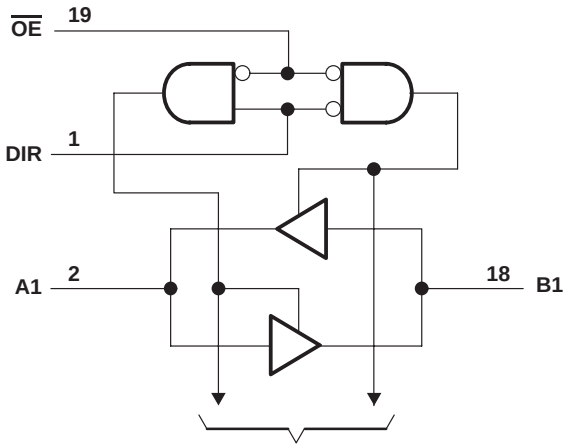
TEXAS INSTRUMENTS

## logic diagrams (positive logic)

**SN74ALS1640A**




**SN74ALS1645A**




## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, $V_{CC}$ . . . . . 7 V
Input voltage, $V_I$: All inputs . . . . . 7 V
I/O ports . . . . . 5.5 V
Package thermal impedance, $\theta_{JA}$ (see Note 1): DW package . . . . . 97°C/W
N package . . . . . 67°C/W
Storage temperature range, $T_{stg}$ . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51, except for through-hole packages, which use a trace length of zero.

## recommended operating conditions

| | | SN74ALS1640A SN74ALS1645A | | | UNIT |
|---|---|---|---|---|---|
| | | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $I_{OH}$ | High-level output current | | | –15 | mA |
| $I_{OL}$ | Low-level output current | | | 16 | mA |
| $T_A$ | Operating free-air temperature | 0 | | 70 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | SN74ALS1640A SN74ALS1645A | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP† | MAX | |
| $V_{IK}$ | | $V_{CC}$ = 4.5 V, | $I_I$ = –18 mA | | | –1.5 | V |
| $V_{OH}$ | | $V_{CC}$ = 4.5 V to 5.5 V, | $I_{OH}$ = –0.4 mA | $V_{CC}$–2 | | | V |
| | | $V_{CC}$ = 4.5 V | $I_{OH}$ = –3 mA | 2.4 | 3.2 | | |
| | | | $I_{OH}$ = –15 mA | 2 | | | |
| $V_{OL}$ | | $V_{CC}$ = 4.5 V | $I_{OL}$ = 8 mA | | 0.25 | 0.4 | V |
| | | | $I_{OL}$ = 16 mA | | 0.35 | 0.5 | |
| $I_I$ | Control inputs | $V_{CC}$ = 5.5 V | $V_I$ = 7 V | | | 0.1 | mA |
| | A or B ports | | $V_I$ = 5.5 V | | | 0.1 | |
| $I_{IH}$ | Control inputs | $V_{CC}$ = 5.5 V, | $V_I$ = 2.7 V | | | 20 | µA |
| | A or B ports‡ | | | | | 20 | |
| $I_{IL}$ | Control inputs | $V_{CC}$ = 5.5 V, | $V_I$ = 0.4 V | | | –0.1 | mA |
| | A or B ports‡ | | | | | –0.1 | |
| $I_O$§ | | $V_{CC}$ = 5.5 V, | $V_O$ = 2.25 V | –30 | | –112 | mA |
| $I_{CC}$ | SN74ALS1640A | $V_{CC}$ = 5.5 V | | | 18 | 32 | mA |
| | SN74ALS1645A | $V_{CC}$ = 5.5 V | | | 25 | 38 | |

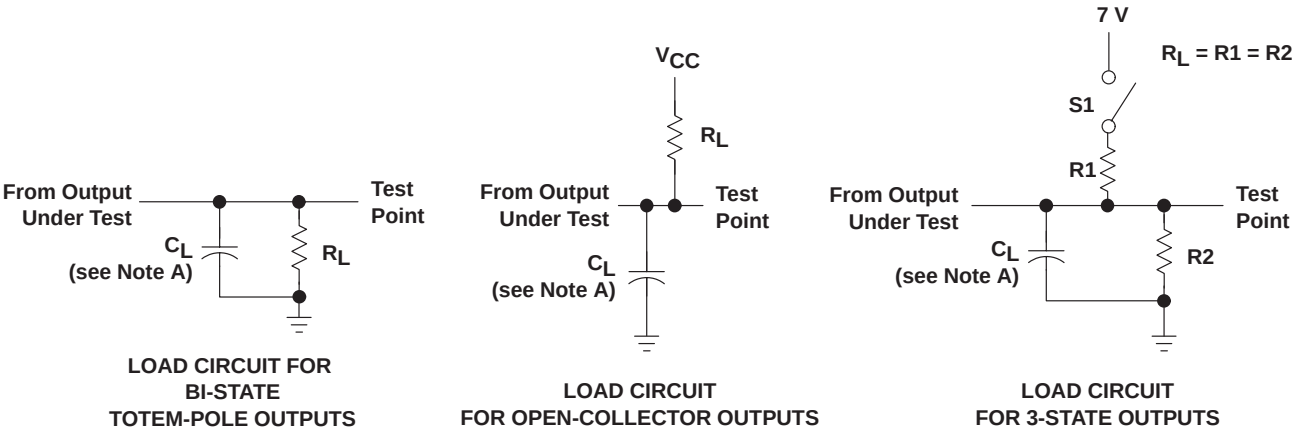
† All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
‡ For I/O ports, the parameters $I_{IH}$ and $I_{IL}$ include the off-state output current.
§ The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit output current, $I_{OS}$.

## switching characteristics (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 4.5 V to 5.5 V, $C_L$ = 50 pF, R1 = 500 Ω, R2 = 500 Ω, $T_A$ = MIN to MAX¶ | | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | SN74ALS1640A | | SN74ALS1645A | | |
| | | | MIN | MAX | MIN | MAX | |
| $t_{PLH}$ | A or B | B or A | 4 | 15 | 2 | 13 | ns |
| $t_{PHL}$ | | | 2 | 10 | 2 | 13 | |
| $t_{PZH}$ | $\overline{OE}$ | A or B | 5 | 20 | 8 | 25 | ns |
| $t_{PZL}$ | | | 5 | 22 | 8 | 25 | |
| $t_{PHZ}$ | $\overline{OE}$ | A or B | 2 | 10 | 2 | 12 | ns |
| $t_{PLZ}$ | | | 5 | 13 | 3 | 18 | |

¶ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

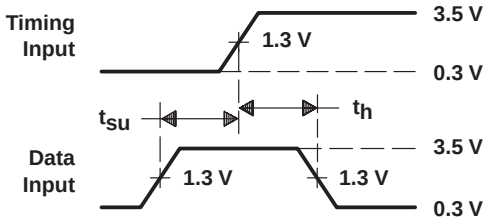
## PARAMETER MEASUREMENT INFORMATION
## SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



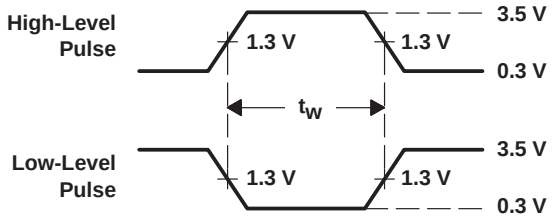

LOAD CIRCUIT FOR BI-STATE TOTEM-POLE OUTPUTS

LOAD CIRCUIT FOR OPEN-COLLECTOR OUTPUTS

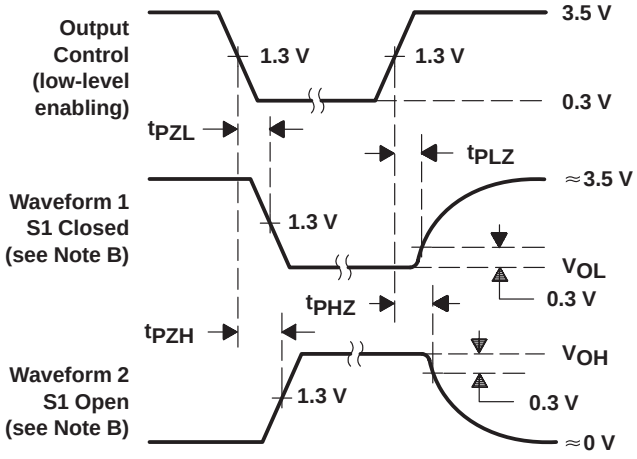
LOAD CIRCUIT FOR 3-STATE OUTPUTS



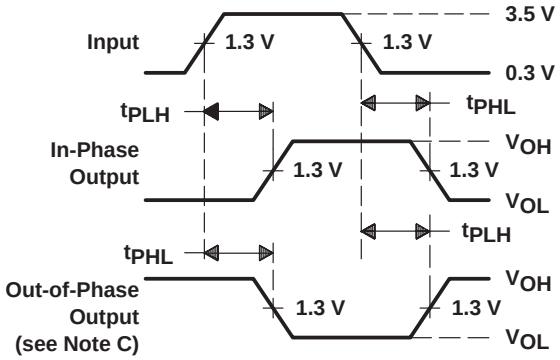

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
PULSE DURATIONS




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
D. All input pulses have the following characteristics: PRR ≤ 1 MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.
E. The outputs are measured one at a time with one transition per measurement.

**Figure 1. Load Circuits and Voltage Waveforms**

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