查询SN54F175供应商

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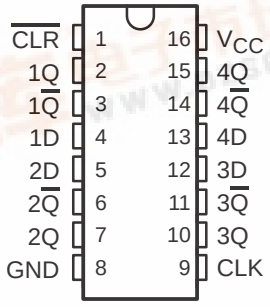
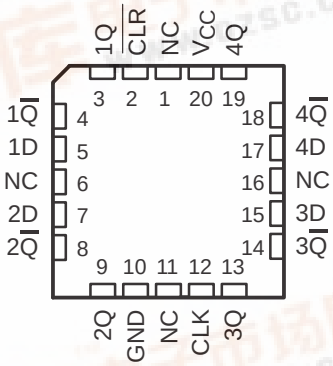
SDFS058A – D2932, MARCH 1987 – REVISED OCTOBER 1993

- **Contain Four Flip-Flops With Double-Rail Outputs**
- **Buffered Clock and Direct Clear Inputs**
- **Applications Include:**
  - **Buffer/Storage Registers**
  - **Shift Registers**
  - **Pattern Generators**
- **Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

SN54F175 . . . J PACKAGE
SN74F175 . . . D OR N PACKAGE
(TOP VIEW)



SN54F175 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

These monolithic, positive-edge-triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic with a direct clear ($\overline{CLR}$) input. Information at the data (D) inputs meeting setup time requirements is transferred to outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock (CLK) input is at either the high or low level, the D-input signal has no effect at the output.

The SN54F175 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74F175 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

INPUTS			OUTPUTS	
$\overline{CLR}$	CLK	D	Q	$\overline{Q}$
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\overline{Q}_0$

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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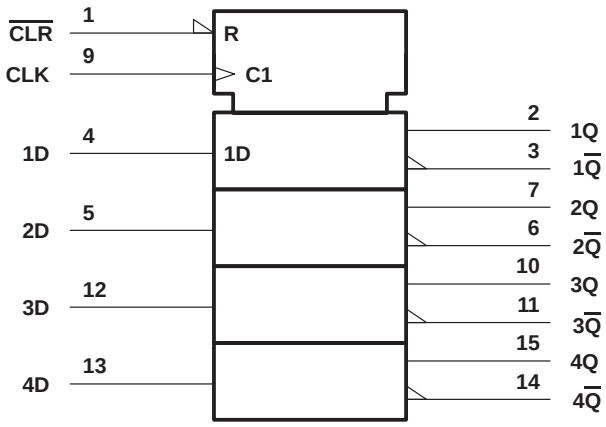
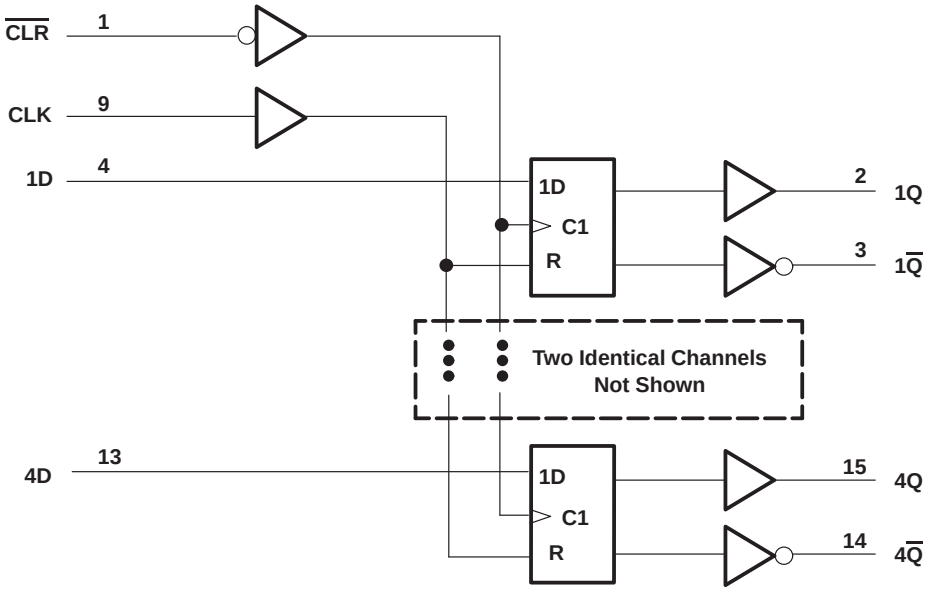
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



Pin numbers shown are for the D, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . . –1.2 V to 7 V
Input current range . . . . . –30 mA to 5 mA
Voltage range applied to any output in the high state . . . . . –0.5 V to V_{CC}
Current into any output in the low state . . . . . 40 mA
Operating free-air temperature range: SN54F175 . . . . . –55°C to 125°C
SN74F175 . . . . . 0°C to 70°C
Storage temperature range . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input voltage ratings may be exceeded provided the input current ratings are observed.

recommended operating conditions

		SN54F175			SN74F175			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{IK}	Input clamp current			–18			–18	mA
I_{OH}	High-level output current			– 1			– 1	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	–55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54F175			SN74F175			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = –18 mA			–1.2			–1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = – 1 mA	2.5	3.4		2.5	3.4		V
	V_{CC} = 4.75 V,	I_{OH} = – 1 mA				2.7			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.3	0.5		0.3	0.5	V
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	µA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.5 V			– 0.6			– 0.6	mA
I_{OS}§	V_{CC} = 5.5 V,	V_O = 0	–60		–150	–60		–150	mA
I_{CC}	V_{CC} = 5.5 V,	See Note 2		22.5	34		22.5	34	mA

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

NOTE 2: I_{CC} is measured with outputs open with 4.5 V applied to all data inputs after a momentary ground followed by 4.5 V applied to CLK.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			V_{CC} = 5 V, T_A = 25°C		SN54F175		SN74F175		UNIT
			′F175						
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	100	0	100	0	100	MHz
t_w	Pulse duration	CLK high	4		4		4		ns
		CLK low	5		5		5		
		$\overline{CLR}$ low	5		5		5		
t_{su}	Setup time, data before CLK↑	High or low	3		3		3		ns
	Setup time, inactive state, data before CLK↑†	$\overline{CLR}$ high	5		5		5		
t_h	Hold time, data after CLK↑	High or low	1		1		1		ns

† Inactive-state setup time is also referred to as recovery time.

switching characteristics (see Note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX‡				UNIT
			′F175			SN54F175		SN74F175		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			100	140		100		100		MHz
t_{PLH}	CLK	Q or $\overline{Q}$	3.2	4.6	6.5	2.7	8.5	3.2	7.5	ns
t_{PHL}			3.2	6.1	8.5	3.2	10.5	3.2	9.5	
t_{PLH}	$\overline{CLR}$	$\overline{Q}$	3.2	6.1	8.5	3.2	10	3.2	9	ns
t_{PHL}		Q	3.7	8.6	11.5	3.7	15	3.7	13	

‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
NOTE 3: Load circuits and waveforms are shown in Section 1.

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