#### 查询SN74F382供应商

## 捷多邦,专业PCB打样工厂,24小时加急出货 SN74F382 ARITHMETIC LOGIC UNIT/FUNCTION GENERATOR

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<ul> <li>Fully Parallel 4-Bit ALU in 20-Pin Package</li> <li>Ideally Suited for High-Density Economical</li> </ul>	DW OR N PACKAGE (TOP VIEW)
Processors	
<ul> <li>Ripple-Carry (C<sub>n+4</sub>) and Overflow (OVR)</li> </ul>	B1 2 19 A2
Outputs	A0 3 18 B2
<ul> <li>Arithmetic and Logic Operations Selected</li> </ul>	B0 [ 4 17 ] A3
Specifically to Simplify System	S0 5 16 B3
Implementation:	S1 [ 6 15 ] C <sub>n</sub>
A Minus B	S2 [] 7 14 ]] C <sub>n+4</sub>
B Minus A	F0 [ 8 13 ] OVR
A Plus B	F1 🛛 9 12 🕽 F3
Five Other Functions	GND [] 10 11 ]] F2
Package Options Include Plastic	
Small-Outline Packages and Standard	
Plastic 300-mil DIPs	
description	

#### description

The SN74F382 is an arithmetic logic unit (ALU)/function generator that performs eight binary arithmetic/logic operations on two 4-bit words as shown in the function table. The exclusive-OR, AND, and OR functions of the two Boolean variables are provided without the use of external circuits. In addition, the outputs can be cleared (low) or preset (high) as desired. The device provides a ripple-carry ( $C_{n+4}$ ) output to ripple the carry to the  $C_n$  input of the next stage. It detects and indicates the two's complement overflow condition via the overflow (OVR) output. OVR is logically equivalent to  $C_{n+3} \oplus C_{n+4}$ . When the SN74F382 is cascaded to handle word lengths longer than four bits in length, only the most significant OVR is used.

The SN74F382 is characterized for operation from 0°C to 70°C.

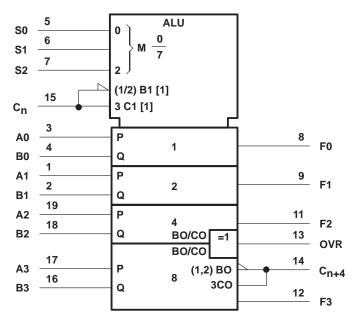
	FUNCTION TABLE								
SI	ELECTIC	<b>N</b>	ARITHMETIC/LOGIC						
S2	<b>S</b> 1	S0	OPERATION						
L	L	L	Clear						
L	-5.1	н	B minus A						
260	Н	L	A minus B						
L	Н	Н	A plus B						
н	L	L	$A \oplus B$						
н	L	Н	A + B						
н	Н	L	AB						
Н	Н	Н	Preset						



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	PIN DESIGNATIONS								
DESIGNATION	PIN NO.	FUNCTION							
A3, A2, A1, A0	17, 19, 1, 3	Word A inputs							
B3, B2, B1, B0	16, 18, 2, 4	Word B inputs							
S2, S1, S0	7, 6, 5	Function-select inputs							
C <sub>n</sub>	15	Carry input for addition, inverted carry input for subtraction							
F3, F2, F1, F0	12, 11, 9, 8	Function outputs							
C <sub>n+4</sub>	14	Ripple-carry output							
OVR	13	Overflow output							
V <sub>CC</sub>	20	Supply voltage							
GND	10	Ground							

## logic symbol<sup>†</sup>



<sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## function table

Certain differences exist in the OVR and  $C_{n+4}$  function table compared with similar parts from other technologies and other vendors. No differences exist in the arithmetic modes (B minus A, A minus B, and A plus B) where these outputs perform valuable cascade functions. There are slight differences in the other modes (clear, A + B, A  $\oplus$  B, AB, and preset), in which these outputs strictly *don't care*.

The following function table is a condensed version and assumes for  $A_n$  that A0, A1, A2, and A3 inputs all agree, and for  $B_n$  that B0, B1, B2, and B3 inputs all agree. This table is intended to point out the response of these OVR and  $C_{n+4}$  outputs in all modes of operation to facilitate incoming inspection.



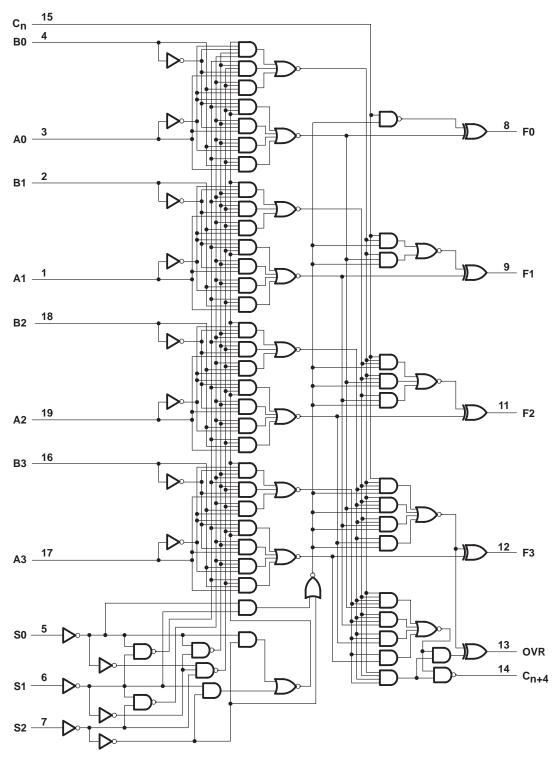
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Check nick         S2         S1         S0         Cn         An         Bn         F3         F2         F1         F0           Clear         L         L         L         X         X         X         L <th colspan="9">FUNCTION TABLE</th> <th></th>	FUNCTION TABLE												
OPERATION         S2         S1         S0         Cn         An         Bn         F3         F2         F1         F0           Clear         L         L         L         X         X         X         L         L         L         L         H         H         H         H         H         H         H         H         H         L	ARITHMETIC/LOGIC		INPUTS					OUTPUTS					<b>C</b> .
B minus A         L         L         L         L         H         H         H         H         L         L         L         L         L         L         L         L         L         L         H         H         H         H         L	OPERATION	S2	S1	S0	Cn	An	Bn	F3	F2	F1	F0		C <sub>n+4</sub>
B minus A         L         L         L         H         H         H         H         H         L	Clear	L	L	L	Х	Х	Х	L	L	L	L	Н	Н
B minus A         L         L         H         H         L					L							L	L
B minus A         L         L         H													н
B minus A       L       L       H       L													L
H         L         H         L <th< td=""><td>B minus A</td><td>L</td><td>L</td><td>Н</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td>н</td></th<>	B minus A	L	L	Н									н
A minus B         L         H         H         H         H         L													н
A minus B       L       H						н	L	L	L			L	L
A minus B       L       H       L       H       H       H       H       H       H       L					Н	н	Н	L	L	L	L	L	Н
A minus B         L         H         L         H													L
A minus B       L       H       L       H													L
A minus B       L       H       L       H       L       L       L       L       H       L       L       L       H       L       L       L       H       L													Н
H       L       H       L       L       L       H       H       L       H       L       H	A minus B	L	Н	L									L H
A plus B       L       H       L<													L
A plus B       L       H       L       H       H       H       H       H       L       L       L       H       H       H       H       L<													н
A plus B       L       H       H       H       H       H       H       H       H       H       H       H       L       L       L       L       L       L       L       H       H       H       H       H       H       H       L<					н	н	Н	L	L	L	L	L	н
A plus B       L       H       H       L       H       H       H       H       H       H       L<					L	L	L	L	L	L	L	L	L
A plus B       L       H       H       H       H       H       L <thl< th="">       L       <thl< th="">       L       <thl< th=""> <thl< td="" thr<=""><td></td><td></td><td></td><td></td><td>L</td><td>L</td><td>Н</td><td></td><td></td><td></td><td></td><td>L</td><td>L</td></thl<></thl<></thl<></thl<>					L	L	Н					L	L
A plus B       L       H       H       L       L       L       L       H       L       L       L       H       L       L       L       H       L <thl< th="">       L       <thl< th="">       L       <thl< th=""> <thl< td="" thr<=""><td></td><td rowspan="5">LH</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td>L</td></thl<></thl<></thl<></thl<>		LH											L
Image: Control of the state of the stat	A plus B		н	Н									н
H       H       L												L H	
H         H         H         H         H         H         L         L           X         L													Н
													н
					Х	L	L	L	L	L		L	L
					х	L	Н	н	Н	Н	Н	L	L
	$A \oplus B$	H L	L	L									L
													Н
								———					Н
													L
	A L R	ц		ц									L
	ATD		L										L
													Ĥ
						L		L			-		Н
					Х								L
	AB	Н	Н	L	Х		L						н
												L	
													Н
													L
	Presot	Ц	ц	ц									L
	FIESEL		п	п									L L
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## logic diagram (positive logic)





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#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, V <sub>CC</sub> Input voltage range, V <sub>I</sub> (see Note 1)	
Input current range	
Voltage range applied to any output in the high state	
Current into any output in the low state	40 mÅ
Operating free-air temperature range	0°C to 70°C
Storage temperature range	65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input voltage ratings may be exceeded provided the input current ratings are observed.

#### recommended operating conditions

		MIN	NOM	MAX	UNIT
VCC	Supply voltage	4.5	5	5.5	V
VIH	High-level input voltage	2			V
VIL	Low-level input voltage			0.8	V
IIK	Input clamp current			-18	mA
ЮН	High-level output current			- 1	mA
I <sub>OL</sub>	Low-level output current			20	mA
TA	Operating free-air temperature	0		70	°C

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		Т	TEST CONDITIONS			MAX	UNIT
VIK		$V_{CC} = 4.5 V,$	lı = – 18 mA			-1.2	V
Vou		$V_{CC} = 4.5 V,$	I <sub>OH</sub> = – 1 mA	2.5	3.4		V
VOH		V <sub>CC</sub> = 4.75 V,	I <sub>OH</sub> = – 1 mA	2.7	,		v
V <sub>OL</sub>		$V_{CC} = 4.5 V,$	I <sub>OL</sub> = 20 mA		0.3	0.5	V
Ц		V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = 7 V			0.1	mA
ЧН		V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = 2.7 V			20	μΑ
	Any A or B					- 2.4	
Ι <sub>ΙL</sub>	Any S	V <sub>CC</sub> = 5.5 V,	$V_{I} = 0.5 V$			- 0.6	mA
	Cn					- 3	
los§		V <sub>CC</sub> = 5.5 V,	$V_{O} = 0$	-60		-150	mA
Icc		V <sub>CC</sub> = 5.5 V,	See Note 2		54	81	mA

<sup>‡</sup> All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^{\circ}\text{C}$ .

§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

NOTE 2: ICC is measured with all outputs open, S0 and Cn inputs at 4.5 V, and all other inputs grounded.



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### switching characteristics (see Note 3)

PARAMETER FROM (INPUT)		TO (OUTPUT)	C R	V <sub>CC</sub> = 5 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 500 Ω, T <sub>A</sub> = 25°C			$V_{CC} = 4.5 V \text{ to } 5.5 V,$ $C_L = 50 \text{ pF},$ $R_L = 500 \Omega,$ $T_A = \text{MIN to MAX}^{\dagger}$		
			MIN	TYP	MAX	MIN	MAX	1	
<sup>t</sup> PLH	6	Amy E	2.3	5.3	11	2.3	12		
<sup>t</sup> PHL	C <sub>n</sub>	Any F	2.2	4.6	7.5	2.2	8.5	ns	
<sup>t</sup> PLH	Any Ann D	A mu E	2.7	6.9	12	2.4	13		
<sup>t</sup> PHL	Any A or B	Any F	2.5	6.1	10	2.3	11	ns	
<sup>t</sup> PLH	S0, S1, S2	A	4.7	8.3	15	4.3	17		
<sup>t</sup> PHL		Any F	3.3	7.5	14	3.3	15	ns	
<sup>t</sup> PLH	Anna Alen D		3.3	6.6	10	3.3	11		
<sup>t</sup> PHL	Any A or B	C <sub>n+4</sub>	3.4	6.3	10	3	10.5	ns	
<sup>t</sup> PLH	C0 C1 C0		3.6	9.8	16.5	3	17.5	ns	
<sup>t</sup> PHL	S0, S1, S2	OVR or C <sub>n+4</sub>	5	8.6	13	4.6	14	115	
<sup>t</sup> PLH	<u>^</u>		2.2	3.9	5.5	2	6.5		
<sup>t</sup> PHL	C <sub>n</sub>	C <sub>n+4</sub>	3	4.8	6.5	2.6	7.5	ns	
<sup>t</sup> PLH		0\/D	3.3	7	11	3	12.5		
<sup>t</sup> PHL	C <sub>n</sub>	OVR	3	5	6.5	3	8	ns	
<sup>t</sup> PLH	Any A or B	OVR	5.1	8.8	13	4.7	15		
<sup>t</sup> PHL		UVK	3.3	6.9	10.5	3.3	11.5	ns	

<sup>†</sup> For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions. NOTE 3: Load circuits and waveforms are shown in Section 1.



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