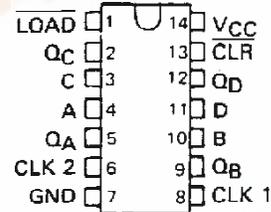SDLS077

SN54196, SN54197, SN54LS196, SN54LS197, SN54S196, SN54S197, SN74196, SN74197, SN74LS196, SN74LS197, SN74S196, SN74S197
50/30/100-MHz PRESETTABLE DECADE OR BINARY COUNTERS/LATCHES

OCTOBER 1976—REVISED MARCH 1988

- Performs BCD, Bi-Quinary, or Binary Counting

- Fully Programmable

- Fully Independent Clear Input

- Input Clamping Diodes Simplify System Design

- Output Q_A Maintains Full Fan-out Capability In Addition to Driving Clock-2 Input

TYPES	GUARANTEED COUNT FREQUENCY		TYPICAL POWER DISSIPATION
	CLOCK 1	CLOCK 2	
'196, '197	0-50 MHz	0-25 MHz	240 mW
'LS196, 'LS197	0-30 MHz	0-15 MHz	80 mW
'S196, 'S197	0-100 MHz	0-50 MHz	375 mW

description

These high-speed monolithic counters consist of four d-c coupled, master-slave flip-flops, which are internally interconnected to provide either a divide-by-two and a divide-by-five counter ('196, 'LS196, 'S196) or a divide-by-two and a divide-by-eight counter ('197, 'LS197, 'S197). These four counters are fully programmable; that is, the outputs may be preset to any state by placing a low on the count/load input and entering the desired data at the data inputs. The outputs will change to agree with the data inputs independent of the state of the clocks.

During the count operation, transfer of information to the outputs occurs on the negative-going edge of the clock pulse. These counters feature a direct clear which when taken low sets all outputs low regardless of the states of the clocks.

These counters may also be used as 4-bit latches by using the count/load input as the strobe and entering data at the data inputs. The outputs will directly follow the data inputs when the count/load is low, but will remain unchanged when the count/load is high and the clock inputs are inactive.

All inputs are diode-clamped to minimize transmission-line effects and simplify system design. These circuits are compatible with most TTL logic families. Series 54, 54LS, and 54S circuits are characterized for operation over the full military temperature range of −55°C to 125°C; Series 74, 74LS, and 74S circuits are characterized for operation from 0°C to 70°C.
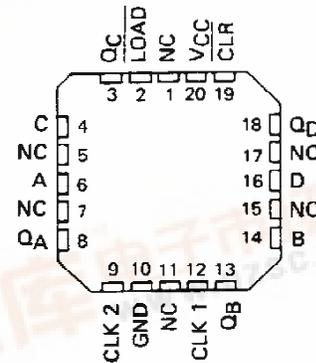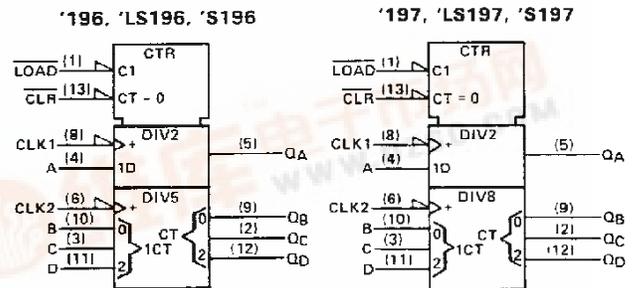
SN54196, SN54LS196, SN54S196,
SN54197, SN54LS197, SN54S197 . . . J OR W PACKAGE
SN74196, SN74197 . . . N PACKAGE
SN74LS196, SN74S196,
SN74LS197, SN74S197 . . . D OR N PACKAGE
(TOP VIEW)

LOAD	1	14	V_{CC}
Q_C	2	13	CLR
C	3	12	Q_D
A	4	11	D
Q_A	5	10	B
CLK 2	6	9	Q_B
GND	7	8	CLK 1

SN54LS196, SN54S196,
SN54LS197, SN54S197 . . . FK PACKAGE
(TOP VIEW)

Top pins: Q_C (3), LOAD (2), NC (1), V_{CC} (20), CLR (19)

C	4	18	Q_D
NC	5	17	NC
A	6	16	D
NC	7	15	NC
Q_A	8	14	B

Bottom pins: CLK 2 (9), GND (10), NC (11), CLK 1 (12), Q_B (13)

NC - No internal connection

logic symbols[†]

'196, 'LS196, 'S196

```
LOAD  (1)   CTR
            C1
CLR   (13)  CT = 0

CLK1  (8)   DIV2
A     (4)   +
            1D        (5)      QA

CLK2  (6)   DIV5
B     (10)  +         (9)      QB
C     (3)   CT        (2)      QC
D     (11)  1CT       (12)     QD
```

'197, 'LS197, 'S197

```
LOAD  (1)   CTR
            C1
CLR   (13)  CT = 0

CLK1  (8)   DIV2
A     (4)   +
            1D        (5)      QA

CLK2  (6)   DIV8
B     (10)  +         (9)      QB
C     (3)   CT        (2)      QC
D     (11)  1CT       (12)     QD
```

[†] These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, N, and W packages.

TEXAS
INSTRUMENTS
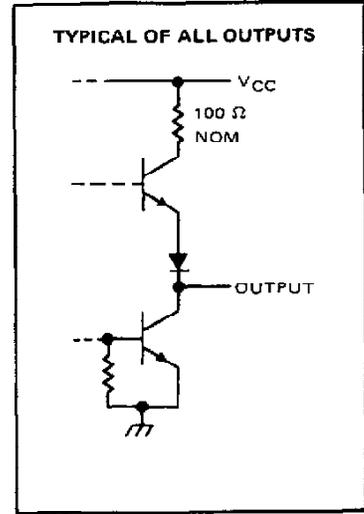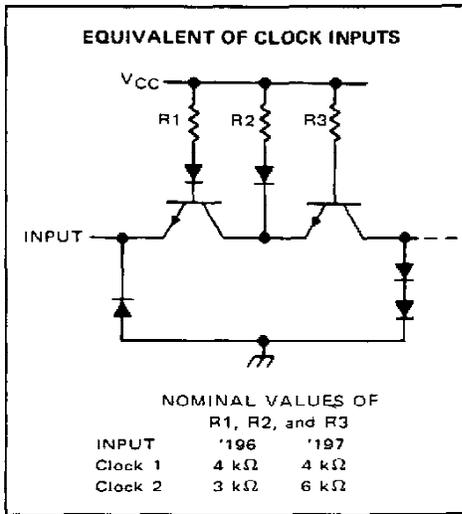POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

typical count configurations

'196, 'LS196, and 'S196 typical count configurations and function tables are the same as those for '176.
'197, 'LS197, and 'S197 typical count configurations and function tables are the same as those for '177.

logic diagrams

'196, 'LS196, and 'S196 logic diagrams are the same as those for '176.
'197, 'LS197, and 'S197 logic diagrams are the same as those for '177.

schematics of inputs and outputs

EQUIVALENT OF LOAD, CLEAR, AND DATA INPUTS

Count/load, Data: $R_{eq} = 4 \, k\Omega$ NOM
Clear: $R_{eq} = 2 \, k\Omega$ NOM

EQUIVALENT OF CLOCK INPUTS

NOMINAL VALUES OF R1, R2, and R3

INPUT	'196	'197
Clock 1	4 kΩ	4 kΩ
Clock 2	3 kΩ	6 kΩ

TYPICAL OF ALL OUTPUTS

100 Ω NOM

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . 7 V
Input voltage . . . . 5.5 V
Interemitter voltage (see Note 2) . . . . 5.5 V
Operating free-air temperature range: SN54196, SN54197 Circuits . . . . −55°C to 125°C
 SN74196, SN74197 Circuits . . . . 0°C to 70°C
Storage temperature range . . . . −65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor. For this circuit, this rating applies between the Clear and Load inputs.

recommended operating conditions

		SN54196, SN54197			SN74196, SN74197			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				−800			−800	µA
Low-level output current, I_{OL}				16			16	mA
Count frequency	Clock-1 input	0		50	0		50	MHz
	Clock-2 input	0		25	0		25	
Pulse width, t_w	Clock-1 input	10			10			ns
	Clock-2 input	20			20			
	Clear	15			15			
	Load	20			20			
Input hold time, t_h (see Note 3)	High-level data	$t_{w(load)}$			$t_{w(load)}$			ns
	Low-level data	$t_{w(load)}$			$t_{w(load)}$			
Input setup time, t_{su} (see Note 3)	High-level data	10			10			ns
	Low-level data	15			15			
Count enable time, t_{en} (see Note 4)		20			20			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

NOTES: 3. Setup and hold times are with respect to the falling edge of the load input.
4. Minimum count enable time is the interval immediately preceding the negative-going edge of the clock pulse during which interval the count/load and clear inputs must both be high to ensure counting.

SN54196, SN54197, SN74196, SN74197
50-MHz PRESETTABLE DECADE OR BINARY COUNTERS/LATCHES

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54196, SN74196			SN54197, SN74197			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH} High-level input voltage				2			2			V
V_{IL} Low-level input voltage						0.8			0.8	V
V_{IK} Input clamp voltage		V_{CC} = MIN, I_I = −12 mA				−1.5			−1.5	V
V_{OH} High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −800 μA		2.4	3.4		2.4	3.4		V
V_{OL} Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA¶			0.2	0.4		0.2	0.4	V
I_I Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V				1			1	mA
I_{IH} High-level input current	Data, Load	V_{CC} = MAX, V_I = 2.4 V				40			40	μA
	Clear, clock 1					80			80	
	Clock 2					120			80	
I_{IL} Low-level input current	Data, Load	V_{CC} = MAX, V_I = 0.4 V				−1.6			−1.6	mA
	Clear					−3.2			−3.2	
	Clock 1					−4.8			−4.8	
	Clock 2					−6.4			−3.2	
I_{OS} Short-circuit output current§		V_{CC} = MAX	SN54′	−20		−57	−20		−57	mA
			SN74′	−18		−57	−18		−57	
I_{CC} Supply current		V_{CC} = MAX, See Note 5			48	59		48	59	mA

NOTE 5: I_{CC} is measured with all inputs grounded and all outputs open.
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.
¶Q_A outputs are tested at I_{OL} = 16 mA plus the limit value of I_{IL} for the clock-2 input. This permits driving the clock-2 input while fanning out to 10 Series 54/74 loads.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER #	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54196 SN74196			SN54197 SN74197			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
f_{max}	Clock 1	Q_A	C_L = 15 pF, R_L = 400 Ω, See Note 6	50	70		50	70		MHz
t_{PLH}	Clock 1	Q_A			7	12		7	12	ns
t_{PHL}					10	15		10	15	
t_{PLH}	Clock 2	Q_B			12	18		12	18	ns
t_{PHL}					14	21		14	21	
t_{PLH}	Clock 2	Q_C			24	36		24	36	ns
t_{PHL}					28	42		28	42	
t_{PLH}	Clock 2	Q_D			14	21		36	54	ns
t_{PHL}					12	18		42	63	
t_{PLH}	A, B, C, D	Q_A, Q_B, Q_C, Q_D			16	24		16	24	ns
t_{PHL}					25	38		25	38	
t_{PLH}	Load	Any			22	33		22	33	ns
t_{PHL}					24	36		24	36	
t_{PHL}	Clear	Any			25	37		25	37	ns

#f_{max} ≡ maximum count frequency.
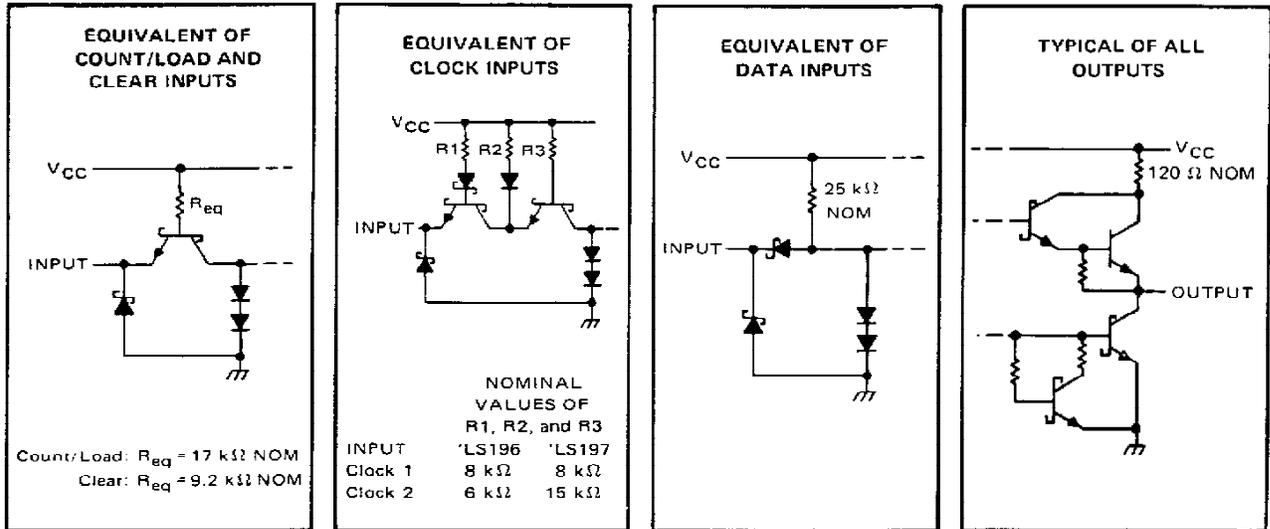t_{PLH} ≡ propagation delay time, low-to-high-level output.
t_{PHL} ≡ propagation delay time, high-to-low-level output.
NOTE 6: Load circuit, input conditions, and voltage waveforms are the same as those shown for the '176, '177 except that testing f_{max}, V_{IL} = 0.3 V.

schematics of inputs and outputs

| EQUIVALENT OF COUNT/LOAD AND CLEAR INPUTS | EQUIVALENT OF CLOCK INPUTS | EQUIVALENT OF DATA INPUTS | TYPICAL OF ALL OUTPUTS |

Count/Load: R_{eq} = 17 kΩ NOM
Clear: R_{eq} = 9.2 kΩ NOM

NOMINAL VALUES OF R1, R2, and R3

INPUT	'LS196	'LS197
Clock 1	8 kΩ	8 kΩ
Clock 2	6 kΩ	15 kΩ

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . 7 V
Input voltage . . . . 5.5 V
Operating free-air temperature range: SN54LS196, SN54LS197 Circuits . . . . −55°C to 125°C
                                       SN74LS196, SN74LS197 Circuits . . . . 0°C to 70°C
Storage temperature range . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

			SN54LS196, SN54LS197			SN74LS196, SN74LS197			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
I_{OH}	High-level output current				−400			−400	μA
I_{OL}	Low-level output current				4			8	mA
	Count frequency	Clock-1 input	0		30	0		30	MHz
		Clock-2 input	0		15	0		15	
t_w	Pulse width	Clock-1 input	20			20			ns
		Clock-2 input	30			30			
		Clear	15			15			
		Load	20			20			
t_h	Input hold time, (see Note 3)	High-level data	$t_{w(load)}$			$t_{w(load)}$			ns
		Low-level data	$t_{w(load)}$			$t_{w(load)}$			
t_{su}	Input setup time, (see Note 3)	High-level data	10			10			ns
		Low-level data	15			15			
t_{enable}	Count enable time, (see Note 4)	Clock 1	30			30			ns
		Clock 2	50			50			
T_A	Operating free-air temperature		−55		125	0		70	°C

NOTES: 3. Setup and hold times are with respect to the falling edge of the load input.
4. Minimum count enable time is the interval immediately preceding the negative-going edge of the clock pulse during which interval the count/load and clear inputs must both be high to ensure counting.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS[†]		SN54LS196 SN54LS197 MIN	TYP‡	MAX	SN74LS196 SN74LS197 MIN	TYP‡	MAX	UNIT
V_{IH} High-level input voltage				2			2			V
V_{IL} Low-level input voltage						0.7			0.8	V
V_{IK} Input clamp voltage		V_{CC} = MIN, I_I = −18 mA				−1.5			−1.5	V
V_{OH} High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = $V_{IL\,max}$, I_{OH} = −400 µA		2.5	3.4		2.7	3.4		V
V_{OL} Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = $V_{IL\,max}$	I_{OL} = 4 mA¶		0.25	0.4		0.25	0.4	V
			I_{OL} = 8 mA¶					0.35	0.5	
I_I Input current at maximum input voltage	Data, Load	V_{CC} = MAX, V_I = 5.5 V				0.1			0.1	mA
	Clear, clock 1					0.2			0.2	
	Clock 2 of 'LS196					0.4			0.4	
	Clock 2 of 'LS197					0.2			0.2	
I_{IH} High-level input current	Data, Load	V_{CC} = MAX, V_I = 2.7 V				20			20	µA
	Clear, clock 1					40			40	
	Clock 2 of 'LS196					80			80	
	Clock 2 of 'LS197					40			40	
I_{IL} Low-level Input current	Data, Load	V_{CC} = MAX, V_I = 0.4 V				−0.4			−0.4	mA
	Clear					−0.8			−0.8	
	Clock 1					−2.4			−2.4	
	Clock 2 of 'LS196					−2.8			−2.8	
	Clock 2 of 'LS197					−1.3			−1.3	
I_{OS} Short-circuit output current§		V_{CC} = MAX		−20		−100	−20		−100	mA
I_{CC} Supply current		V_{CC} = MAX, See Note 5		16		27	16		27	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.
¶Q_A outputs are tested at specified I_{OL} plus the limit value of I_{IL} for the clock-2 input. This permits driving the clock-2 input while maintaining full fan-out capability.
NOTE 5. I_{CC} is measured with all inputs grounded and all outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

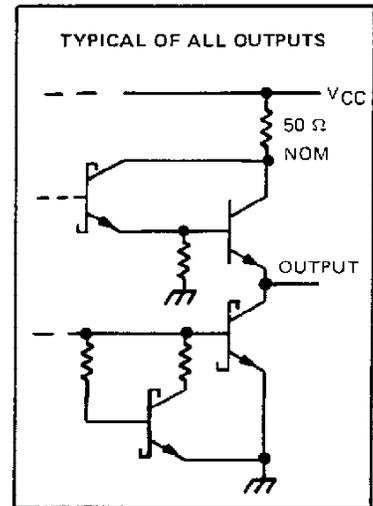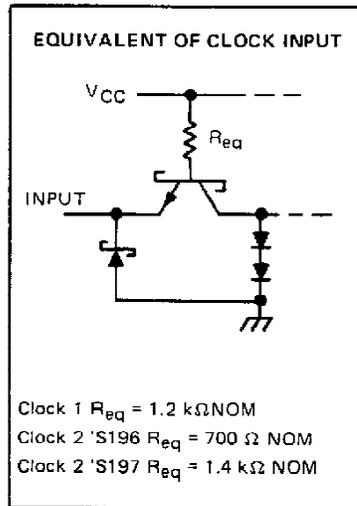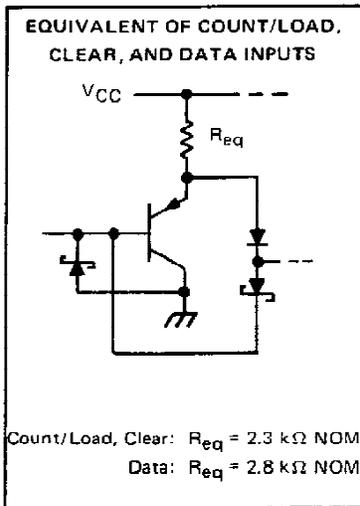| PARAMETER #	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54LS196 SN74LS196 MIN	TYP	MAX	SN54LS197 SN74LS197 MIN	TYP	MAX	UNIT
f_{max}	Clock 1	Q_A		30	40		30	40		MHz
t_{PLH}	Clock 1	Q_A			8	15		8	15	ns
t_{PHL}					13	20		14	21	
t_{PLH}	Clock 2	Q_B			16	24		12	19	ns
t_{PHL}					22	33		23	35	
t_{PLH}	Clock 2	Q_C	C_L = 15 pF, R_L = 2 kΩ, See Note 6		38	57		34	51	ns
t_{PHL}					41	62		42	63	
t_{PLH}	Clock 2	Q_D			12	18		55	78	ns
t_{PHL}					30	45		63	95	
t_{PLH}	A, B, C, D	Q_A, Q_B, Q_C Q_D			20	30		18	27	ns
t_{PHL}					29	44		29	44	
t_{PLH}	Load	Any			27	41		26	39	ns
t_{PHL}					30	45		30	45	
t_{PHL}	Clear	Any			34	51		34	51	ns

#f_{max} ≡ maximum count frequency.
t_{PLH} ≡ propagation delay time, low-to-high-level output, t_{PHL} ≡ propagation delay time, high-to-low-level output.
NOTE 6: Load circuit, input conditions, and voltage waveforms are the same as those shown for the '176, '177 except that t_r ≤ 15 ns, t_f ≤ 6 ns, and V_{ref} = 1.3 V (as opposed to 1.5 V).

schematics of inputs and outputs

EQUIVALENT OF COUNT/LOAD, CLEAR, AND DATA INPUTS	EQUIVALENT OF CLOCK INPUT	TYPICAL OF ALL OUTPUTS

Count/Load, Clear: R_{eq} = 2.3 kΩ NOM
Data: R_{eq} = 2.8 kΩ NOM

Clock 1 R_{eq} = 1.2 kΩNOM
Clock 2 'S196 R_{eq} = 700 Ω NOM
Clock 2 'S197 R_{eq} = 1.4 kΩ NOM

50 Ω NOM

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . 7 V
Input voltage . . . . 5.5 V
Operating free-air temperature range: SN54S196, SN54S197 Circuits . . . . −55°C to 125°C
                         SN74S196, SN74S197 Circuits . . . . 0°C to 70°C
Storage temperature range . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54S196, SN54S197			SN74S196, SN74S197			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				−1			−1	mA
Low-level output current, I_{OL}				20			20	mA
Clock frequency	Clock-1 input	0		100	0		100	MHz
	Clock-2 input	0		50	0		50	
Pulse width, t_W	Clock-1 input	5			5			ns
	Clock-2 input	10			10			
	Clear	30			30			
	Load	5			5			
Input hold time, t_h (see Note 3)	High-level data	3↓			3↓			ns
	Low-level data	3↓			3↓			
Input setup time, t_{su} (see Note 3)	High-level data	6↓			6↓			ns
	Low-level data	6↓			6↓			
Count enable time, t_{en} (see Note 4)		12			12			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

NOTES: 3. Setup and hold times are with respect to the falling edge of the load input.
      4. Minimum count enable time is the interval immediately preceding the negative-going edge of the clock pulse during which interval the count/load and clear inputs must both be high to ensure counting.

SN54S196, SN54S197, SN74S196, SN74S197
100-MHz PRESETTABLE DECADE OR BINARY COUNTERS/LATCHES

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS †		SN54S196, SN74S196 MIN	TYP‡	MAX	SN54S197, SN74S197 MIN	TYP‡	MAX	UNIT
VIH				2			2			V
VIL						0.8			0.8	V
VIK		VCC = MIN, II = −18 mA				−1.2			−1.2	V
VOH		VCC = MIN, VIH = 2 V, VIL = 0.8 V, IOH = −1 mA	54S	2.5	3.4		2.5	3.4		V
			74S	2.7	3.4		2.7	3.4		
VOL		VCC = MIN, VIH = 2 V, VIL = 0.8 V, IOL = 20 mA¶				0.5			0.5	V
II		VCC = MAX, VI = 5.5 V				1			1	mA
IIH	Clock 1, clock 2	VCC = MAX, VI = 2.7 V				150			150	μA
	All other inputs					50			50	
IIL	Data, Load Clear	VCC = MAX, VI = 0.5V				−0.75			−0.75	mA
	Clock 1					−8			−8	mA
	Clock 2					−10			−6	mA
IOS§		VCC = MAX		−30		−110	−30		−110	mA
ICC		VCC = MAX, See Note 5	54S		75	110		75	110	mA
			74S		75	120		75	120	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at VCC = 5 V, TA = 25°C.
¶ QA outputs are tested at IOL = 20 mA plus the limit value of IIL for the clock-2 input. This permits driving the clock-2 input while fanning out to 10 Series 54S/74S loads.
§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.
NOTE 5: ICC is measured with all input grounded and all outputs open.

switching characteristics, VCC = 5 V, TA = 25°C

PARAMETER #	(FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54S196, SN74S196 MIN	TYP	MAX	SN54S197, SN74S197 MIN	TYP	MAX	UNIT
fmax	Clock 1	QA		100	140		100	140		MHz
tPLH	Clock 1	QA			5	10		5	10	ns
tPHL					6	10		6	10	
tPLH	Clock 2	QB			5	10		5	10	ns
tPHL					8	12		8	12	
tPLH	Clock 2	QC	RL = 280 Ω, CL = 15 pF, See Note 7		12	18		12	18	ns
tPHL					16	24		15	22	
tPLH	Clock 2	QD			5	10		18	27	ns
tPHL					8	12		22	33	
tPLH	A,B,C,D	QA,QB,QC,QD			7	12		7	12	ns
tPHL					12	18		12	18	
tPLH	Load	Any			10	18		10	18	ns
tPHL					12	18		12	18	
tPHL	Clear	Any			26	37		26	37	ns

#fmax = maximum count frequency.
tPLH = propagation delay time, low-to-high-level output.
tPHL = propagation delay time, high-to-low-level output.
NOTE 7: Load circuit, input conditions, and voltage waveforms are the same as those shown in Section 1.

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