

- Four J-K Flip-Flops in a Single Package . . . Can Reduce FF Package Count by 50%
- Common Positive-Edge-Triggered Clocks with Hysteresis . . . Typically 200 mV
- Fully Buffered Outputs
- Typical Clock Input Frequency . . . 45 MHz

description

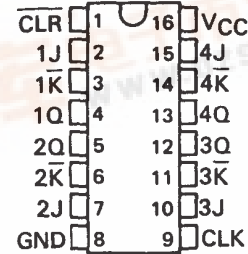
These quadruple TTL J-K flip-flops incorporate a number of third-generation IC features that can simplify system design and reduce flip-flop package count by as much as 50%. They feature hysteresis at the clock input, fully buffered outputs, and direct clear capability. The positive-edge-triggered SN54376 and SN74376 are directly compatible with most Series 54/74 MSI registers.

The SN54376 is characterized for operation over the full military temperature range of -55°C to 125°C; the SN74376 is characterized for operation from 0°C to 70°C.

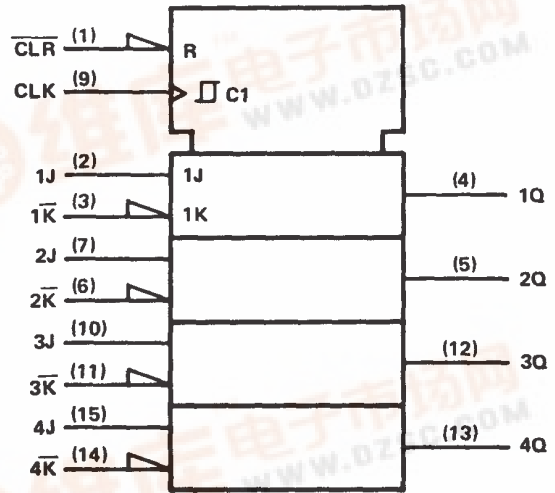
FUNCTION TABLE (EACH FLIP-FLOP)

COMMON INPUTS		INPUTS		OUTPUT
CLEAR	CLOCK	J	K	Q
L	X	X	X	L
H	↑	L	H	Q ₀
H	↑	H	H	H
H	↑	L	L	L
H	↑	H	L	TOGGLE
H	L	X	X	Q ₀

SN54376 . . . J PACKAGE
 SN74376 . . . N PACKAGE
 (TOP VIEW)

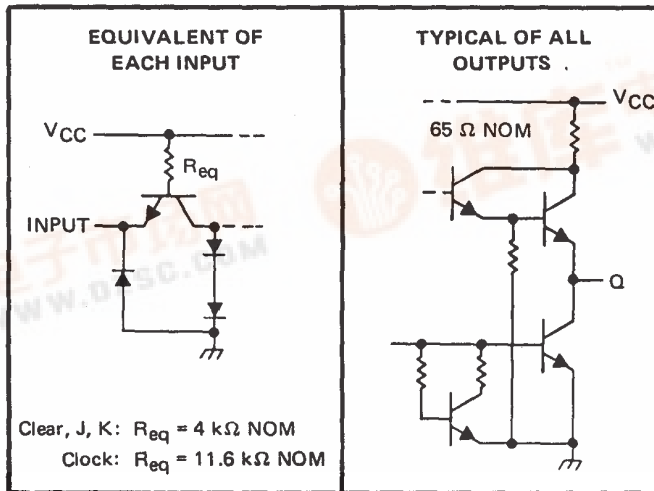


logic symbol



†This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.

schematics of inputs and outputs



Resistor values shown are nominal.



SN54376, SN74376 QUADRUPLE J-K FLIP-FLOPS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Operating free-air temperature range: SN54376	-55°C to 125°C
SN74376	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminals.

recommended operating conditions

	SN54376			SN74376			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-800			-800	μ A
Low-level output current, I_{OL}			16			16	mA
Clock frequency	0		30	0		30	MHz
Pulse width, t_w	Clock high	22		22			ns
	Clock low	12		12			
	Preset or clear low	12		12			
Setup time, t_{su}	J, K inputs	0†		0†			ns
	Clear inactive state	10†		10†			
Input hold time, t_h	20†			20†			ns
Operating free-air temperature, T_A	-55		125	0		70	°C

† The arrow indicates the edge of the clock pulse used for reference: † for the rising edge, ‡ for the falling edge.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V_{IH} High-level input voltage		2			V
V_{IL} Low-level input voltage				0.8	V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -12 \text{ mA}$			-1.5	V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OH} = -800 \mu\text{A}$	2.4	3.4		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OL} = 16 \text{ mA}$		0.2	0.4	V
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1	mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}, V_I = 2.4 \text{ V}$			40	μ A
I_{IL} Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			-1.6	mA
I_{OS} Short-circuit output current§	$V_{CC} = \text{MAX}$	-30		-85	mA
I_{CC} Supply current	$V_{CC} = \text{MAX}$		52	74	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max} Maximum clock frequency	$C_L = 15 \text{ pF}, R_L = 400 \Omega,$ See Note 2	30	45		MHz
t_{PHL} Propagation delay time, high-to-low-level output from clear			17	30	ns
t_{PLH} Propagation delay time, low-to-high-level output from clock			22	35	ns
t_{PHL} Propagation delay time, high-to-low-level output from clock			24	35	ns

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

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