

- Package Options Include Plastic "Small Outline" Packages, Flat Packages, and Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

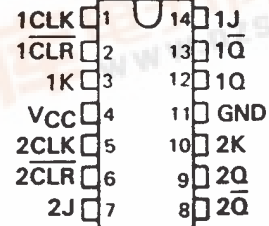
**description**

The '73, and 'H73, contain two independent J-K flip-flops with individual J-K, clock, and direct clear inputs. The '73, and 'H73, are positive pulse-triggered flip-flops. J-K input is loaded into the master while the clock is high and transferred to the slave on the high-to-low transition. For these devices the J and K inputs must be stable while the clock is high.

The 'LS73A contains two independent negative-edge-triggered flip-flops. The J and K inputs must be stable one setup time prior to the high-to-low clock transition for predictable operation. When the clear is low, it overrides the clock and data inputs forcing the Q output low and the  $\bar{Q}$  output high.

The SN5473, SN54H73, and the SN54LS73A are characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN7473, and the SN74LS73A are characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

SN5473, SN54LS73A . . . J OR W PACKAGE  
SN7473 . . . N PACKAGE  
SN74LS73A . . . D OR N PACKAGE  
(TOP VIEW)



'73  
FUNCTION TABLE

INPUTS				OUTPUTS	
CLR	CLK	J	K	Q	$\bar{Q}$
L	X	X	X	L	H
H	$\downarrow$	L	L	$Q_0$	$\bar{Q}_0$
H	$\downarrow$	H	L	H	L
H	$\downarrow$	L	H	L	H
H	$\downarrow$	H	H	TOGGLE	
H	$\downarrow$	H	H	TOGGLE	

'LS73A  
FUNCTION TABLE

INPUTS				OUTPUTS	
CLR	CLK	J	K	Q	$\bar{Q}$
L	X	X	X	L	H
H	$\downarrow$	L	L	$Q_0$	$\bar{Q}_0$
H	$\downarrow$	H	L	H	L
H	$\downarrow$	L	H	L	H
H	$\downarrow$	H	H	TOGGLE	
H	H	X	X	$Q_0$	$\bar{Q}_0$

FOR CHIP CARRIER INFORMATION,  
CONTACT THE FACTORY



# SN5473, SN54LS73A, SN7473, SN74LS73A DUAL J-K FLIP-FLOPS WITH CLEAR

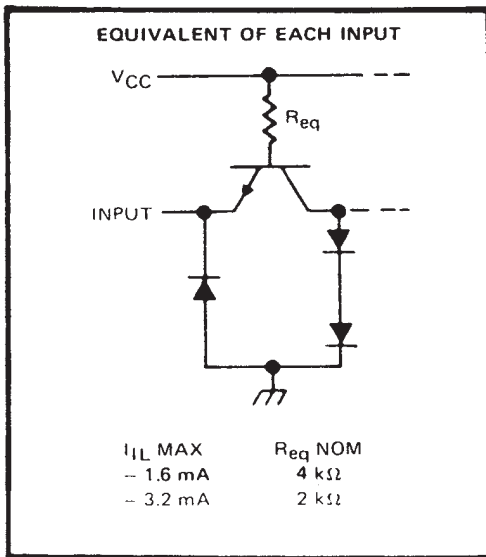
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## logic symbols†

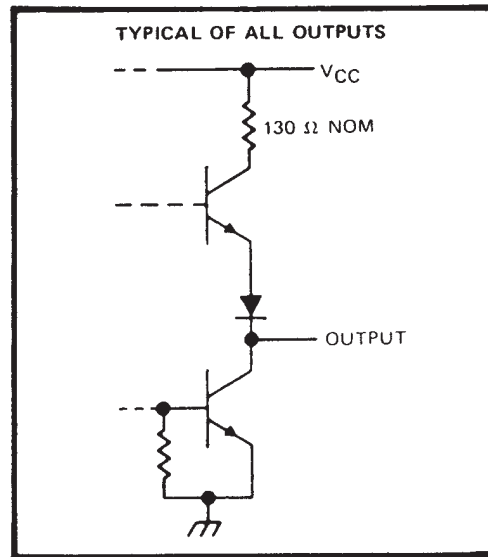


†These symbols are in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.

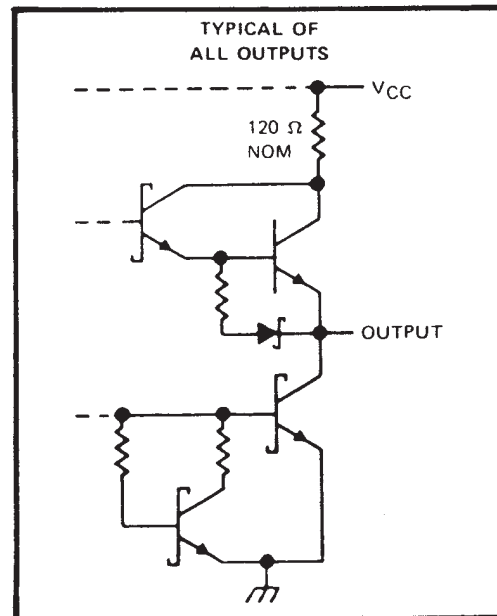
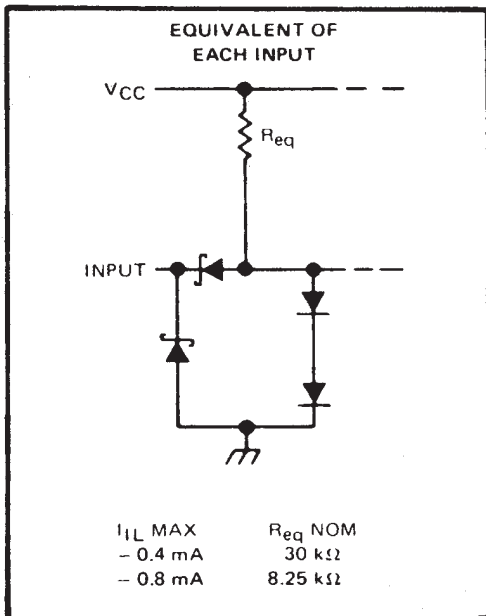
## schematics of inputs and outputs



'73



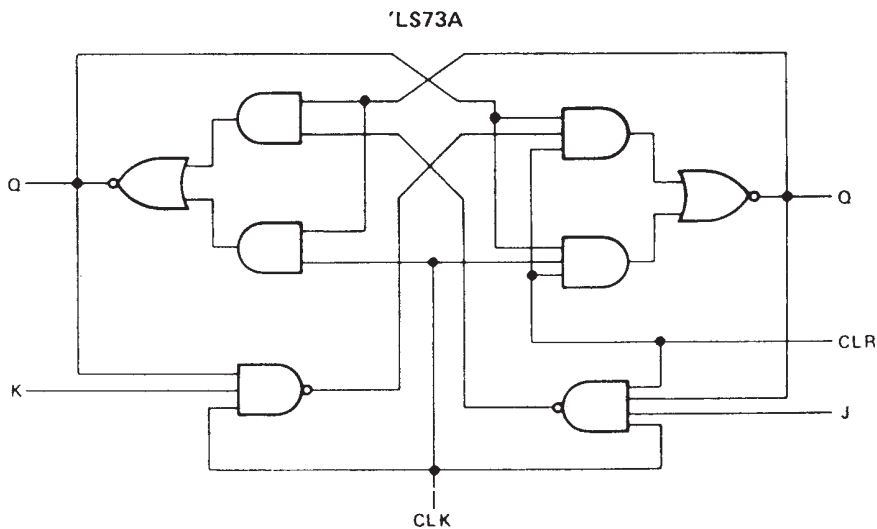
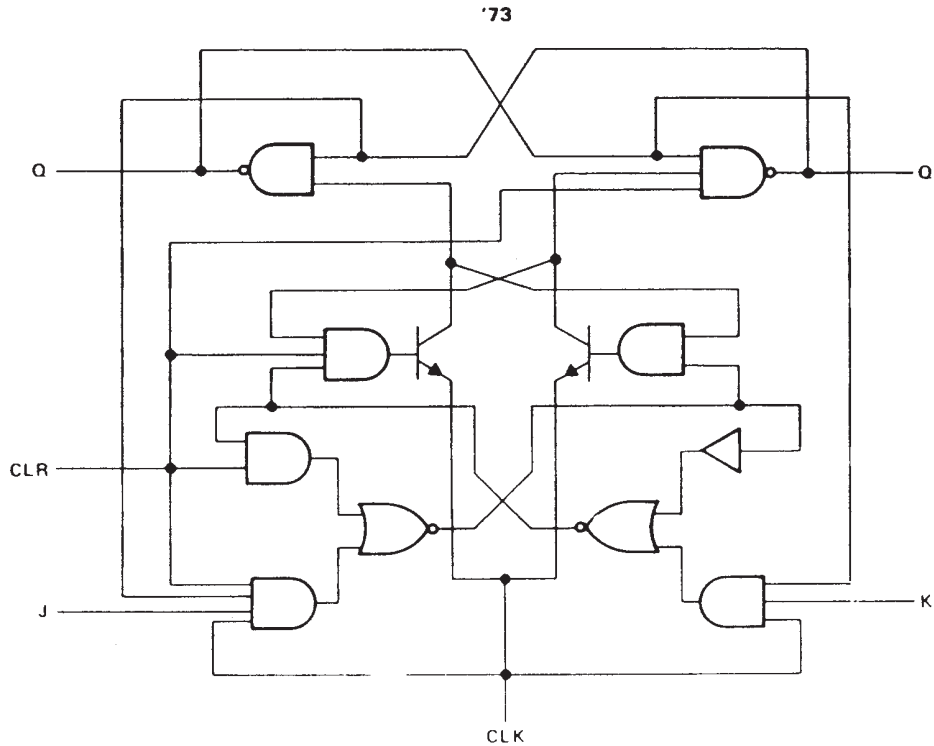
'LS73



# SN5473, SN54LS73A, SN7473, SN74LS73A DUAL J-K FLIP-FLOPS WITH CLEAR

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## logic diagrams (positive logic)



### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$ (See Note 1) .....	7 V
Input voltage: '73 .....	5.5 V
'LS73A .....	7 V
Operating free-air temperature range: SN54' .....	-55°C to 125°C
SN74' .....	0°C to 70°C
Storage temperature range .....	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

# SN5473, SN54LS73A, SN7473, SN74LS73A DUAL J-K FLIP-FLOPS WITH CLEAR

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## recommended operating conditions

		SN5473			SN7473			UNIT		
		MIN	NOM	MAX	MIN	NOM	MAX			
$V_{CC}$	Supply voltage	4.5	5	5.5	4.75	5	5.25	V		
$V_{IH}$	High-level input voltage	2			2			V		
$V_{IL}$	Low-level input voltage			0.8			0.8	V		
$I_{OH}$	High-level output current			-0.4			-0.4	mA		
$I_{OL}$	Low-level output current			16			16	mA		
$t_w$	Pulse duration	CLK high		20			20	ns		
		CLK low		47			47			
		$\overline{CLR}$ low		25			25			
$t_{su}$	Input setup time before CLK ↑			0			0	ns		
$t_h$	Input hold time data after CLK ↓			0			0	ns		
$T_A$	Operating free-air temperature			-55			125	0	70	°C

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN5473			SN7473			UNIT	
			MIN	TYP‡	MAX	MIN	TYP‡	MAX		
$V_{IK}$		$V_{CC} = \text{MIN}, I_I = -12 \text{ mA}$			-1.5			-1.5	V	
$V_{OH}$		$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OH} = -0.4 \text{ mA}$	2.4	3.4		2.4	3.4		V	
$V_{OL}$		$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OL} = 16 \text{ mA}$		0.2	0.4		0.2	0.4	V	
$I_I$		$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1			1	mA	
$I_{IH}$	J or K	$V_{CC} = \text{MAX}, V_I = 2.4 \text{ V}$			40			40	$\mu\text{A}$	
	$\overline{CLR}$ or CLK				80			80		
$I_{IL}$	J or K	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			-1.6			-1.6	mA	
	$\overline{CLR}$				-3.2			-3.2		
	CLK				-3.2			-3.2		
$I_{OS}§$		$V_{CC} = \text{MAX}$	-20		-57		-18		-57	mA
$I_{CC}¶$		$V_{CC} = \text{MAX}, \text{ See Note 2}$		10	20		10	20	mA	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at  $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$ .

§ Not more than one output should be shorted at a time.

¶ Average per flip-flop.

NOTE 2: With all outputs open,  $I_{CC}$  is measured with the Q and  $\overline{Q}$  outputs high in turn. At the time of measurement, the clock input is grounded.

## switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$ (see note 3)

PARAMETER#	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT	
$f_{max}$					15	20		MHz	
$t_{PLH}$	$\overline{CLR}$	$\overline{Q}$	$R_L = 400 \Omega,$	$C_L = 15 \text{ pF}$			16	25	ns
$t_{PHL}$		Q					25	40	ns
$t_{PLH}$	CLK	Q or $\overline{Q}$					16	25	ns
$t_{PHL}$							25	40	ns

#  $f_{max}$  = maximum clock frequency;  $t_{PLH}$  = propagation delay time, low-to-high-level output;  $t_{PHL}$  = propagation delay time, high-to-low-level output.

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

# SN5473, SN54LS73A, SN7473, SN74LS73A DUAL J-K FLIP-FLOPS WITH CLEAR

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## recommended operating conditions

		SN54LS73A			SN74LS73A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V <sub>CC</sub>	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V <sub>IH</sub>	High-level input voltage	2			2			V
V <sub>IL</sub>	Low-level input voltage	0.7			0.8			V
I <sub>OH</sub>	High-level output current	-0.4			-0.4			mA
I <sub>OL</sub>	Low-level output current	4			8			mA
f <sub>clock</sub>	Clock frequency	0	30		0	30		MHz
t <sub>w</sub>	Pulse duration	CLK high		20	20		ns	
		CLR low		25	20			
t <sub>su</sub>	Set up time-before CLK↓	data high or low		20	20		ns	
		CLR inactive		20	20			
t <sub>h</sub>	Hold time-data after CLK↓	0			0			ns
T <sub>A</sub>	Operating free-air temperature	-55	125		0	70		°C

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54LS73A			SN74LS73A			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V <sub>IK</sub>		V <sub>CC</sub> = MIN, I <sub>I</sub> = -18 mA	-1.5			-1.5			V
V <sub>OH</sub>		V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = MAX, I <sub>OH</sub> = -0.4 mA	2.5	3.4		2.7	3.4		V
V <sub>OL</sub>		V <sub>CC</sub> = MIN, V <sub>IL</sub> = MAX, V <sub>IH</sub> = 2 V, I <sub>OL</sub> = 4 mA	0.25 0.4			0.25 0.4			V
		V <sub>CC</sub> = MIN, V <sub>IL</sub> = MAX, V <sub>IH</sub> = 2 V, I <sub>OL</sub> = 8 mA				0.35 0.5			
I <sub>I</sub>	J or K	V <sub>CC</sub> = MAX, V <sub>I</sub> = 7 V	0.1			0.1			mA
	CLR		0.3			0.3			
	CLK		0.4			0.4			
I <sub>IH</sub>	J or K	V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.7 V	20			20			μA
	CLR		60			60			
	CLK		80			80			
I <sub>IL</sub>	J or K	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.4 V	-0.4			-0.4			mA
	CLR or CLK		-0.8			-0.8			
I <sub>OS</sub> §		V <sub>CC</sub> = MAX, See Note 4	-20	-100	-20	-100		mA	
I <sub>CC</sub> (Total)		V <sub>CC</sub> = MAX, See Note 2	4	6	4	6		mA	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

NOTE 2: With all outputs open, I<sub>CC</sub> is measured with the Q and Q̄ outputs high in turn. At the time of measurement, the clock input is grounded.

NOTE 4: For certain devices where state commutation can be caused by shorting an output to ground, an equivalent test may be performed with V<sub>O</sub> = 2.25 V and 2.125 V for the 54 family and the 74 family, respectively, with the minimum and maximum limits reduced to one half of their stated values.

## switching characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
f <sub>max</sub>			R <sub>L</sub> = 2 kΩ, C <sub>L</sub> = 15 pF		30	45		MHz
t <sub>PLH</sub>	CLR or CLK	Q or Q̄			15	20		ns
t <sub>PHL</sub>					15	20		ns

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

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