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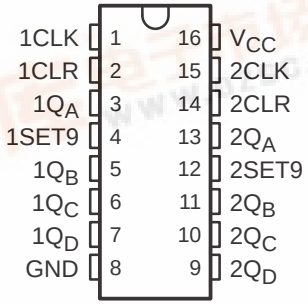
SN54LS490, SN74LS490
DUAL 4-BIT DECADE COUNTERS

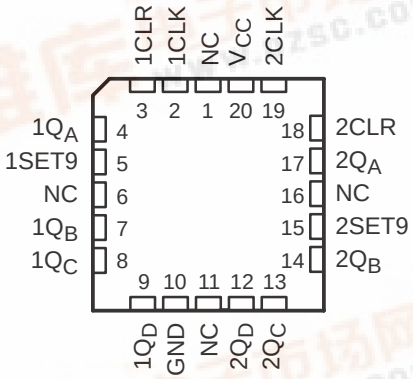
SDLS125A – OCTOBER 1976 – REVISED JULY 1998

- **Dual Versions of the SN54LS90 and SN74LS90 Counters**
- **Individual Clock, Direct Clear, and Set-to-9 Inputs for Each Decade Counter**
- **Dual Counters Can Significantly Improve System Densities as Package Count Can Be Reduced by 50%**
- **Maximum Count Frequency of 25 MHz . . . 35 MHz Typical**
- **Buffered Outputs Reduce Possibility of Collector Commutation**
- **Package Options Include Plastic Small-Outline (D) Packages, Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) DIPs**

SN54LS490 . . . J OR W PACKAGE
SN74LS490 . . . D OR N PACKAGE
(TOP VIEW)



SN54LS490 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

Each of these monolithic circuits contains eight master-slave flip-flops and additional gating to implement two individual 4-bit decade counters in a single package. Each decade counter has individual clock (1CLK, 2CLK), clear (1CLR, 2CLR), and set-to-9 (1SET9, 2SET9) inputs. BCD count sequences of any length up to divide-by-100 can be implemented with a single ’LS490 device. Buffering on each output is provided to significantly reduce susceptibility to collector commutation. All inputs are diode clamped to reduce the effects of line ringing. The counters have parallel outputs from each counter stage so that submultiples of the input count frequency are available for system timing signals.

The SN54LS490 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LS490 is characterized for use in industrial systems operating from 0°C to 70°C.

CLEAR/SET-TO-9 FUNCTION TABLE
(each counter)

INPUTS		OUTPUTS			
CLR	SET9	Q_A	Q_B	Q_C	Q_D
H	L	L	L	L	L
L	H	H	L	L	H
L	L	Count			

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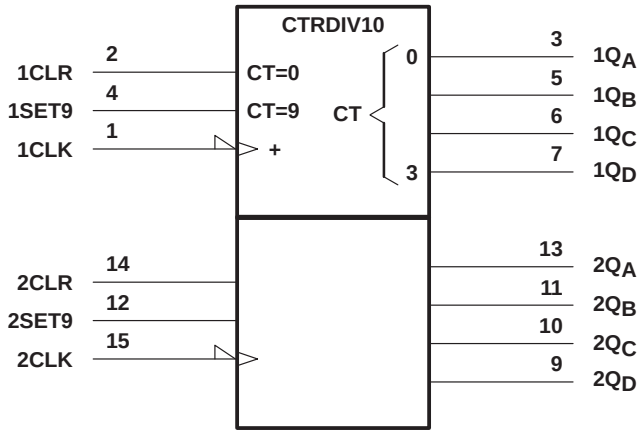
BCD COUNT SEQUENCE
(each counter)

COUNT	OUTPUTS			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

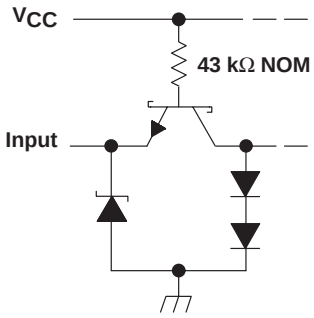
logic symbol†



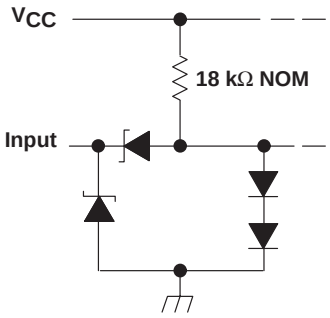
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, N, and W packages.

schematics of inputs and outputs

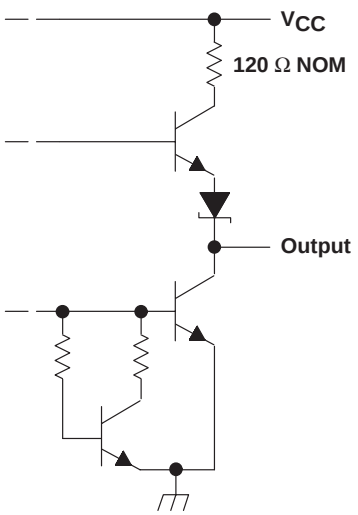
EQUIVALENT OF EACH CLK INPUT



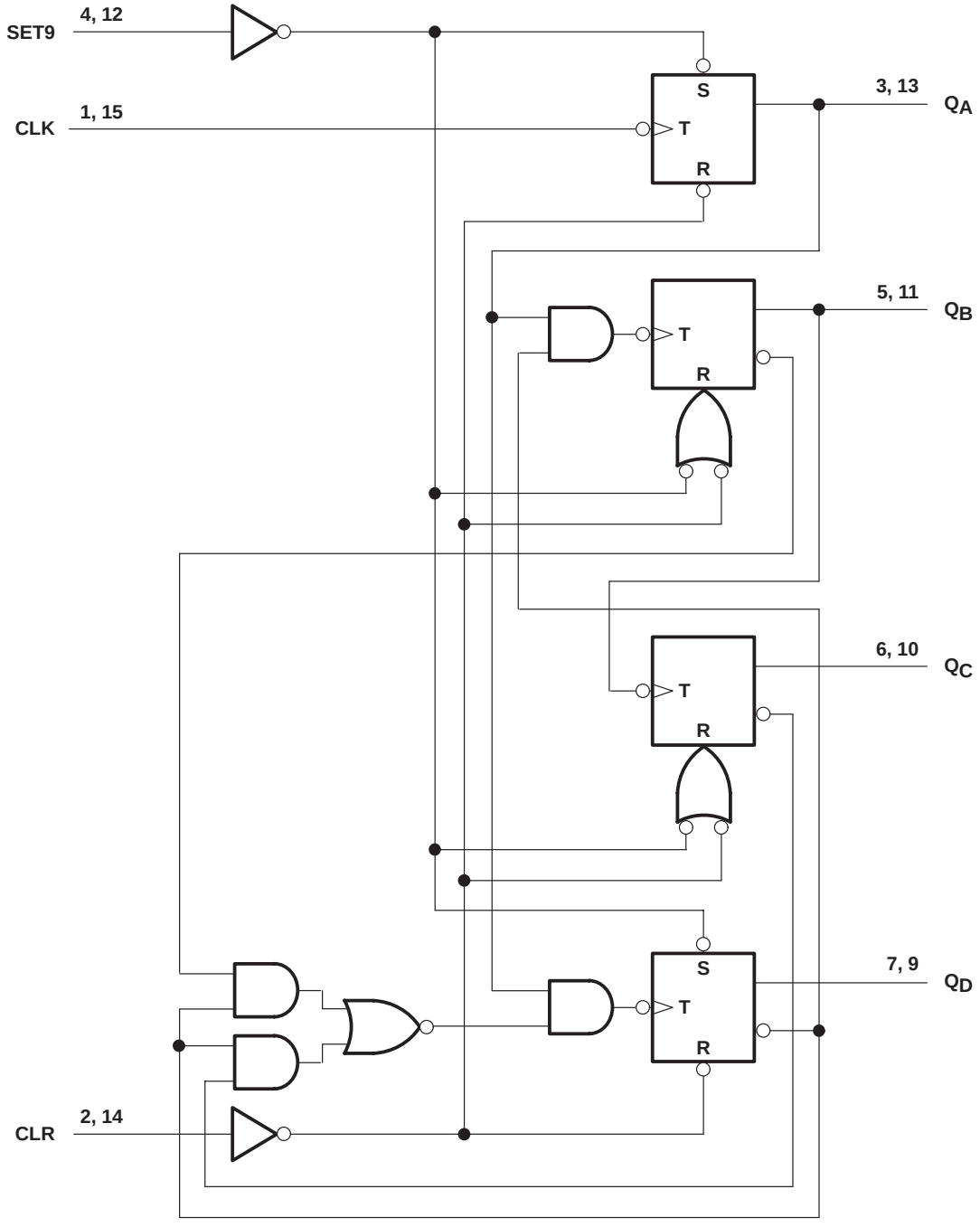
EQUIVALENT OF EACH CLR AND SET9 INPUT



TYPICAL OF ALL OUTPUTS



logic diagram (each counter)



Pin numbers shown are for the D, J, N, and W packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) . . . . . –0.5 V to 7 V
Clear and set-to-9 voltage . . . . . –0.5 V to 7 V
Clock input voltage . . . . . –0.5 V to 5.5 V
Package thermal impedance, θ_{JA} (see Note 2): D package . . . . . 113°C/W
N package . . . . . 78°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. Voltage values are with respect to network ground terminal.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

recommended operating conditions

		SN54LS490			SN74LS490			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
I_{OH}	High-level output current			–400			–400	μA
I_{OL}	Low-level output current			4			8	mA
f_{count}	Count frequency	0		25	0		25	MHz
t_w	Pulse width (any input)	20			20			ns
t_{su}	Clear or set-to-9 inactive-state setup time	25↓‡			25↓‡			ns
T_A	Operating free-air temperature	–55		125	0		70	°C

‡ The arrow (↓) indicates that the falling edge of the clock pulse is used for reference.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

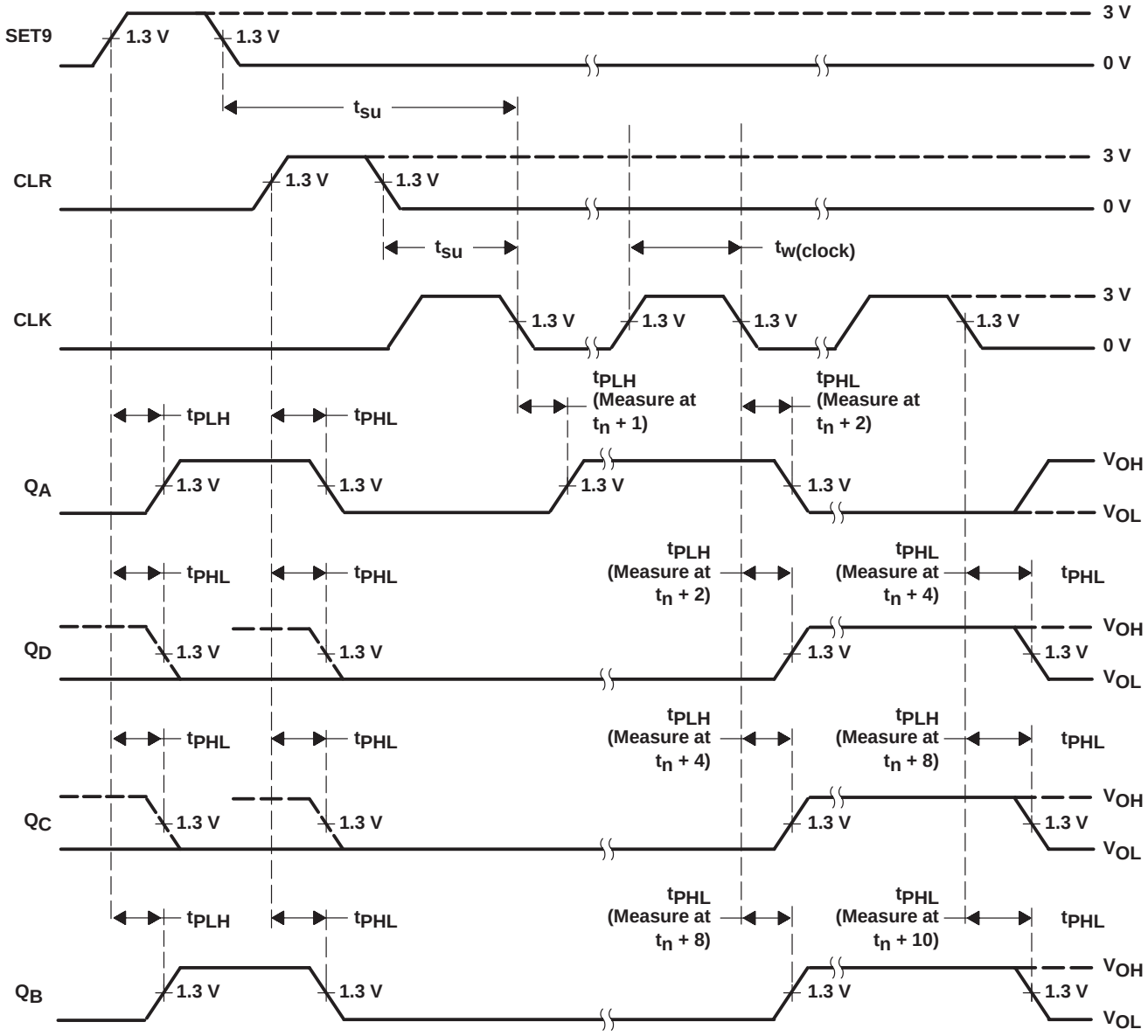
PARAMETER			TEST CONDITIONS†		SN74LS490			SN74LS490			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = –18 mA			–1.5			–1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL}max		2.5	3.4		2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL}max	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 8 mA					0.35	0.5	
I_I	Input current at maximum input voltage	CLR, SET9	V_{CC} = MAX,	V_I = 7 V			0.1			0.1	mA
		CLK	V_{CC} = MAX,	V_I = 5.5 V			0.2			0.2	
I_{IH}	High-level input current	CLR, SET9	V_{CC} = MAX,	V_I = 2.7 V			20			20	μA
		CLK					100			100	
I_{IL}	Low-level input current	CLR, SET9	V_{CC} = MAX,	V_I = 0.4 V			–0.4			–0.4	mA
		CLK					–1.6			–1.6	
I_{OS}§	Short-circuit output current		V_{CC} = MAX		–20		–100	–20		–100	mA
I_{CC}	Supply current		V_{CC} = MAX,	See Note 3		15	26		15	26	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.
NOTE 3: I_{CC} is measured with all outputs open, both CLR inputs grounded following momentary connection to 4.5 V, and all other inputs grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see Figures 1 and 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{max}	CLK	Q_A	C_L = 15 pF,	R_L = 2 kΩ	25	35		MHz
t_{PLH}	CLK	Q_A	C_L = 15 pF,	R_L = 2 kΩ		12	20	ns
t_{PHL}						13	20	
t_{PLH}	CLK	Q_B, Q_D	C_L = 15 pF,	R_L = 2 kΩ		24	39	ns
t_{PHL}						26	39	
t_{PLH}	CLK	Q_C	C_L = 15 pF,	R_L = 2 kΩ		32	54	ns
t_{PHL}						36	54	
t_{PHL}	CLR	Any	C_L = 15 pF,	R_L = 2 kΩ		24	39	ns
t_{PLH}	SET9	Q_A, Q_D	C_L = 15 pF,	R_L = 2 kΩ		24	39	ns
t_{PHL}		Q_B, Q_C				20	36	

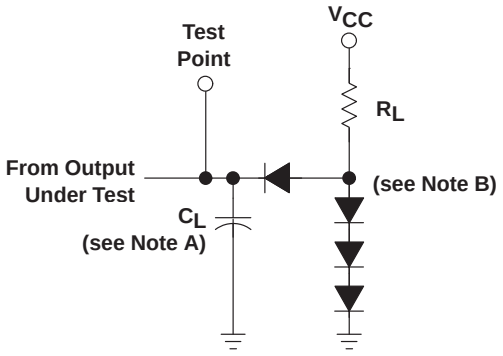
PARAMETER MEASUREMENT INFORMATION



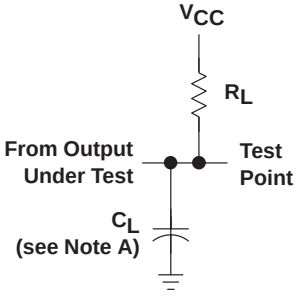
NOTE A: Input pulses are supplied by a generator having the following characteristics: $t_r \le 15$ ns, $t_f \le 6$ ns, PRR ≤ 1 MHz, duty cycle = 50%, $Z_O \approx 50\ \Omega$.

Figure 1. Voltage Waveforms

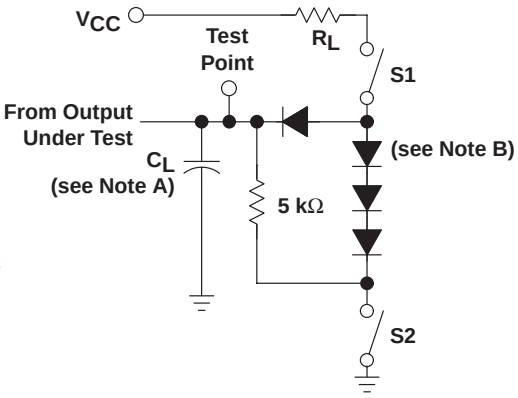
PARAMETER MEASUREMENT INFORMATION



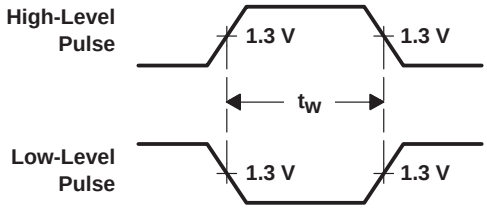
LOAD CIRCUIT FOR
BI-STATE
TOTEM-POLE OUTPUTS



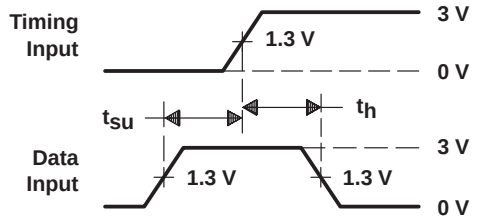
LOAD CIRCUIT
FOR OPEN-COLLECTOR OUTPUTS



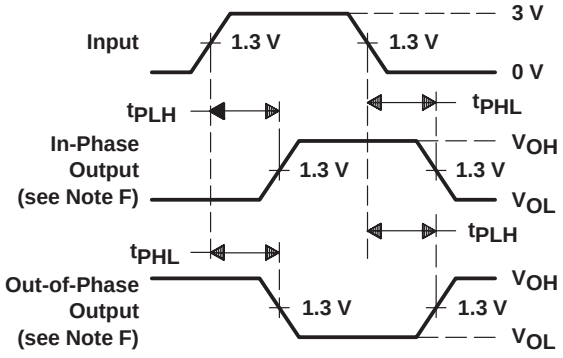
LOAD CIRCUIT
FOR 3-STATE OUTPUTS



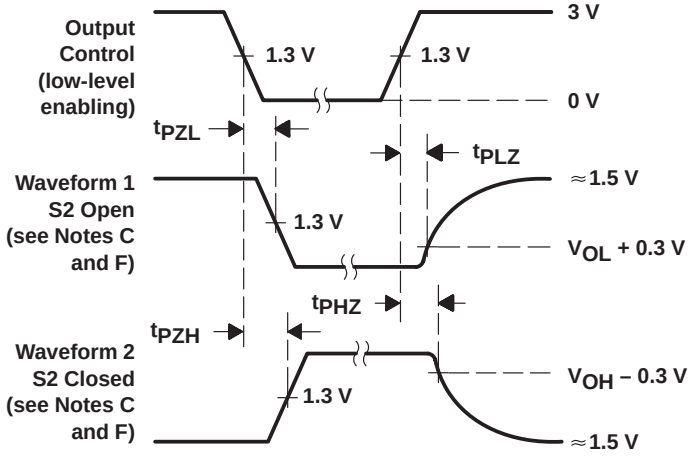
VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance.
B. All diodes are 1N3064 or equivalent.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.
E. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O \approx 50\ \Omega$, $t_r \le 15$ ns, $t_f \le 6$ ns.
F. S1 and S2 are closed for t_{PLH}, t_{PHL}, t_{PHZ}, and t_{PLZ}; S1 is open and S2 is closed for t_{PZH}; S1 is closed and S2 is open for t_{PZL}.
G. The outputs are measured one at a time with one input transition per measurement.

Figure 2. Load Circuits and Voltage Waveforms

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