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SN54LS375, SN74LS375 4-BIT BISTABLE LATCHES

SDLS166 OCTOBER 1976 - REVISED MARCH 1988

 Supply Voltage and Ground on Corner Pins To Simplify P-C Board Layout

description

The SN54LS375 and SN74LS375 bistable latches are electrically and functionally identical to the SN54LS75 and SN74LS75, respectively. Only the arrangement of the terminals has been changed in the SN54LS375 and SN74LS375.

These latches are ideally suited for use as temporary storage for binary information between processing units and input/output or indicator units. Information present at a data (D) input is transferred to the Q output when the enable (C) is high and the Q output will follow the data input as long as the enable remains high. When the enable goes low, the information (that was present at the data input a the time the transition occurred) is retained at the Q output until the enable goes high.

All inputs are diode-clamped to minimize transmissionline effects and simplify system design. The SN54LS375 is characterized for operation over the full military temperature range of – 55°C to 125°C; SN74LS375 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE (EACH LATCH)										
INPUTS OUTPUTS										
D	G	Q	ā							
L	н	L	н							
н	н	H	L							
x	L	Q ₀	<u>ō</u> 0							

 $\label{eq:H} H = high level, L = low level, X = irrelevant \\ Q_0 = the level of Q before the high-to low transition of C.$

logic symbol[†]

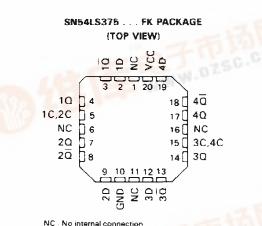
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1D_(1)	1D	
10,20 (4)	C1	(5) 10
· · · · ·	C2	2Q
2D_(7)	20	(6) 20
3D <u>(9)</u>	3D	(11) 30
3C,4C (12)	C3	(13) 30
L	C4	40
4D (15)	4D	(14) 40

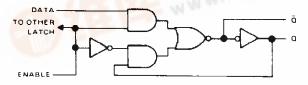
[†]This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, N. and W packages.

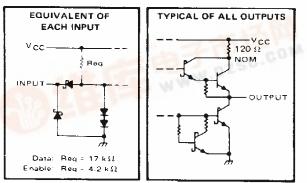
SN54L\$375 . . . J OR W PACKAGE SN74LS375 ... D OR N PACKAGE (TOP VIEW) 1D 10 5 4D 12 15 14 40 10 Π_3 10,20 13 40 Π4 12 3C,4C 20 Пs 20 6 11 30 2D 10 30 GND Π_8 9 🗋 3D



logic diagram (each latch)



schematics of inputs and outputs



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SN54LS375, SN74LS375 4-BIT BISTABLE LATCHES

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC (see Note 1)														
Input voltage				•	•	 -		-	-	•		•	7	v
Operating free-air temperature range:	SN54L5375												-55°C to 125°	°C
, c	SN74LS375												. 0°C to 70	°C
Storage temperature range														

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

			SN54LS375			SN74LS375				
		MIN	NOM	MAX	MIN	NOM	MAX			
Vcc	Supply voltage	4.5	5	5.5	4,75	5	5.25	V		
VIH	High-level input voltage	2			2			V		
VIL	Low-level input voltage			0.7	1		0.8	V		
юн	High-level output current			~ 0.4			- 0.4	mA		
IOL	Low-level output current			4			8	mA		
1 _W	Width of enabling pulse	20			20			ns		
setup	Setup time	20			20			ns		
Lhold	Hold time	0			0			ПS		
TA	Operating free-air temperature	- 55		125	0		70	°C		

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	TEST CONDITIONS T			SN54LS	375				
PARAMETER	TEST CONDI	MIN	TYP‡	MAX	MIN	TYP‡	MAX		
Vik	V _{CC} = MIN, 11 = -18 mA				-1.5			- 1.5	V
V _{OH}	$V_{CC} = MIN, V_{IH} = 2 V,$ $I_{OH} = -0.4 \text{ mA}$	V _{IL} = MAX	2.5	3.5	·	2.7	3.5		v
	$V_{CC} = MIN, V_{IH} = 2V,$	10L = 4 mA		0.25	0.4		0.25		
VOL	VIL = MAX	IOL = 8 mA					0.35	0.5	1 ×
		Dinput			0.1			0.1	mA
4	$V_{CC} = MAX$. $V_{I} = 7V$	Cinput			0.4			0.4	1
	Vcc = MAX Vi = 2.7 V	D input			20			20	
ЧΗ	V _{CC} = MAX V _I = 2.7 V	Cinput			80	<u> </u>		80	4 μA
		D input			- 0.4			- 0.4	mA
ΊL	$V_{CC} = MAX, V_{\parallel} = 0.4 V$	C input			- 16	<u> </u>		- 1.6	1
¹ 05 ;	VCC = MAX		-20		- 100	-20		- 100	mA
'CC	VCC = MAX. See Note 2			6.3	12		6.3	12	mA

f. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡] All typical values are at $V_{CC} = 5 V$, $T_A = 25 C$. § Not more than one output should be shorted at a time.

NOTE 2 ^{-1}CC is tested with all inputs grounded and all outputs open

switching characteristics, VCC = 5 V, TA = 25° C (see note 3)

PARAMETER	FROM (INPLIT)	TO {OUTPUT}	TEST CO		MIN TYP	MAX	UNIT
¹ PLH	D	0			15	27	
1PHL		Ŭ			9	17	ns
TPLH	 D	ā	$B_L = 2 k \Omega_c$	C _L ≃ 15 pF	12	20	ns
^t PHL			0 L 2 K34,	OL ISP	7	15	115
†₽LH					15	27	
^t PHL					14	25	ns
1PLH	с —	ā			16	30	
^t PHL	C				7	15	ns

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.



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