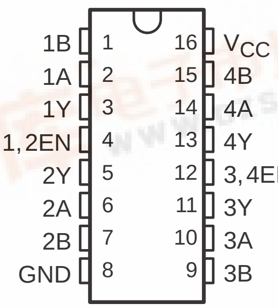
SN55LBC175
QUADRUPLE LOW-POWER DIFFERENTIAL LINE RECEIVER

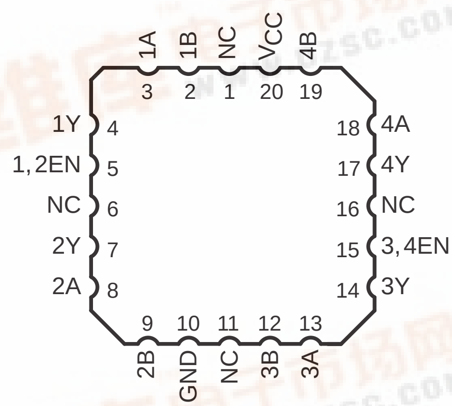
SGLS083A – MARCH 1995 – REVISED JUNE 2000

- **Meets EIA Standards RS-422-A, RS-423-A, RS-485, and CCITT V.11**
- **Designed to Operate With Pulse Durations as Short as 20 ns**
- **Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments**
- **Input Sensitivity . . . ±200 mV**
- **Low-Power Consumption . . . 20 mA Max**
- **Open-Circuit Fail-Safe Design**
- **Common-Mode Input Voltage Range of –7 V to 12 V**

J OR W PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

The SN55LBC175 is a monolithic quadruple differential line receiver with 3-state outputs and is designed to meet the requirements of the EIA Standards RS-422-A, RS-423-A, RS-485, and CCITT V.11. This device is optimized for balanced multipoint bus transmission at data rates up to and exceeding 10 million bits per second. The receivers are enabled in pairs with an active-high enable input. Each differential receiver input features high impedance, hysteresis for increased noise immunity, and sensitivity of ±200 mV over a common-mode input voltage range of 12 V to –7 V. Fail-safe design ensures that if the inputs are open-circuited, the outputs are always high. This device is designed using the Texas Instruments proprietary LinBiCMOS™ technology allowing low power consumption, high switching speeds, and robustness.

This device offers optimum performance when used with the SN55LBC174 quadruple line driver. The SN55LBC175 is available in the 16-pin CDIP (J) package, a 16-pin CPAK (W) package, or a 20-pin LCCC (FK) package.

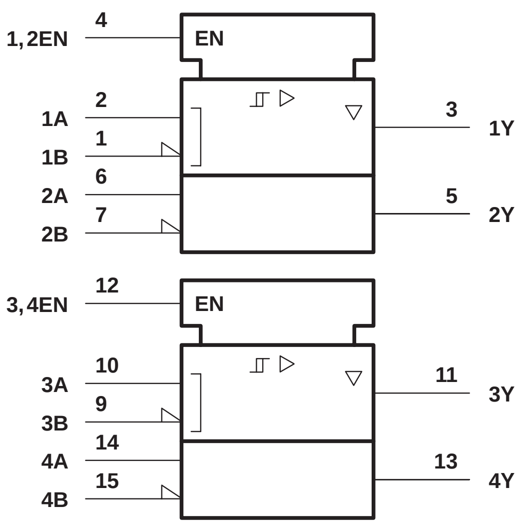
The SN55LBC175 is characterized over the military temperature range of –55°C to 125°C.

FUNCTION TABLE
(each receiver)

DIFFERENTIAL INPUTS A–B	ENABLE	OUTPUT Y
$V_{ID} \geq 0.2$ V	H	H
$-0.2\text{ V} < V_{ID} < 0.2$ V	H	?
$V_{ID} \leq -0.2$ V	H	L
X	L	Z
Open circuit	H	H

H = high level, L = low level, X = irrelevant,
Z = high impedance (off), ? = indeterminate

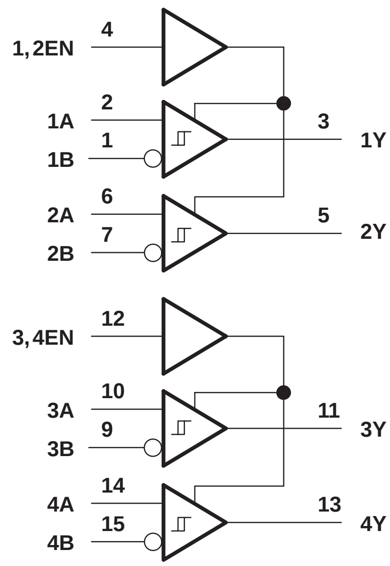
logic symbol†



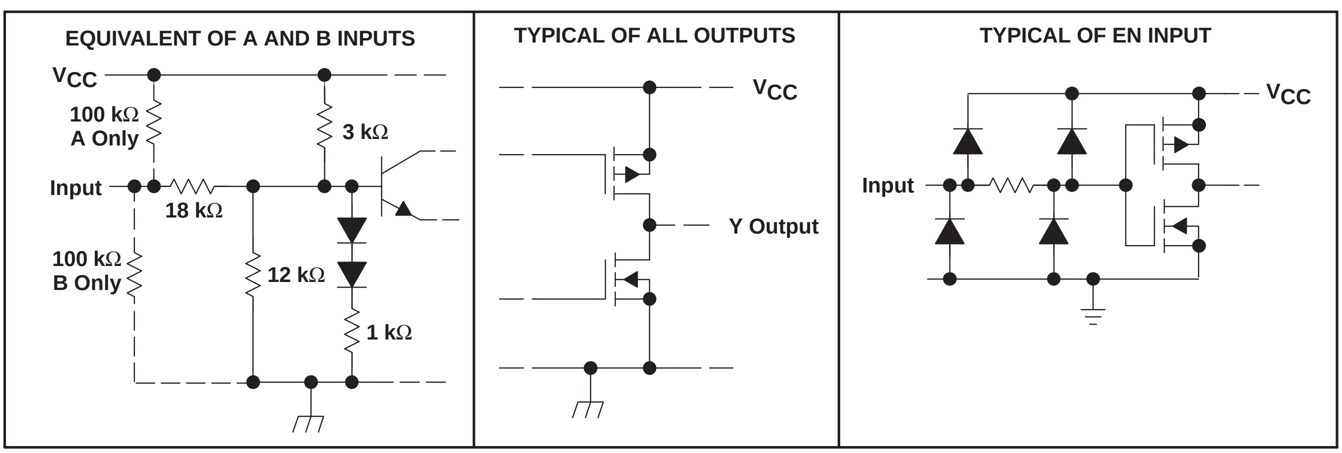
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for the J or W package.

logic diagram (positive logic)



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) . . . . –0.3 V to 7 V
Input voltage, A or B inputs, V_I . . . . ±25 V
Differential input voltage, V_{ID} (see Note 2) . . . . ±25 V
Data and control voltage range . . . . –0.3 V to 7 V
Continuous total dissipation . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A . . . . –55°C to 125°C
Storage temperature range, T_{stg} . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to GND.
2. Differential input voltage is measured at the noninverting input with respect to the corresponding inverting input.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 125°C$ POWER RATING
FK	1375 mW	11.0 mW/°C	275 mW
J	1375 mW	11.0 mW/°C	275 mW
W	1000 mW	8.0 mW/°C	200 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
Common-mode input voltage, V_{IC}		–7		12	V
Differential input voltage, V_{ID}				±6	V
High-level input voltage, V_{IH}	EN inputs	2			V
Low-level input voltage, V_{IL}	EN inputs			0.8	V
High-level output current, I_{OH}				–8	mA
Low-level output current, I_{OL}				16	mA
Operating free-air temperature, T_A		–55		125	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

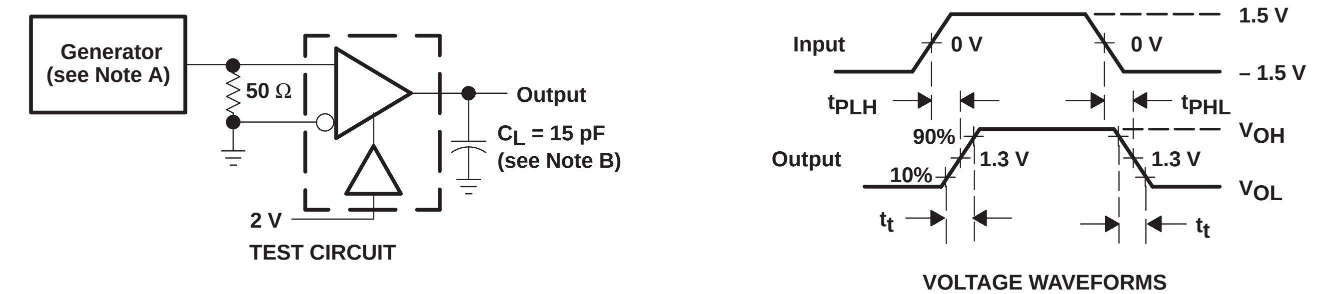
PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage		$I_O = -8$ mA			0.2	V
V_{IT-}	Negative-going input threshold voltage		$I_O = 8$ mA	−0.2			V
V_{hys}	Hysteresis voltage ($V_{IT+} - V_{IT-}$)				45		mV
V_{IK}	Enable input clamp voltage		$I_I = -18$ mA		−0.9	−1.5	V
V_{OH}	High-level output voltage		$V_{ID} = 200$ mV, $I_{OH} = -8$ mA	3.5	4.5		V
V_{OL}	Low-level output voltage		$V_{ID} = -200$ mV, $I_{OL} = 8$ mA		0.3	0.5	V
			$V_{ID} = -200$ mV, $I_{OL} = 8$ mA, $T_A = 125°C$			0.7	
I_{OZ}	High-impedance-state output current		$V_O = 0$ V to V_{CC}			±20	µA
I_I	Bus input current	A or B inputs	$V_{IH} = 12$ V, $V_{CC} = 5$ V, Other inputs at 0 V		0.7	1	mA
			$V_{IH} = 12$ V, $V_{CC} = 0$ V, Other inputs at 0 V		0.8	1	
			$V_{IH} = -7$ V, $V_{CC} = 5$ V, Other inputs at 0 V		−0.5	−0.8	
			$V_{IH} = -7$ V, $V_{CC} = 0$ V, Other inputs at 0 V		−0.4	−0.8	
I_{IH}	High-level enable input current		$V_{IH} = 5$ V			±20	µA
I_{IL}	Low-level enable input current		$V_{IL} = 0$ V			−20	µA
I_{OS}	Short-circuit output current		$V_O = 0$		−80	−120	mA
I_{CC}	Supply current		Outputs enabled, $I_O = 0$, $V_{ID} = 5$ V		11	20	mA
			Outputs disabled		0.9	1.4	

† All typical values are at $V_{CC} = 5$ V and $T_A = 25°C$.

switching characteristics, $V_{CC} = 5$ V, $C_L = 15$ pF

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
t_{PHL}	Propagation delay time, high- to low-level output	$V_{ID} = -1.5$ V to 1.5 V, See Figure 1	25°C	11	22	30	ns
			−55°C to 125°C			35	
t_{PLH}	Propagation delay time, low- to high-level output	$V_{ID} = -1.5$ V to 1.5 V, See Figure 1	25°C	11	22	30	ns
			−55°C to 125°C			35	
t_{PZH}	Output enable time to high level	See Figure 2	25°C		17	40	ns
			−55°C to 125°C			45	
t_{PZL}	Output enable time to low level	See Figure 3	25°C		18	30	ns
			−55°C to 125°C			35	
t_{PHZ}	Output disable time from high level	See Figure 2	25°C		30	40	ns
			−55°C to 125°C			55	
t_{PLZ}	Output disable time from low level	See Figure 3	25°C		23	30	ns
			−55°C to 125°C			45	
$t_{sk(p)}$	Pulse skew ($\|t_{PHL} - t_{PLH}\|$)	See Figure 1	25°C		4	6	ns
			−55°C to 125°C			7	
t_t	Transition time	See Figure 1	25°C		3	10	ns
			−55°C to 125°C			16	

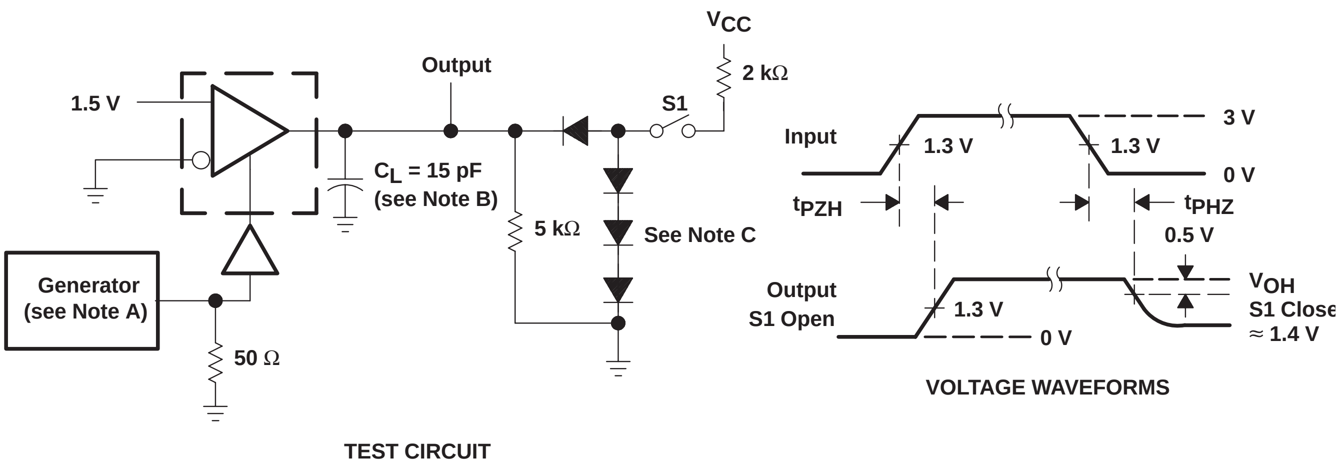
PARAMETER MEASUREMENT INFORMATION



NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle ≤ 50%, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

B. C_L includes probe and jig capacitance.

Figure 1. t_{PLH} and t_{PHL} Test Circuit and Voltage Waveforms



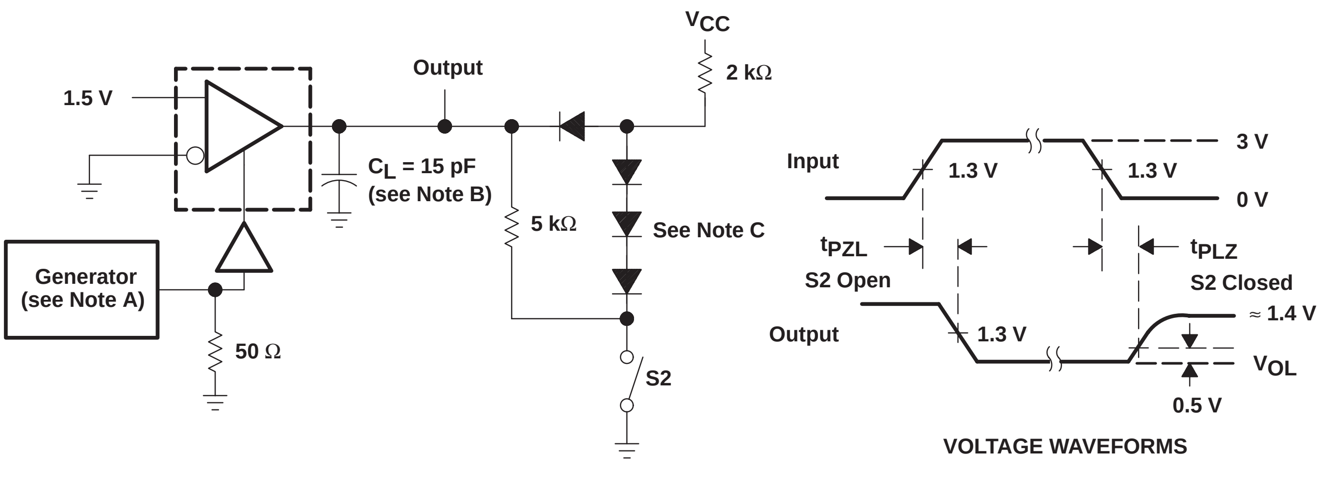
NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle ≤ 50%, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

B. C_L includes probe and jig capacitance.

C. All diodes are 1N916 or equivalent.

Figure 2. t_{PHZ} and t_{PZH} Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle ≤ 50%, $t_r \leq$ 6 ns, $t_f \leq$ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N916 or equivalent.

Figure 3. t_{PZL} and t_{PLZ} Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE vs DIFFERENTIAL INPUT VOLTAGE

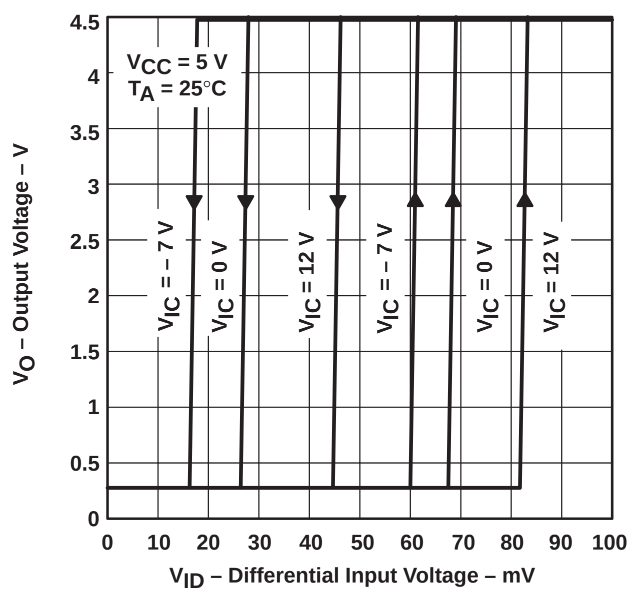


Figure 4

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

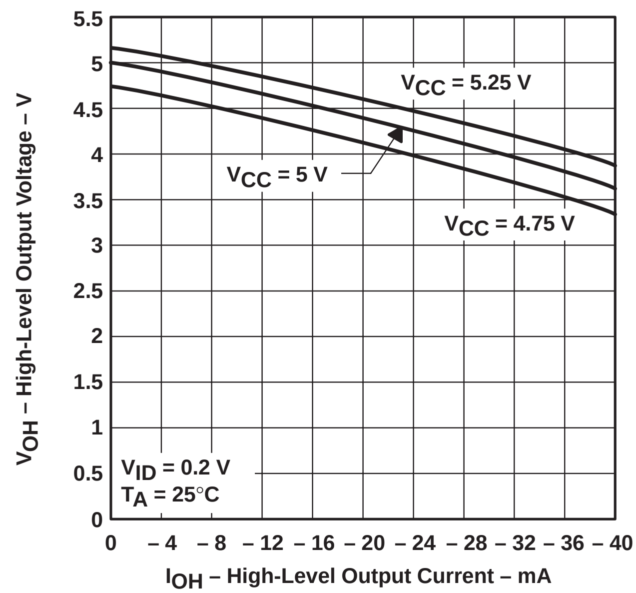


Figure 5

TYPICAL CHARACTERISTICS

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

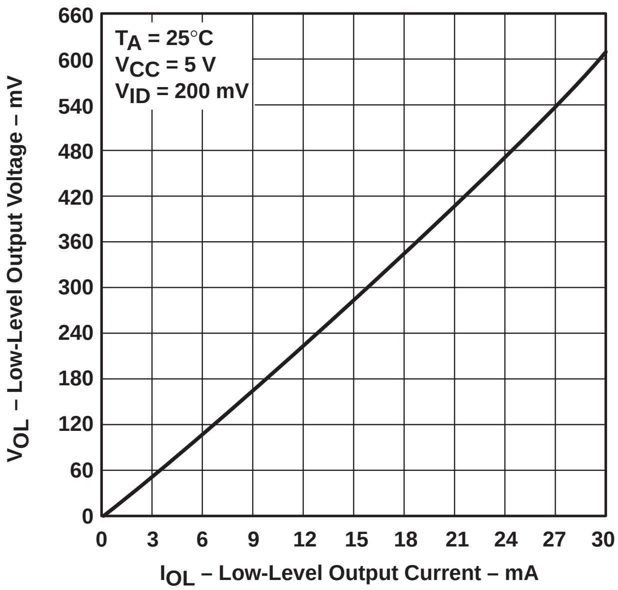


Figure 6

AVERAGE SUPPLY CURRENT
vs
FREQUENCY

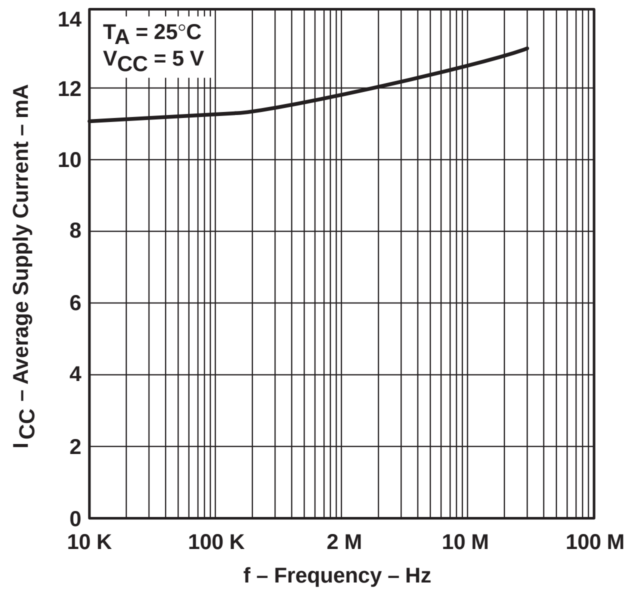


Figure 7

BUS
INPUT CURRENT
vs
INPUT VOLTAGE
(COMPLEMENTARY INPUT AT 0 V)

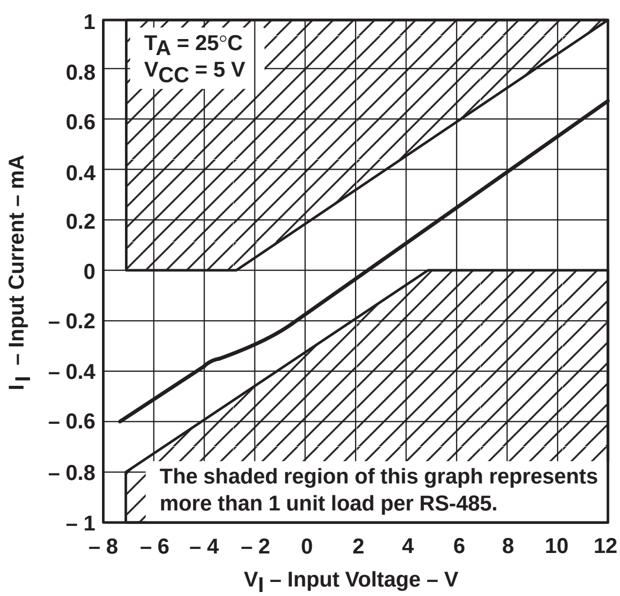


Figure 8

PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE

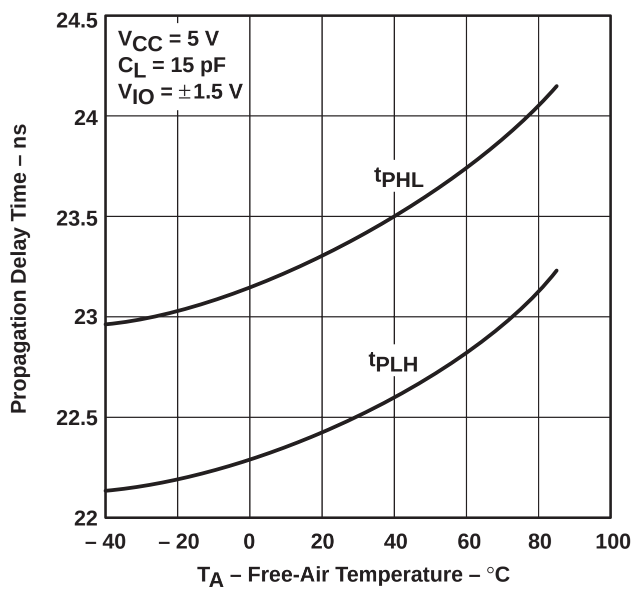


Figure 9

IMPORTANT NOTICE