Evaluation Unit of THS8083

1. Overview and main components of the evaluation circuit board.

The evaluation unit is designed to fully evaluate all the functions of the THS8083 device, meanwhile the design of the print circuit board can be used as a reference when customers try to design a system by using THS8083.

The figure 2 is block diagram of the PC board. Based on the diagram, the PC board consists of following main parts.

- THS8083 device. The package of this device is implemented in the power-pad package. So the PCB area directly under THS8083 is exposed cooper. The exposed bottom of the die of the device should be soldered to this area of the board. This will dramatically help the heat dissipation of the device, and increase the reliability of the system.

- The ALTERA FPGA contains all the control logic of the panel display. It has I2C slave module with device address 80H, display data formatter, and display timing generator.

- Two voltage regulators are U16 and U20. Both of them are TPS73HD301, each has dual voltage outputs. This is the power pad package also, the bottom of the device is soldered on the PCB board's ground plan to help the heat dispassion.

2. Connectors and their usage

Following are the connectors that will be used for THS8083 function evaluation. There may be more connectors than the ones are drowned in the block diagram or in schematics. But they will not be used for THS8083 evaluation. Please ignore those that are not on the schematics.

- The power supply of the evaluation unit is provided by a single external power supply, which should be connected to a DIN-5 connector of the unit.

- Video input signals from PC graphics card can be connected to the DB15 VGA connector, or to the five separated SMA connectors on the board. For the best performance, these SMA connectors should be used. A video cable with five separated BNC connectors is shipped with the evaluation unit to fully explore the THS8083. There are no jumper selections on the board to connect or disconnect the video-input signal from the DB15 or SMAs. Only one of the two connectors (DB15 or SMA) can be connected to input signals at the same time.

- DB25 is used to connect to a PC's parallel port. A window program in the PC will control the THS8083 and FPGA on the board via this connection. For details, please refer to the software manual.

- A 60-pin connector is used to connect to the LCD panel display via a ribbon-cable. The other end of a ribbon cable is an adapter on a small PCB, which is used for connecting to back of a LCD panel.

- A 6-pin connector is used to connect to a back-light module of the LCD panel. Associated with this connector, there is a potentiometer for the brightness adjustment.

Note: The Black-color wire of the back-light cable is corresponding to pin 1 of the header (U14) on the PC board. Make sure this connection is right before turn on the power.

Following figure dictated the orientation of this connection.

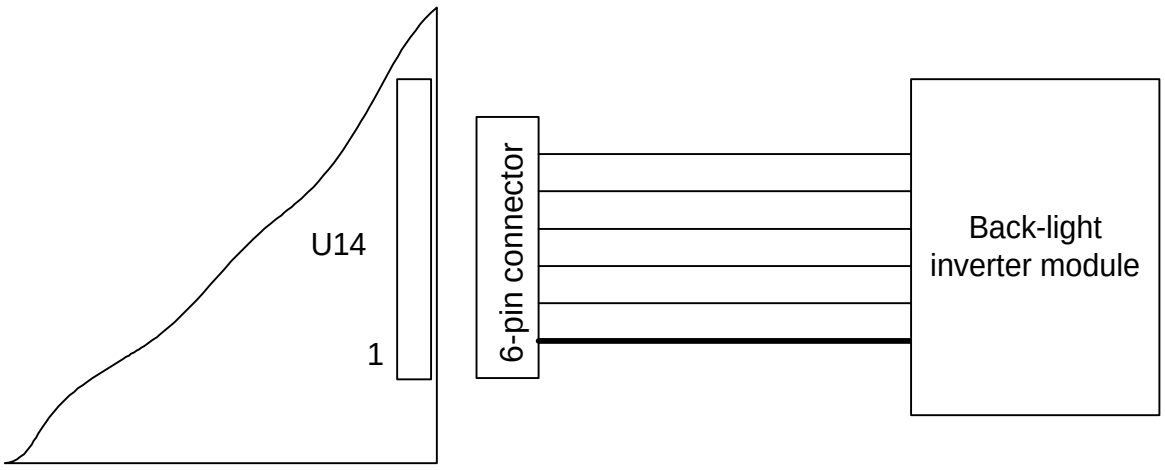


Figure 2. The power cable connection of back-light inverter module to THS8083 EVM board.

3. FPGA Controller

Figure3 is the top-level design schematic of the ALTERA FPGA. Figure4 is the block diagram of this design. These diagrams present a good overview of the functions of the FPGA controller. If the design of the FPGA is needed, please contact your TI local sales office. Following are the main module inside this FPGA.

- I2C slave module has been implemented. This allows a PC to control all the devices on board through a single interface.
- Timing generator generates the HS, VS timing for display module interface
- Data path manager controls interfacing different modes from THS8083 output data to LCD panel
- Register bank stores all the register settings from PC via I2C

For programmable setting, please refer to the software Manuel.

4. Jumper setting table

The order of jumpers in following table is arranged according to their physical location on the PCB. Starting from the left-up corner of the board, then goes to right-down of the board.

Jumper name	Setting	Description
JP22	OPEN	Not used, always open
JP5	Close	Digital 3.3V supply, always close
JP52	Close	Digital 3.3V supply for digital data buffer, always close
JP2	Close	3.3V of digital PLL of THS8083
JP62	Open	These two pins are for the I2C testing, always open
JP57	Close	The THS8083 I2C address selection. When it is closed, the I2C address of THS8083 is 40H for writing and 41H for reading. When it is open, the I2C address of THS8083 is 42H for writing and 43H for reading.
JP1	Close	Analog 3.3V power supply for the PLL in THS8083

JP61	Close	When the middle pin is connected to the 'PC' mark, the input vertical sync signal comes from a PC graphics card. When the middle pin is connected to the 'PLD' mark, the vertical sync signal is generated by the ALTERA FPGA.
JP21	Open	Not used for this version PCB
JP35	Open	Not used for this version PCB
JP20	Open	Not used for this version PCB
JP43	Close	FPGA 3.3V power supply, always closed
JP40	Open	Not used for this version PCB
JP41	Open	Not used for this version PCB
JP42	Open	Not used for this version PCB
JP23	Close	Enable/disable the data bus buffer, middle pin connected 'EN' pin will enable the bus buffer.
JP26	Close	Enable/disable the data bus buffer, middle pin connected 'EN' pin will enable the bus buffer.
JP68	Open	Always open, this is the test point of vertical sync signal.
JP67	Open	Always open, this is the test point of PLL locking signal of THS8083.
JP9	Open	Not used for this version PCB
JP69	Open	Not used for this version PCB
JP70	Open	Not used for this version PCB
JP71	Open	Not used for this version PCB
JP46	Open	Not used for this version PCB
JP50	Open	Not used for this version PCB
JP12	Open	Not used for this version PCB
JP17	Open	Not used for this version PCB
JP38	Close	FPGA output enable, always close to enable
JP39	Open	Not used for this version PCB
JP13	Open	Test point of ADCCLK1 of THS8083
JP47	Open	Test point of ACDCLK1 of THS8083
JP48	Open	Test point of ADCCLK2 of THS8083
JP49	Open	Test point of DTOCLK3 of THS8083
JP60	Close	Output enable of THS8083, always close to enable it
JP25	Open	Not used for this version PCB
JP27	Open	Not used for this version PCB
JP4	Open	Not used for this version PCB
JP16	Open	Not used for this version PCB
JP15	Open	Not used for this version PCB
JP33	Close	When middle pin is connected to 'SW', the reset signal comes from the U22(TLC7703, voltage supervising device)
JP36	Close	ADCCLK1 is selected for the input clock of FPGA
JP34	Open	If it is closed, the DTOCLK3 will be selected as the clock of FPGA
JP37	Open	Not used for this version PCB
JP29	Close	The middle pin is connected to 'EN' to enable video data output to LCD panel
JP30	Close	The middle pin is connected to 'EN' to enable video data output to LCD panel
JP3	Close	Analog 3.3V power supply, always close
JP32	Close	Analog 3.3V power supply, always close
JP53	Close	Analog 3.3V power supply, always close
JP7	Open	Not used for this version PCB
JP8	Open	Not used for this version PCB
JP10	Open	Not used for this version PCB
JP11	Open	Not used for this version PCB
JP14	Open	Not used for this version PCB

JP19	Open	Not used for this version PCB
JP18	Open	Not used for this version PCB

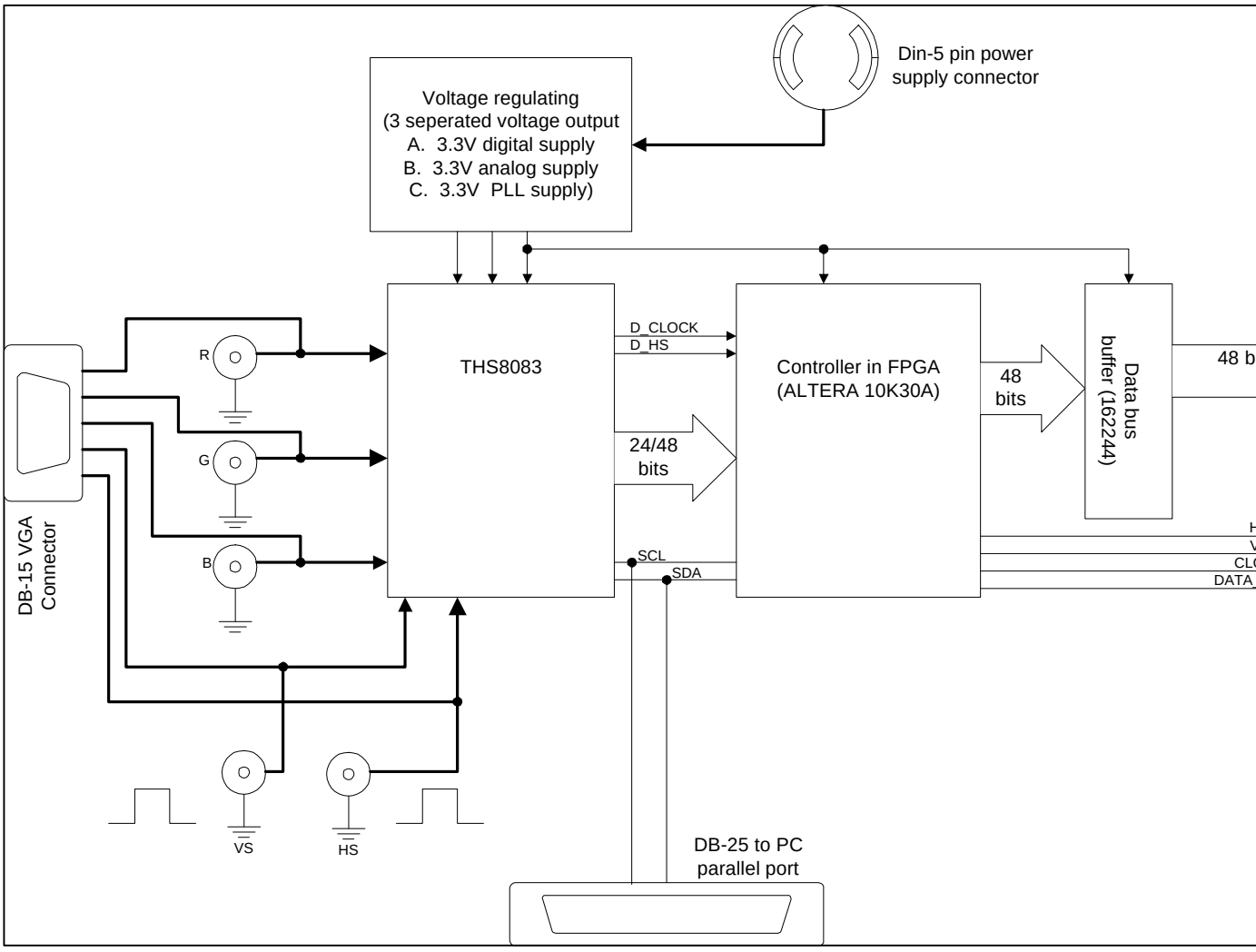


Figure2 Block diagram of the THS8083 evaluation circuit board

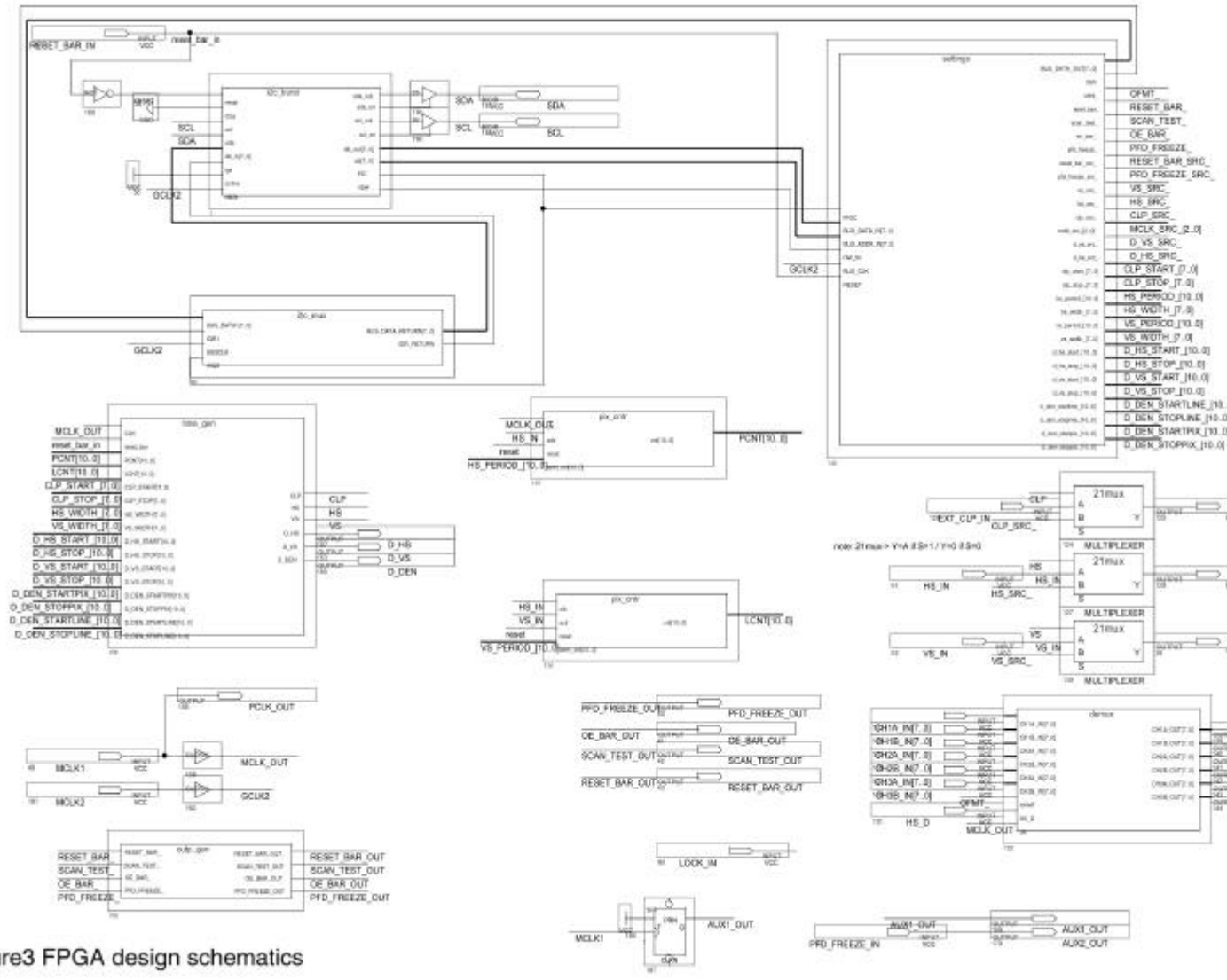


Figure3 FPGA design schematics

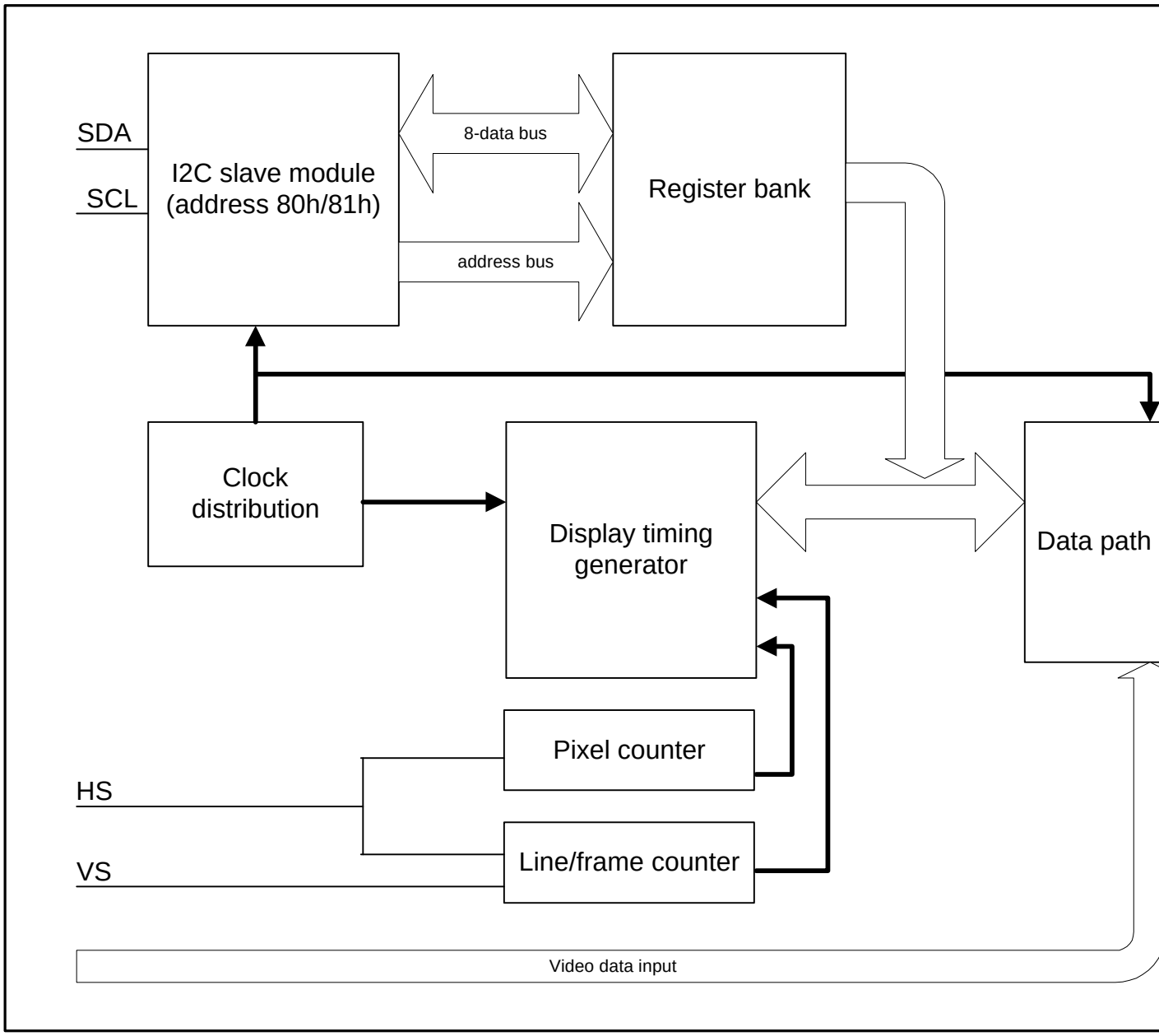
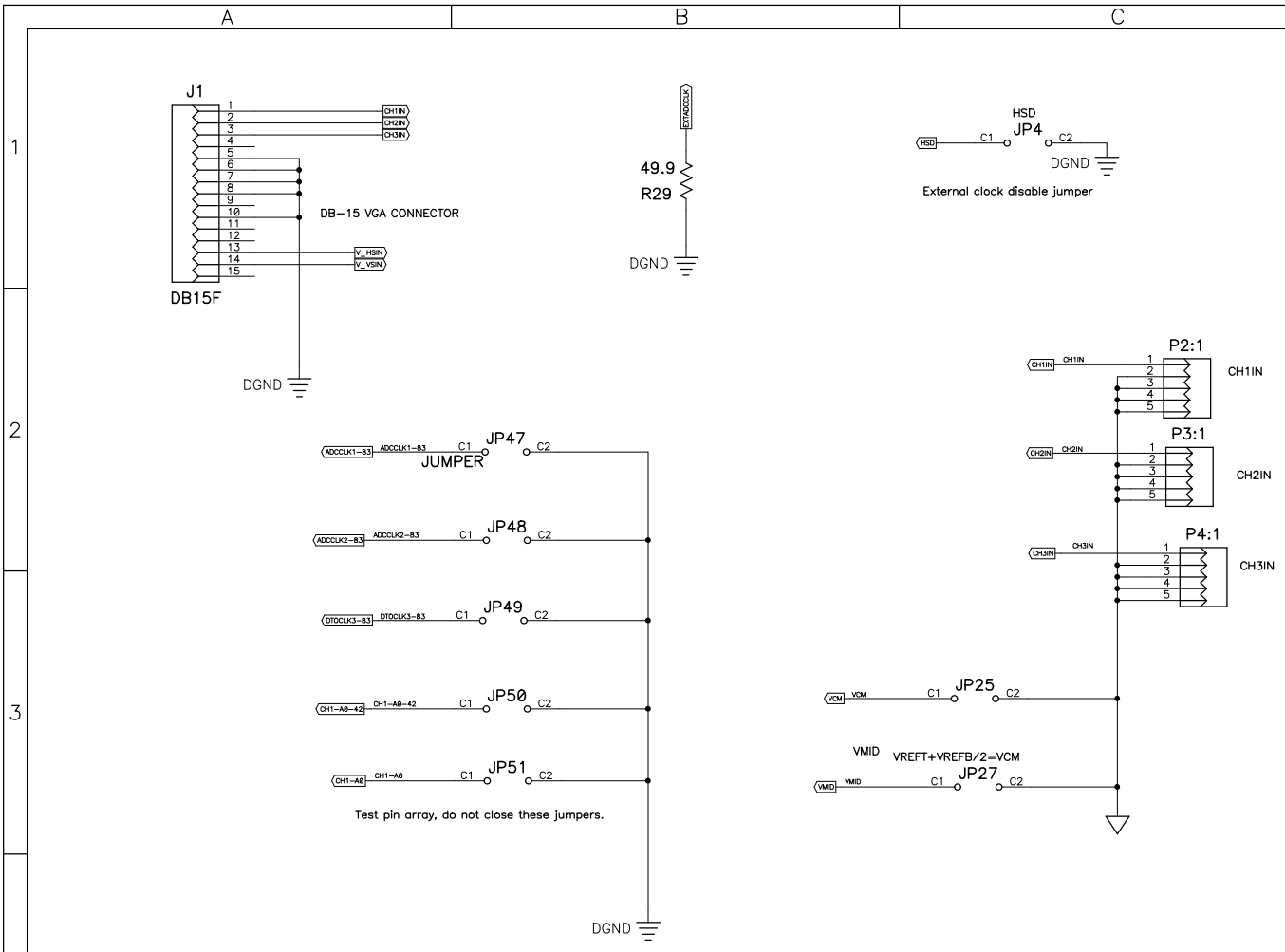
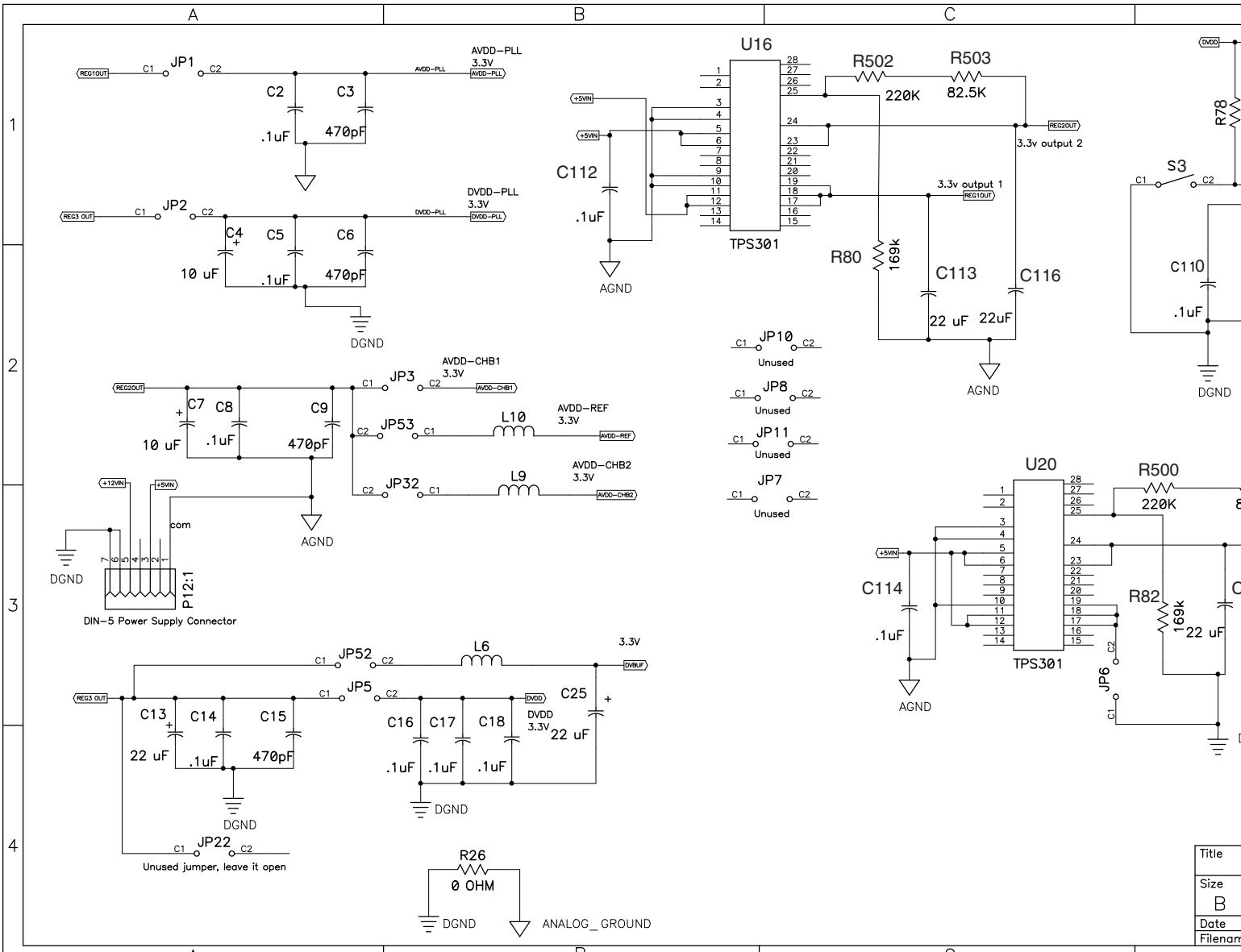
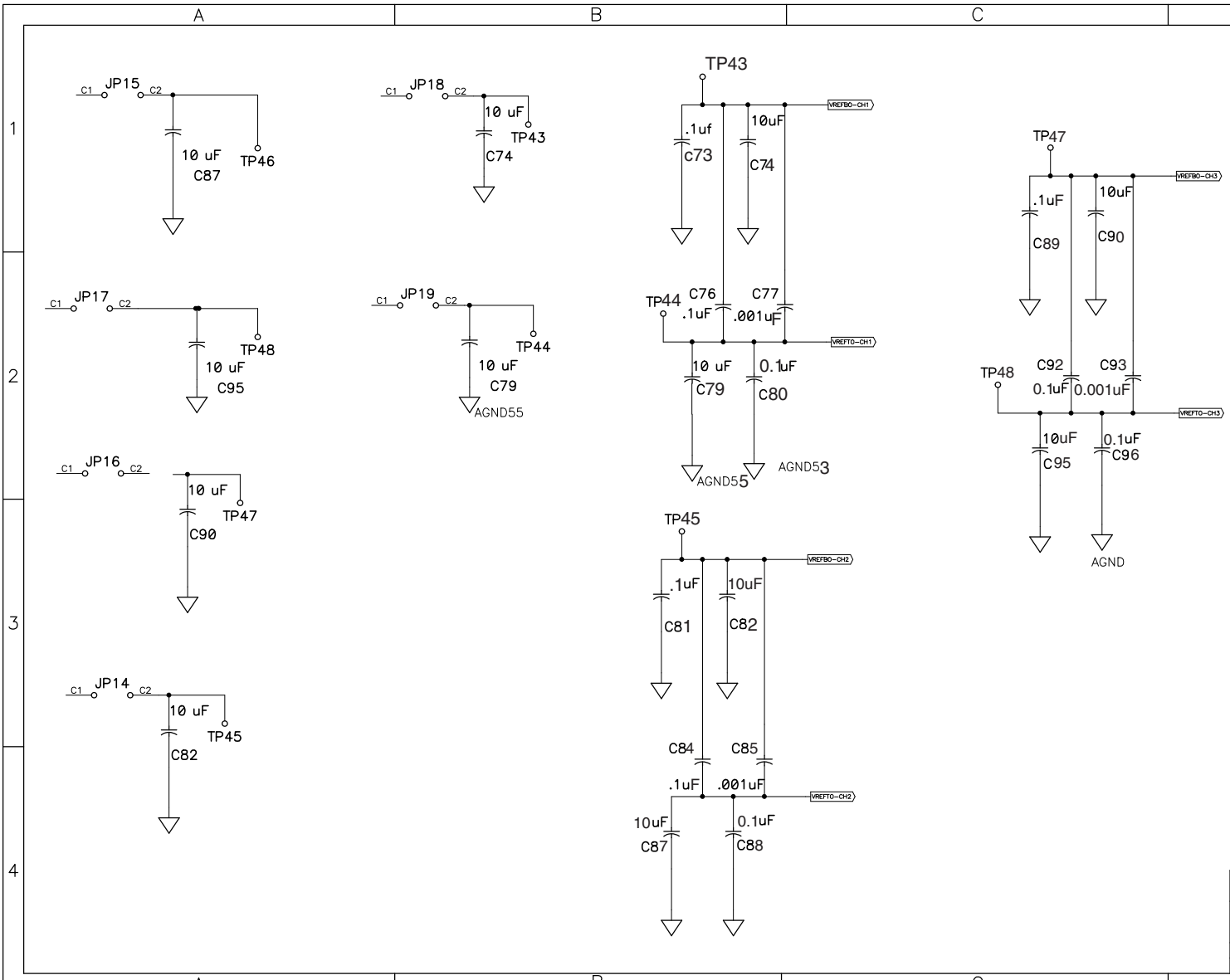
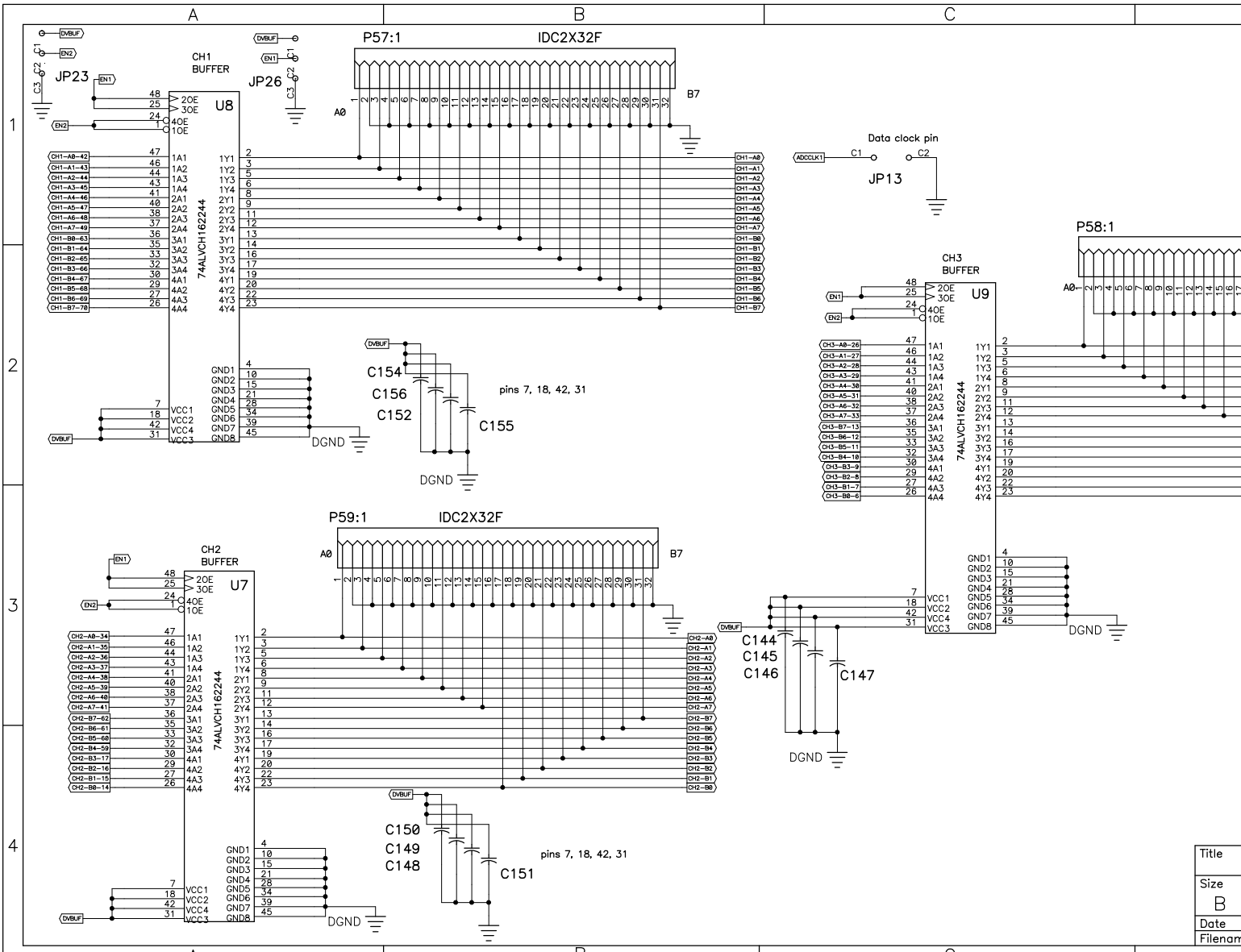


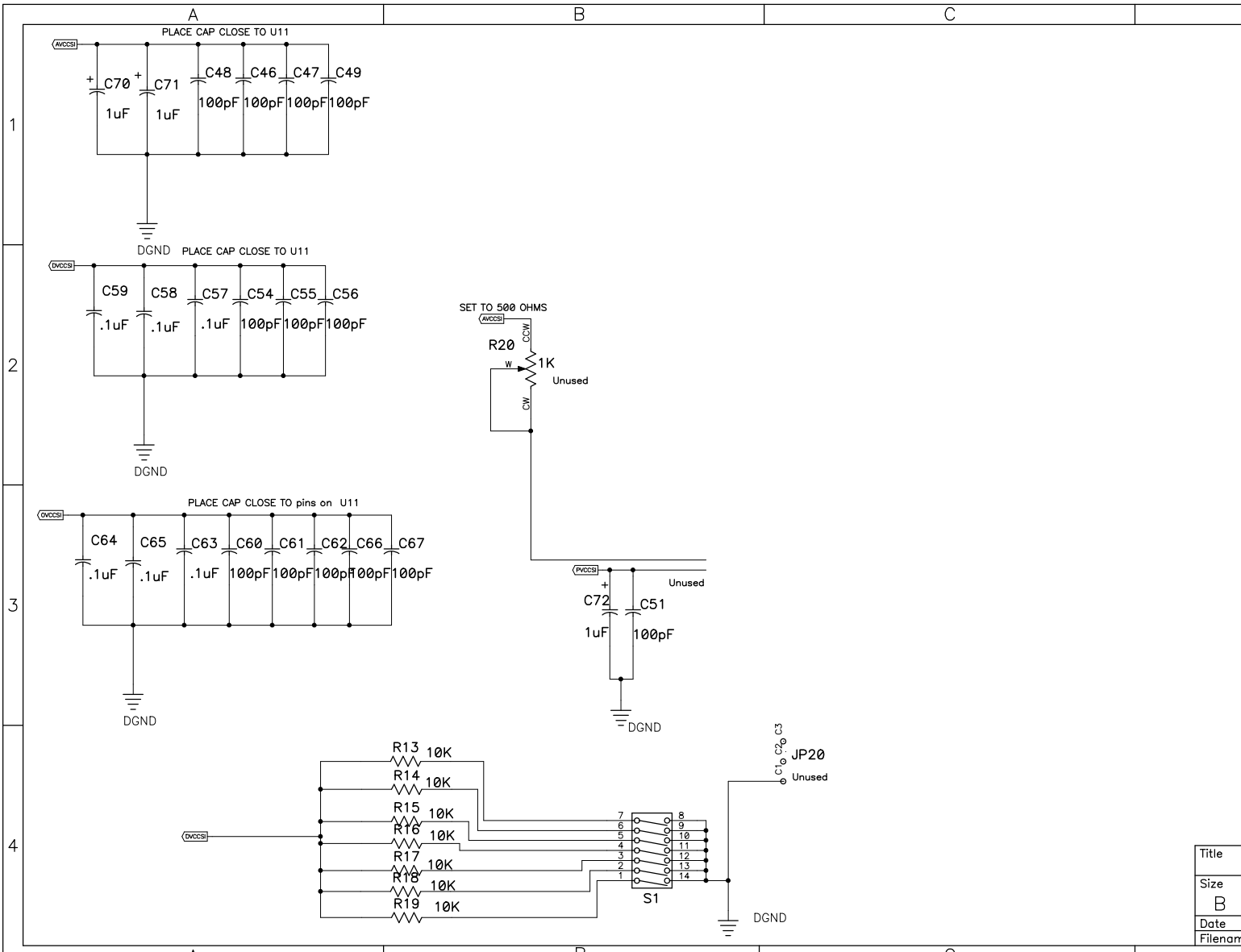
Figure4 Block diagram FPGA design

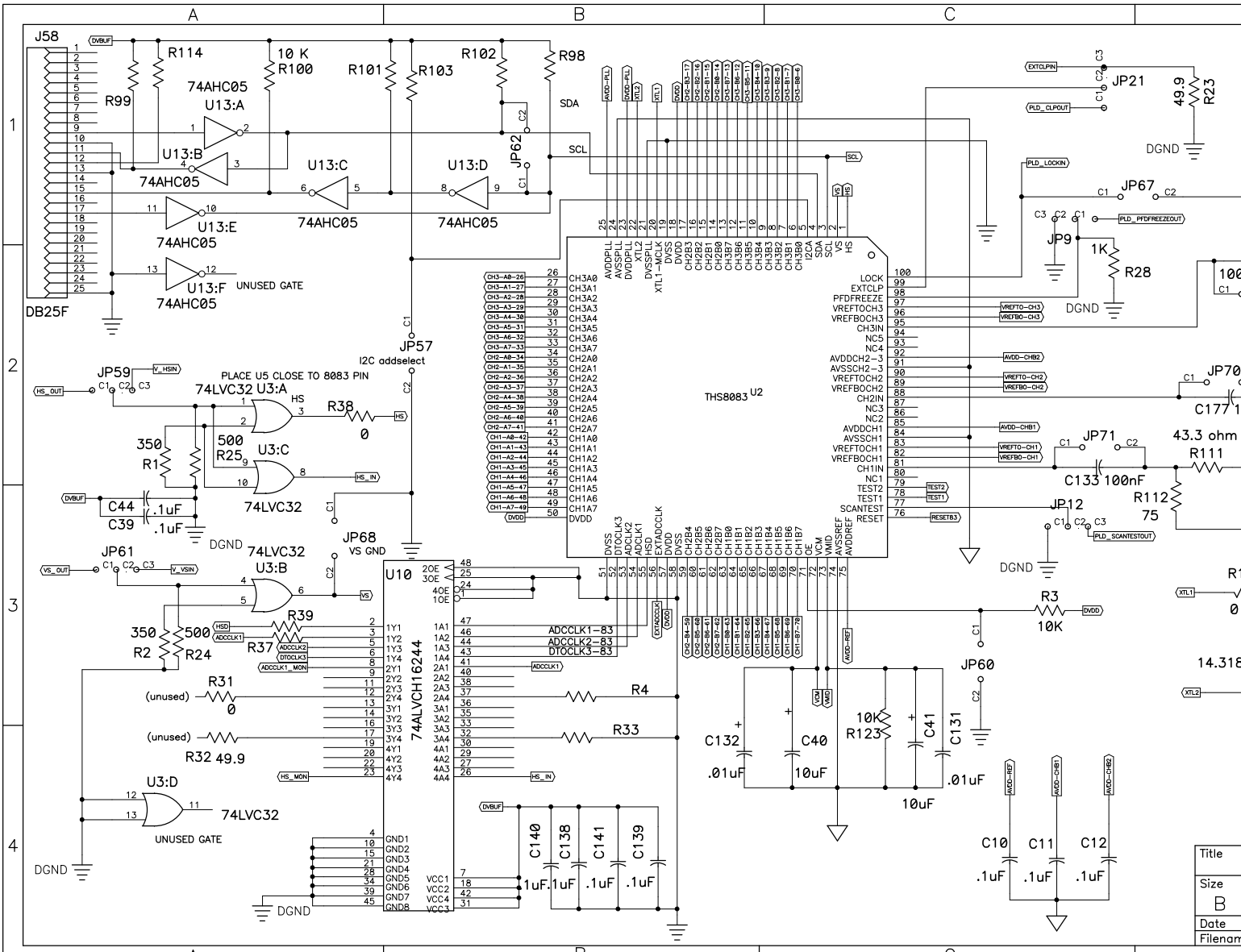

A
B
C
1
2
3
4
J1
CH1IN
CH2IN
CH3IN
V_HSIN
V_VSIN
DB15F
DB-15 VGA CONNECTOR
DGND
EXTADCCLK
49.9
R29
DGND
HSD
JP4
C1
C2
DGND
External clock disable jumper
ADCCLK1-B3
JP47
JUMPER
ADCCLK2-B3
JP48
DTOCLK3-B3
JP49
CH1-A0-42
JP50
CH1-A0
JP51
Test pin array, do not close these jumpers.
DGND
P2:1
CH1IN
P3:1
CH2IN
P4:1
CH3IN
VCM
JP25
VMID
VREFT+VREFB/2=VCM
JP27
Title
Size
B
Date
Filenam

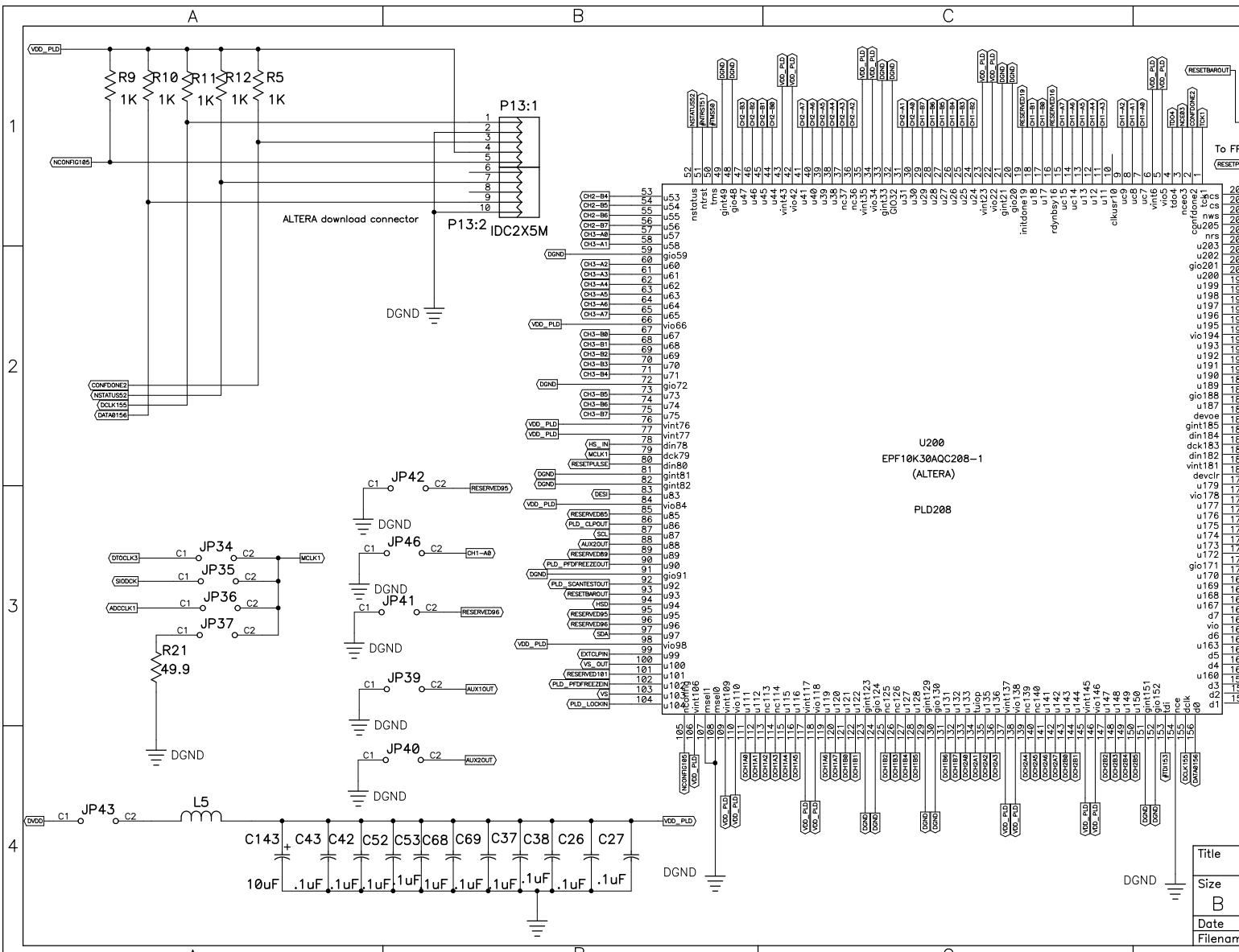

A
B
C
1
2
3
4
JP1
C1
C2
REG1OUT
AVDD-PLL
3.3V
C2
C3
.1uF
470pF
JP2
REG3 OUT
DVDD-PLL
C4
C5
C6
10 uF
.1uF
470pF
DGND
U16
TPS301
R502
220K
R503
82.5K
+5VIN
C112
.1uF
AGND
REG2OUT
3.3v output 2
3.3v output 1
REG1OUT
R80
169k
C113
C116
22 uF
22uF
JP10
Unused
JP8
Unused
JP11
Unused
JP7
Unused
R78
S3
C110
.1uF
DVDD
JP3
AVDD-CHB1
3.3V
C7
C8
C9
JP53
L10
AVDD-REF
JP32
L9
AVDD-CHB2
+12VIN
com
P12:1
DIN-5 Power Supply Connector
U20
R500
220K
C114
R82
169k
22 uF
JP6
JP52
L6
JP5
C25
DVDD
DVBUF
C13
C14
C15
C16
C17
C18
JP22
Unused jumper, leave it open
R26
0 OHM
ANALOG_ GROUND
Title
Size
B
Date
Filenam

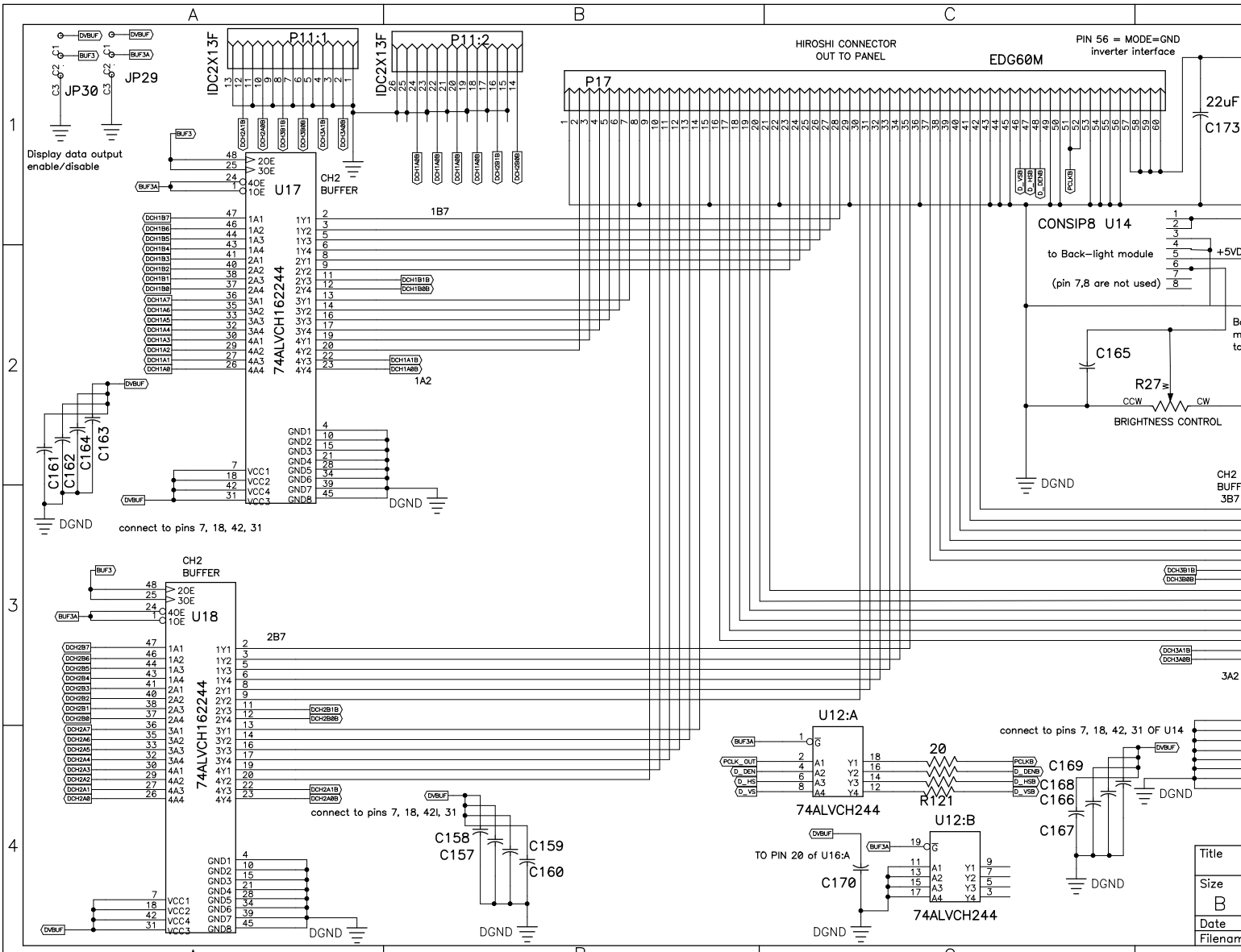

A
B
C
1
2
3
4
JP15
C1
C2
10 uF
C87
TP46
JP18
10 uF
C74
TP43
TP43
.1uf
C73
10uF
C74
VREFBO-CH1
TP47
.1uF
C89
10uF
C90
VREFBO-CH3
JP17
TP48
10 uF
C95
JP19
TP44
10 uF
C79
AGND55
TP44
C76
.1uF
C77
.001uF
VREFTO-CH1
10 uF
C79
0.1uF
C80
AGND55
AGND53
TP48
C92
0.1uF
C93
0.001uF
VREFTO-CH3
10uF
C95
0.1uF
C96
AGND
JP16
10 uF
C90
TP47
TP45
.1uF
C81
10uF
C82
VREFBO-CH2
JP14
10 uF
C82
TP45
C84
C85
.1uF
.001uF
VREFTO-CH2
10uF
C87
0.1uF
C88
Title
Size
B
Date
Filenam


A
B
C
1
2
3
4
CH1
BUFFER
U8
74ALVCH162244
JP23
JP26
P57:1
IDC2X32F
A0
B7
DVBUF
EN1
EN2
C1
C2
C3
DGND
C154
C156
C152
C155
pins 7, 18, 42, 31
Data clock pin
ADCCLK1
JP13
CH3
BUFFER
U9
P58:1
CH2
BUFFER
U7
P59:1
C144
C145
C146
C147
C150
C149
C148
C151
Title
Size
B
Date
Filenam


A
B
C
1
2
3
4
PLACE CAP CLOSE TO U11
AVCCSI
C70
C71
C48
C46
C47
C49
1uF
1uF
100pF
100pF
100pF
100pF
DGND
PLACE CAP CLOSE TO U11
DVCCSI
C59
C58
C57
C54
C55
C56
.1uF
.1uF
.1uF
100pF
100pF
100pF
DGND
SET TO 500 OHMS
AVCCSI
R20
CCW
W
1K
Unused
CW
PLACE CAP CLOSE TO pins on U11
DVCCSI
C64
C65
C63
C60
C61
C62
C66
C67
.1uF
.1uF
.1uF
100pF
100pF
100pF
100pF
100pF
DGND
PVCCSI
Unused
C72
C51
1uF
100pF
DGND
R13 10K
R14 10K
R15 10K
R16 10K
R17 10K
R18 10K
R19 10K
DVCCSI
S1
C1
C2
C3
JP20
Unused
DGND
Title
Size
B
Date
Filenam


A
B
C
J58
DB25F
DVBUF
R114
10 K
R100
R101
R103
R102
R98
R99
74AHC05
U13:A
U13:B
U13:C
U13:D
U13:E
U13:F
UNUSED GATE
SDA
SCL
JP62
JP57
I2C addselect
PLACE U5 CLOSE TO 8083 PIN
74LVC32 U3:A
74LVC32 U3:B
74LVC32 U3:C
74LVC32 U3:D
JP59
JP61
JP68
VS GND
R38
R39
R37
R24
R2
R1
R25
350
500
C44
C39
.1uF
DGND
U10
74ALVCH16244
ADCCLK1-83
ADCCLK2-83
DTOCLK3-83
R4
R33
R31
R32 49.9
(unused)
HS_MON
HS_IN
C140
C138
C141
C139
1uF
THS8083 U2
JP21
JP67
JP9
JP70
JP71
JP12
JP60
R23
49.9
R28
1K
R111
43.3 ohm
R112
75
C133 100nF
C177
R3
10K
R123
C132
C40
C41
C131
.01uF
10uF
C10
C11
C12
EXTCLPIN
PLD_CLPOUT
PLD_LOCKIN
PLD_PFDFREEZEOUT
PLD_SCANTESTOUT
VREFTO-CH3
VREFBO-CH3
VREFTO-CH2
VREFBO-CH2
VREFTO-CH1
VREFBO-CH1
AVDD-CHB2
AVDD-CHB1
AVDD-REF
Title
Size
B
Date
Filenam


A
B
C
1
2
3
4
VDD_PLD
R9 1K
R10 1K
R11 1K
R12 1K
R5 1K
P13:1
P13:2
IDC2X5M
ALTERA download connector
NCONFIG185
CONFDONE2
NSTATUS52
DCLK155
DATA0156
DGND
JP34
JP35
JP36
JP37
JP40
JP41
JP42
JP43
JP46
JP39
DTOCLK3
SIODCK
ADCCLK1
MCLK1
RESERVED95
CH1-A8
RESERVED96
AUX1OUT
AUX2OUT
R21 49.9
L5
DVDD
C143 10uF
C43 .1uF
C42 .1uF
C52 .1uF
C53 1uF
C68 1uF
C69 1uF
C37 1uF
C38 .1uF
C26 .1uF
C27 .1uF
U200
EPF10K30AQC208-1
(ALTERA)
PLD208
RESETBAROUT
To FF
Title
Size
B
Date
Filenam


A
B
C
1
2
3
4
JP30
JP29
C3
C2
C1
DVBUF
BUF3
BUF3A
Display data output
enable/disable
IDC2X13F
P11:1
P11:2
HIROSHI CONNECTOR
OUT TO PANEL
EDG60M
P17
PIN 56 = MODE=GND
inverter interface
22uF
C173
U17
CH2
BUFFER
74ALVCH162244
2OE
3OE
4OE
1OE
1B7
1A2
CONSIP8 U14
to Back-light module
(pin 7,8 are not used)
+5VD
C165
R27
CCW
CW
BRIGHTNESS CONTROL
DGND
C161
C162
C164
C163
connect to pins 7, 18, 42, 31
U18
2B7
connect to pins 7, 18, 42l, 31
C158
C157
C159
C160
U12:A
U12:B
74ALVCH244
20
R121
connect to pins 7, 18, 42, 31 OF U14
C169
C168
C166
C167
TO PIN 20 of U16:A
C170
Title
Size
B
Date
Filenam