



TLC876 Analog-to-Digital Converter Evaluation Board

USER MANUAL

TLC 876 Evaluation Module Application Note

The TLC876 Evaluation Module provides a platform for lab prototype evaluation of the Texas Instruments TLC876 10 bit, 20 MSPS high speed analog to digital converter.

Since practical operation up to 20 MHz can be achieved, the circuit layout is critical and does not lend itself to classical breadboarding techniques. In fact, use of surface mount components is required to achieve proper operation.

Power Supply Requirements

The TLC876 EVM is designed to be powered by regulated lab power supplies. Two lab supplies (AVDD and DVDD) are required for best performance. A third supply can be added since the TLC876 is designed to be able to interface to +3.3 V logic. An additional connection is provided to permit the addition of a +3.3 V supply for DRVDD.

SUPPLY	CONNECTOR	USE
+5V	J4	(AVDD) Analog power and input amplifier stage positive supply.
+5V	J5	(DVDD) ADC internal logic supply.
+5V or +3.3V	J6	(DRVDD) Digital interface logic supply.

The (AGND) Analog and (DGND) Digital ground planes can be tied together if desired at the AGND and DGND points directly below J4 and J5. Additionally, two pads AGND and DGND are provided directly below the ADC for connecting the two ground planes.

This allows the user to adapt to various grounding conditions that may exist in an evaluation circuit interface.

TLC876 EVM Analog Input

The analog input signal is applied to the BNC connector J3. This signal is routed to the TLC876 analog input by one of three paths.

Direct Input

AC Coupled with DC bias

User supplied Input

Direct Input

To route the signal directly to the TLC 876 input, connect XAIN to the pin socket tied to AIN pin 27 of the TLC876. These pin sockets are labeled on the schematic as E2A and E2B.

This provides a 50 ohm load (R11) at the input connector. The input is defined by the internal structure of the sample and hold amplifier on the TLC 876. Refer to the specifications within the TLC 876 data sheet for a detailed explanation.

AC coupled with DC bias

If AC coupling is desired, the DC bias to the amplifier input is controlled by the setting of potentiometer R7. This allows the bias to be varied from near REF "B" (ladder BOTTOM) to near REF "T" (ladder TOP). Connect AINOFF to the pin socket tied to pin 27 of the TLC876 if AC coupling is desired. These pin sockets are labeled as E1A and E1B on the schematic.

The low frequency response pole will be dominated by the 4.7uF capacitor (C15) and the resistance setting of the pot.

User Supplied Input Circuit

A breadboarding area is provided for the user to allow custom input filters or other signal conditioning circuits to be used. To route the signal from the breadboard area to the TLC876 input connect BBAOUT to the pin socket tied to pin 27 of the TLC876. These pin sockets are labeled as E3A and E3B on the schematic.

Only one of the above configurations should be used at any one time to prevent excessive capacitance on the signal path, which could degrade the input signal quality at higher frequencies.

Test Points

Test points TP1 -TP4 are provided for monitoring the following:

TP1	Clock output
TP2	Clock input
TP3	Output enable
TP4	Analog input to the TLC876

Digital Inputs/Outputs

Two buffers (U3 and U6) are provided to insure lengths up to 12" of ribbon cable can be driven reliably. Damping resistors of 22 ohms are placed in series on all high speed lines. All relevant signals are made available at J2.

JP2 can be removed if external control of the STANDBY pin is required.

Pin 24 on the output connector (J2) can be used to drive U3 and U6's outputs to a high impedance state allowing a bus interface to external circuitry. If external control of the outputs is required JP1 should be removed. A Logic 1 applied to J2 pin 24 will tri-state the outputs of the 74AC11244s.

Clock Circuit

An external clock of up to 20 MHZ is required for operation. The clock source is required to drive the 50 ohm BNC input J1. The clock is buffered by inverters (U1) and provides a true (non-inverted) equivalent output at pin 22 of the output connector J2. This provides the user a buffered reference clock output for external circuitry. Note that U1 is powered from DRVDD so output levels will be dependent on the DRVDD supply voltage.

Reference Voltage Circuit

U5, a REF194GS, provides a 25 ppm / degree Centigrade instrumentation quality voltage reference.

Potentiometers R3 and R5 can be adjusted to provide, through the followers U2A and U2B in a force-sense reference connection, any setting from near ground to 4.5 V.

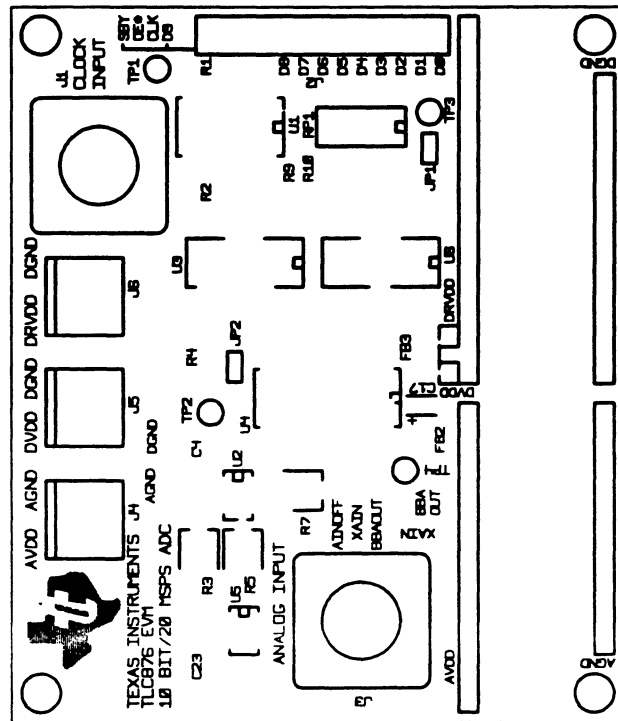
The full scale input span of the TLC876 can be achieved with this circuit. R3 is typically adjusted to provide a voltage of 4.0 V at REFTF. R5 is typically adjusted to provide a voltage of 2.0 V at REFBF.

The user has the option of setting both the full scale span of the analog input and where to center this voltage.

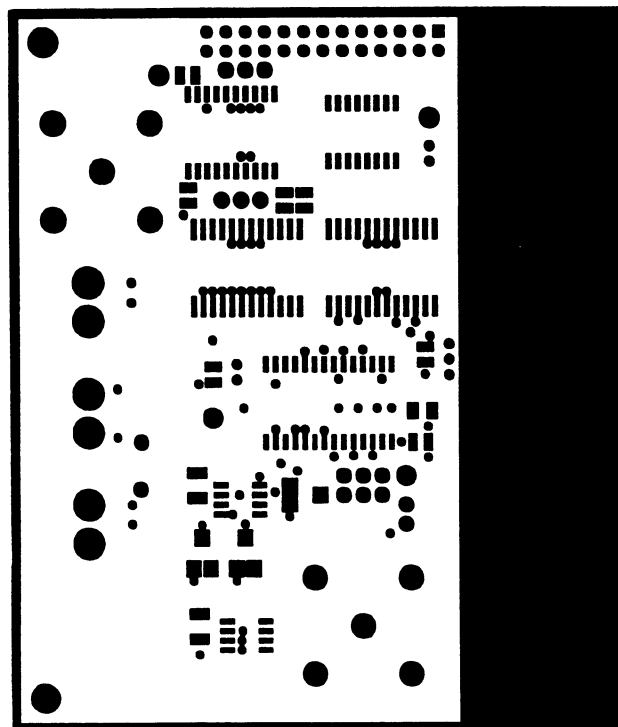
The TLV2442A device employs dual op amps with rail-to-rail outputs which can provide up to 50mA to the TLC876 resistive ladder.

Summary

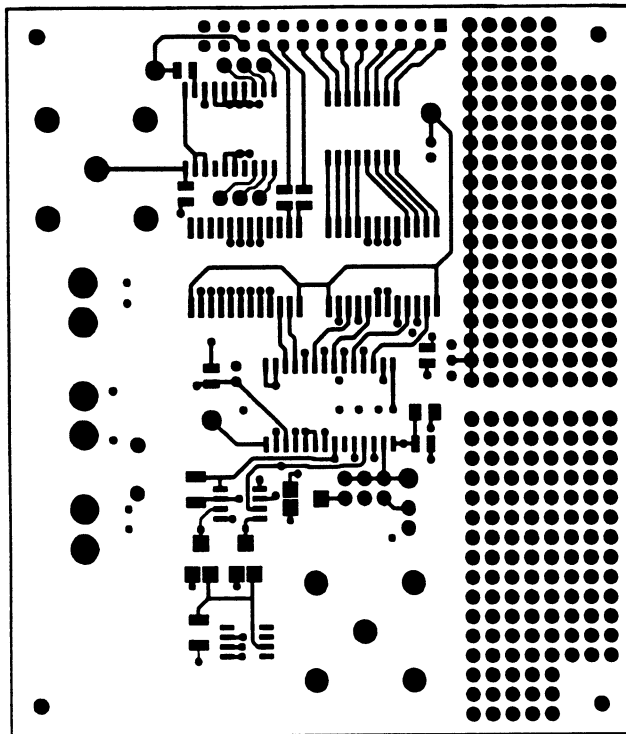
The TLC876 EVM provides the user the ability to quickly evaluate the speed and resolution of the TLC876 ADC for various applications.



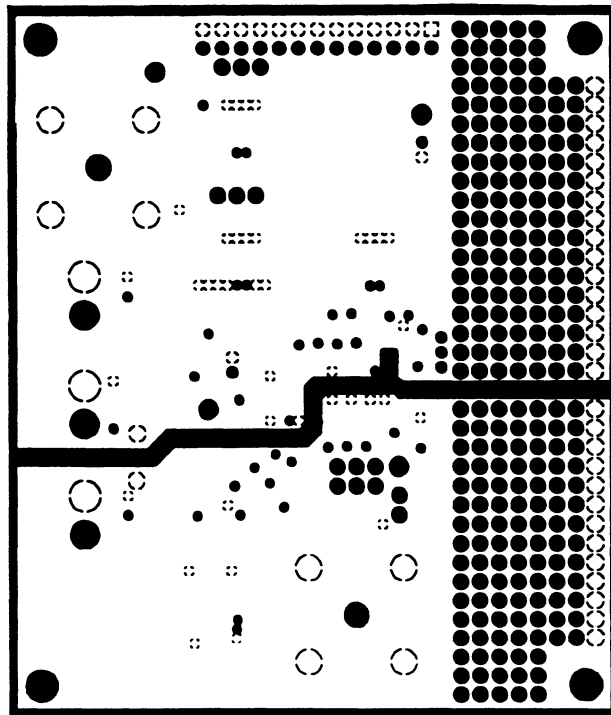
Top Side Silkscreen



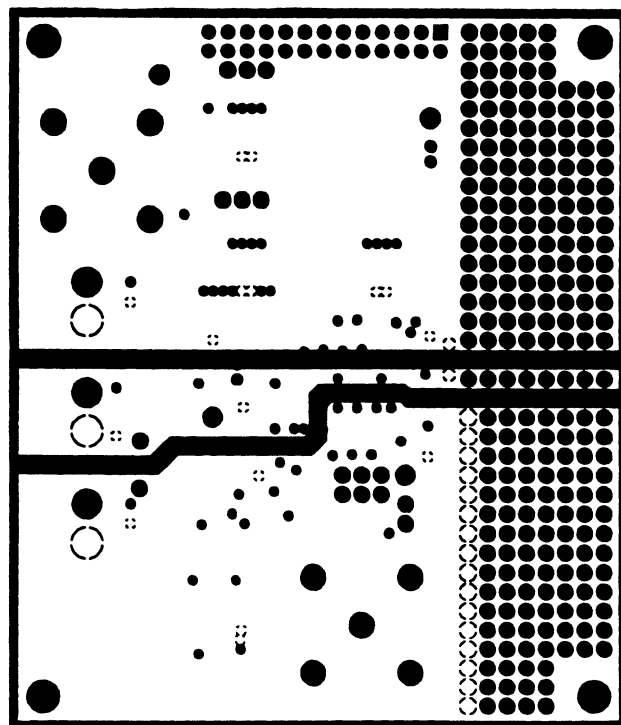
Top Side Soldermask



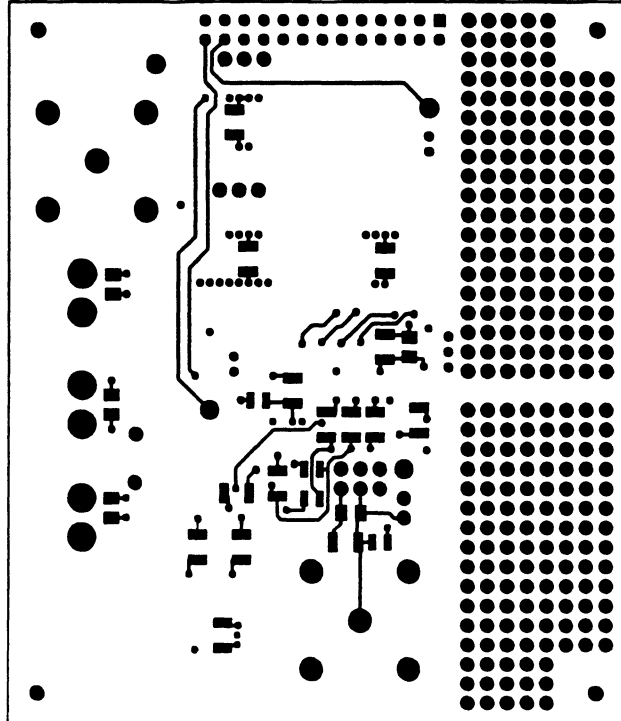
Layer 1



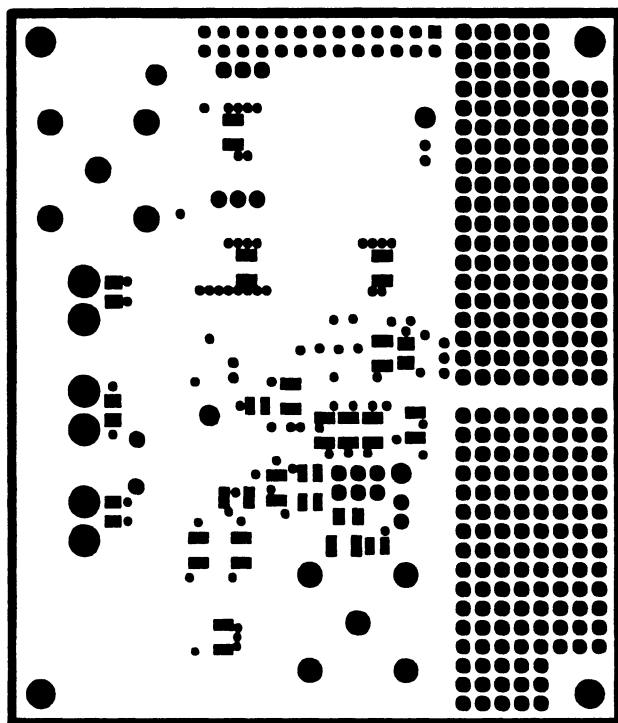
Layer 2



Layer 3



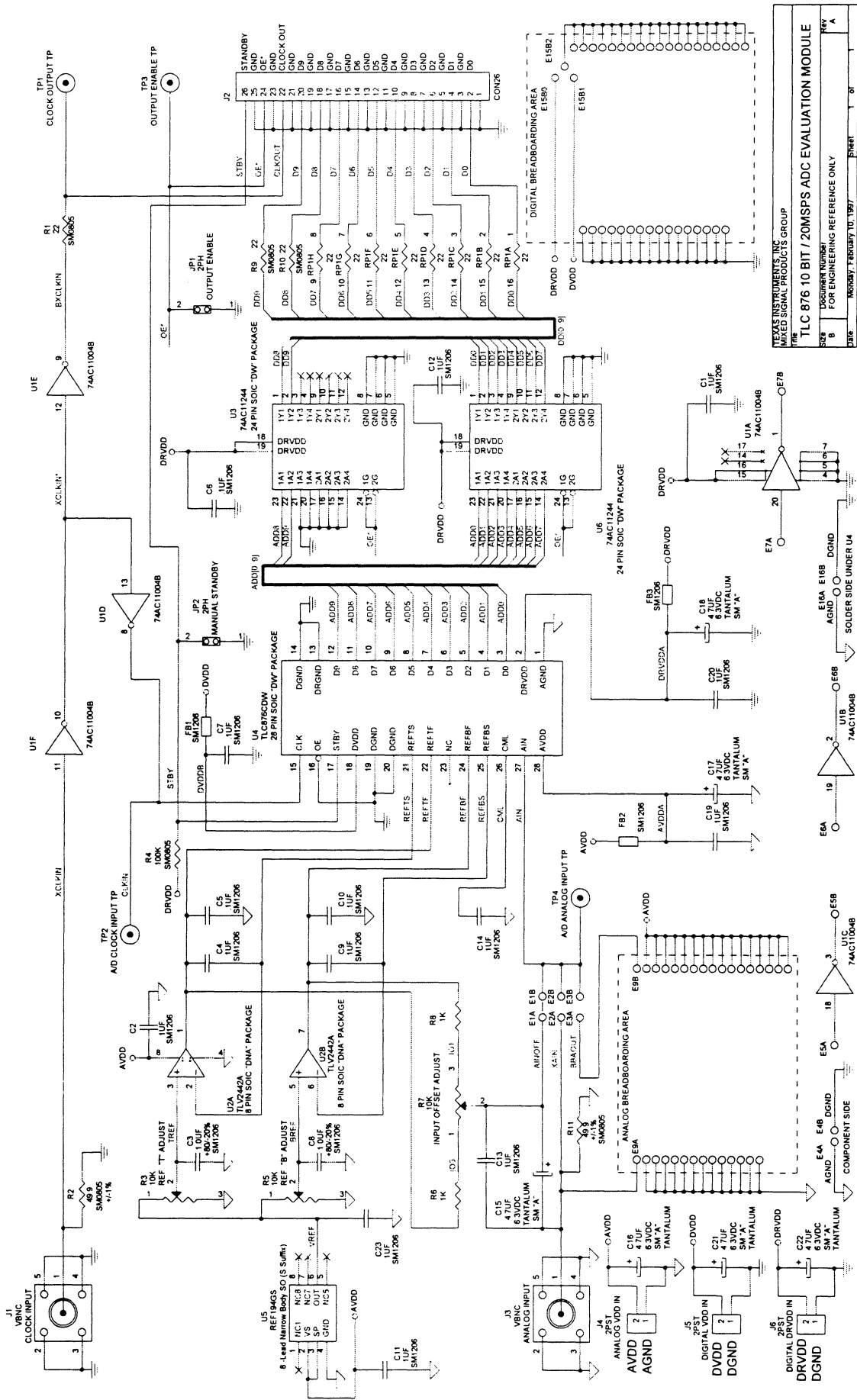
Layer 4



Bottom Side Soldermask



NOTES 10 UNLESS OTHERWISE SPECIFIED CAPACITORS ARE IN UF, $\pm 20\%$, 50VDC
20 UNLESS OTHERWISE SPECIFIED RESISTORS ARE IN OHMS, $\pm 5\%$



TLC876 10 BIT / 20MSPS ADC EVALUATION MODULE			
DATE	DESIGNER	REVISION	REVISION
8	B	1	1
FOR ENGINEERING REFERENCE ONLY			
MONDAY, FEBRUARY 10, 1997			
SHEET			

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Email epic@ti.com

Japan

Phone
 International +81-3-3457-0972
 Domestic +0120-81-0026
Fax
 International +81-3-3457-1259
 Domestic +0120-81-0036
Email pic-japan@ti.com

Asia

Phone	International	+886-2-23786800	
	Domestic	Local Access Code	TI Number
Australia	1-800-881-011		-800-800-1450
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Thailand	0019-991-1111		-800-800-1450
Fax	886-2-2378-6808		
Email	tiasia@ti.com		

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