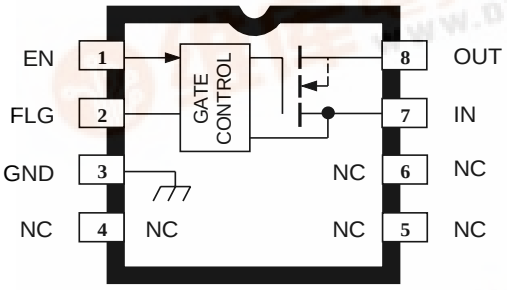
2525 AND 2535

Data Sheet 27447.1

USB POWER CONTROL SWITCHES

A2525EM



Dwg. PP-070A

Note that the A2525EM (DIP) and the A2525EL (SOIC) are electrically identical and share a common terminal number assignment.

ADVANCE INFORMATION
(subject to change without notice)
August 2, 1999

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{IN} ..... **6.0 V**
Output Voltage, V_{OUT} ..... **6.0 V**
Output Current,
I_{OUT} ..... **Internally Limited**
ENABLE Voltage Range,
V_{EN} ..... **–0.3 V to 10 V**
Fault Flag Voltage, V_{FLG} ..... **8.0 V**
Fault Flag Current, I_{FLG} ..... **50 mA**
Package Power Dissipation,
P_D ..... **See Graph**
Operating Temperature Range,
T_A ..... **-40°C to +85°C**
Junction Temperature, T_J ..... **+150°C***
Storage Temperature Range,
T_S ..... **-65°C to 150°C**

* Fault conditions that produce excessive junction temperature will activate device thermal shutdown circuitry. These conditions can be tolerated but should be avoided.

The A2525EL/M and A2535EL/M are integrated high-side power switches, optimized for self-powered and bus-powered Universal Serial Bus (USB) applications. Few external components are necessary to satisfy USB requirements. The A2525EL/EM ENABLE inputs are active high; the A2535EL/EM are active low.

All devices are ideally suited for USB applications. Each switch channel supplies up to 500 mA as required by USB peripheral devices. In addition, the switch's low on-resistance permits achieving the USB voltage-drop requirements. Fault current is limited to typically 750 mA, satisfying the UL 25 VA safety requirements, and a flag output is available to indicate a fault condition to the local USB controller. Momentary voltage drops that may occur on the upstream port when the switch is enabled in bus-powered applications is eliminated by a "soft start" feature.

Additional features include thermal shutdown to prevent catastrophic switch failure from high-current loads, undervoltage lockout to ensure that the device remains OFF unless there is a valid input voltage present, and 3.3 V and 5 V logic-compatible enable inputs.

These switches are provided in 8-pin mini-DIP (suffix 'M') and 8-lead SOIC (suffix 'L') packages.

Features

- 2.7 V to 5.8 V Input
- Up to 500 mA Continuous Load Current
- 140 mΩ Maximum ON-Resistance
- 1.25 A Maximum Short-Circuit Current Limit
- Individual Open-Drain Fault Flag Outputs
- 110 µA Typical ON-State Supply Current
- 1 µA Typical OFF-State Supply Current
- Outputs Can be Forced Higher Than Input (off-state)
- Thermal Shutdown
- 2.4 V Typical Undervoltage Lockout
- 1 ms Turn On (soft-start) and Fast Turn Off
- Active-High or Active-Low Enable Versions
- Improved Replacements for MIC2525-1 and MIC2525-2

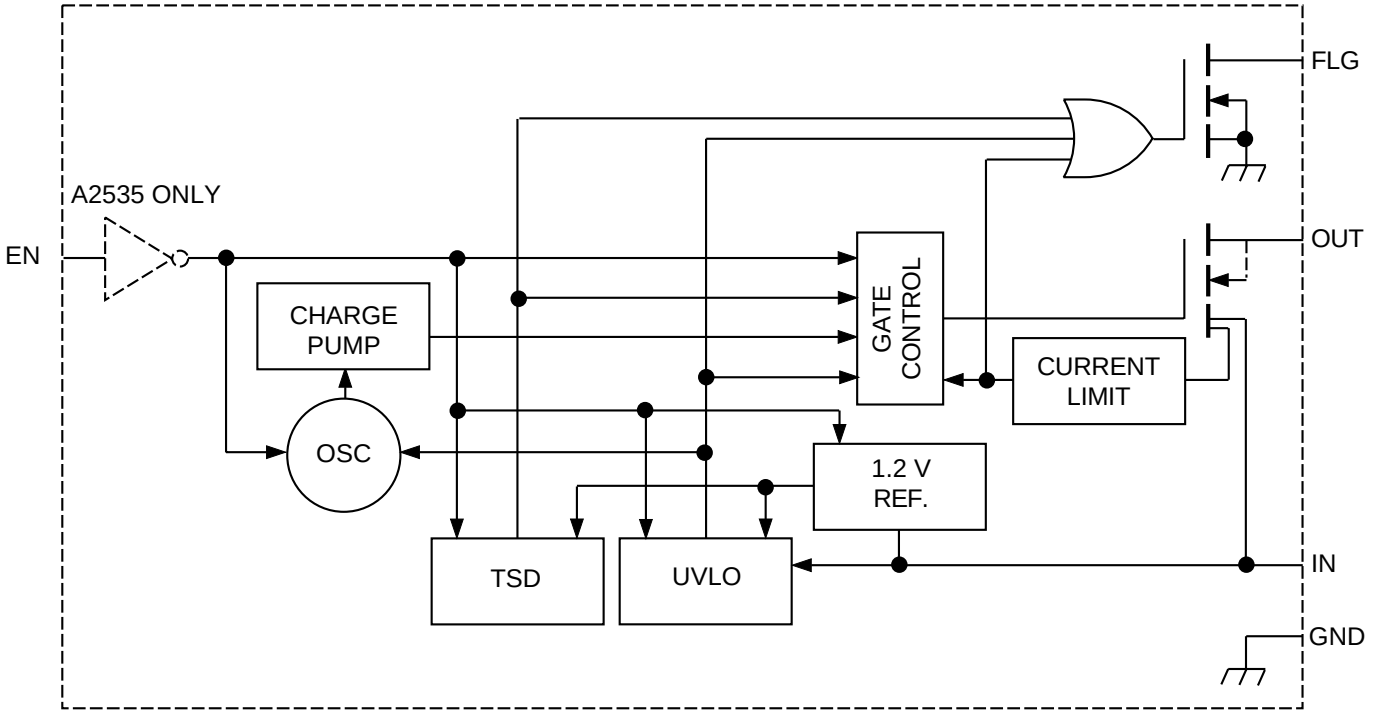
Applications

- USB Hosts and Self-Powered Hubs
- USB Bus-Powered Hubs
- Hot Plug-In Power Supplies
- Battery-Charger Circuits

Allegro®

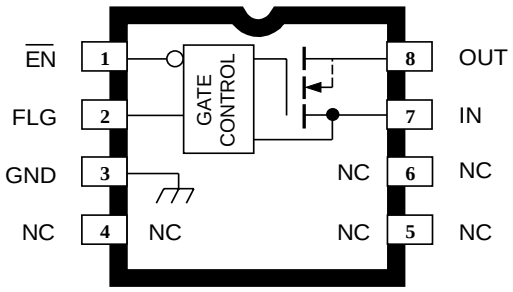
2525 AND 2535
USB
POWER CONTROL
SWITCHES

FUNCTIONAL BLOCK DIAGRAM



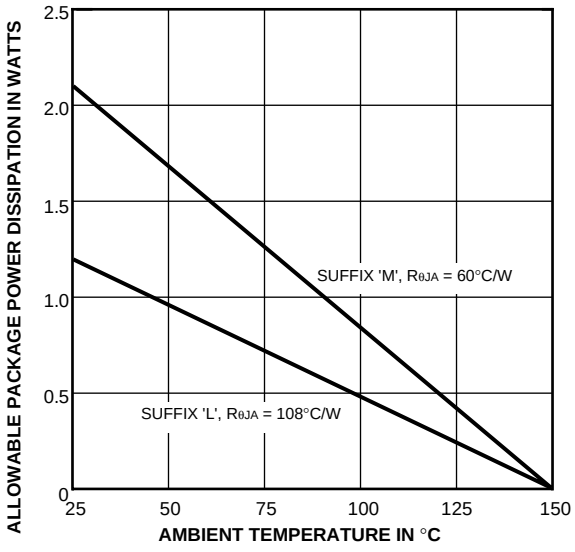
Dwg. FP-049

A2535EM



Dwg. PP-070-1A

Note that the A2535EM (DIP) and the A2535EL (SOIC) are electrically identical and share a common terminal number assignment.



Dwg. GP-009-2

Electrical Characteristics at T_A = 25°C, V_{IN} = 5 V (unless otherwise noted).

Parameter	Test Conditions	Limits			
		Min	Typ	Max	Units
Operating Voltage Range	V_{IN}	2.7	–	5.8	V
Switch Resistance	V_{IN} = 5 V, I_{OUT} = 500 mA	–	100	140	mΩ
	V_{IN} = 3.3 V, I_{OUT} = 500 mA	–	100	140	mΩ
Output Leakage Current	Output disabled, V_{IN} = 5 V, V_{OUT} = 0	–	–	10	µA
Maximum Load Current		500	–	–	mA
Short-Circuit Current Limit	Output enabled into load, V_{OUT} = 4 V	0.5	–	1.25	A
Current-Limit Threshold	Ramped load applied to enabled output, $V_{OUT} \leq 4$ V	–	1.6	–	A
ENABLE Input Threshold	Low-to-high transition	–	2.1	2.4	V
	High-to-low transition	0.8	1.9	–	V
ENABLE Input Hysteresis		–	0.2	–	V
ENABLE Input Current	V_{EN} = 0 V to 5.5 V	–	±0.01	±1.0	µA
ENABLE Input Cap.		–	1.0	–	pF
Output Turn-On Delay	R_L = 10Ω, each output	–	0.5	–	ms
Output Turn-On Rise Time	R_L = 10Ω each output	–	1.0	–	ms
Output Turn-Off Delay	R_L = 10Ω each output	–	1.0	–	µs
Output Turn-Off Fall Time	R_L = 10Ω each output	–	1.0	–	µs
Error Flag Output Resistance	V_{IN} = 5 V, I_L = 10 mA	–	10	–	Ω
	V_{IN} = 3.3 V, I_L = 10 mA	–	15	–	Ω
Error Flag Off Current	V_{FLG} = 5 V	–	0.01	–	µA
Supply Current	Switch OFF (see note), OUT = open	–	0.75	5.0	µA
	Switch ON (see note), OUT = open	–	110	160	µA
UVLO Threshold	Increasing V_{IN}	–	2.5	–	V
	Decreasing V_{IN}	–	2.3	–	V
Over-Temperature Shutdown Threshold	Increasing T_J	–	165	–	°C
	Decreasing T_J	–	155	–	°C

Note — OFF is ≤ 0.8 V and ON is ≥ 2.4 V (active high) for the A2525EL/EM. OFF is ≥ 2.4 V and ON is ≤ 0.8 V (active low) for the A2535EL/EM.

2525 AND 2535
USB
POWER CONTROL
SWITCHES

FUNCTIONAL DESCRIPTION

Power switch

The power switch is an N-channel MOSFET with a maximum on-state resistance of 140 mΩ (V_{IN} = 5 V). Configured as a high-side switch, the power switch prevents current flow in either direction if disabled. The drain body diode is disconnected from the source when the switch is OFF allowing the output voltage to exceed the input voltage without causing current conduction. The power switch supplies a minimum of 500 mA per switch.

Charge pump

An internal charge pump supplies power to the driver circuit and provides the necessary voltage to pull the gate of the MOSFET above the source. The charge pump operates from input voltages as low as 2.7 V. The charge pump is limited to 2.5 µA to establish a controlled turn on time of typically 1 ms.

Driver

The driver controls the gate voltage of the power switch. To limit large current surges and reduce the associated electromagnetic interference (EMI) produced, the driver incorporates circuitry that controls the rise times and fall times of the output voltage. The rise time is typically 1 ms.

ENABLE (EN or $\overline{\text{EN}}$)

The logic enable disables the power switch and the bias for the charge pump, driver, and other circuitry to reduce the supply current to less than 5 µA maximum when a logic high is present on EN (A2525) or a logic low is present (A2535). The proper logic level restores bias to the drive and control circuits and turns the power ON. The enable input is a compatible with both TTL and CMOS logic levels.

Fault flag (FLG)

This open drain output is asserted (active low) when an overcurrent or over temperature condition is encountered. The output will remain asserted until the overcurrent or over temperature condition is removed.

Current sense

A sense FET monitors the current supplied to the load. The sense FET measures current more efficiently than conventional resistance methods. When an overload or short circuit is encountered, the current-sense circuitry sends a control signal to the driver. The driver in turn reduces the gate voltage and drives the power FET into its saturation region, which switches the output into a constant-current mode and holds the current constant while varying the voltage on the load.

Thermal sense

An internal thermal-sense circuit shuts off the power switch when the junction temperature rises to approximately 165°C. Hysteresis is built into the thermal sense circuit. After the device has cooled approximately 10°C, the switch turns back ON. The switch continues to cycle off and on until the fault is removed.

Undervoltage lockout

A voltage-sense circuit monitors the input voltage. When the input voltage is approximately 2 V, a control signal turns OFF the power switch.

APPLICATIONS INFORMATION

Overcurrent

A sense FET is employed for overcurrent conditions. Unlike current-sense resistors, sense FETs do not increase the series resistance of the current path. When an overcurrent condition is detected, the device maintains a constant output current and reduces the output voltage accordingly. Complete shutdown occurs only if the fault is present long enough to activate thermal limiting.

Three possible overload conditions can occur. In the first condition, the output has been shorted before the device is enabled or between V_{IN} has been applied. The device senses the short and immediately switches into a constant-current output.

In the second condition, the short occurs while the device is enabled. At the instant the short occurs, very high currents may flow for a short time before the current-limit circuit can react . After the current-limit circuit has tripped (reached the overcurrent trip threshold) the device switches into constant-current mode.

In the third condition, the load has been gradually increased beyond the recommended operating current. The current is permitted to rise until the current-limit threshold is reached or until the thermal limit of the device is exceeded. The device is capable of delivering current up to the current-limit threshold without damage. Once the threshold has been reached, the device switches into its constant-current mode.

Fault flag (FLG)

The FLG open-drain output is asserted (active low) when an overcurrent or over-temperature condition is encountered. The output will remain asserted until the overcurrent or over-temperature condition is removed. Connecting a heavy capacitive load to an enabled device can cause momentary false over-current reporting from the inrush current flowing through the device, charging the downstream capacitor. An RC filter can be connected to the terminal to reduce false overcurrent reporting. Using low-ESR electrolytic capacitors on the output lowers the inrush current flow through the device during hot-plug events by providing a low impedance energy source, thereby reducing erroneous overcurrent reporting.

Power dissipation and junction temperature

The low on-resistance of the n-channel MOSFET allows small surface-mount packages, such as an SOIC, to pass large currents. The thermal resistance of these packages are high compared to those of power packages; it is good design practice to check power dissipation and junction temperature. The first step is to find $r_{DS(on)}$ at the input voltage and operating temperature. Next, calculate the power dissipation using:

$$P_D = r_{DS(on)} \times I^2$$

Finally, calculate the junction temperature:

$$T_J = P_D \times R_{\theta JA} + T_A$$

where:

T_A = ambient temperature °C

$R_{\theta JA}$ = thermal resistance (SOIC = 108°C/W, DIP = 60°C/W).

Thermal protection

Thermal protection prevents damage to the IC when heavy-overload or short-circuit faults are present for extended periods of time. The faults force these devices into constant-current mode, which causes the voltage across the high-side switch to increase; under short-circuit conditions, the voltage across the switch is equal to the input voltage. The increased dissipation causes the junction temperature to rise to high levels. The protection circuit senses the junction temperature of the switch and shuts it OFF. Hysteresis is built into the thermal sense circuit, and after the device has cooled approximately 20°, the switch turns back ON. The switch continues to cycle in this manner until the load fault or input power is removed.

Undervoltage lock-out (UVLO)

An undervoltage lockout ensures that the power switch is in the OFF state at power up. Whenever the input voltage falls below approximately 2 V, the power switch will be quickly turned OFF. This facilitates the design of hot-insertion systems where it is not possible to turn OFF the power switch before input power is removed. The UVLO will also keep the switch from being turned ON until the power supply has reached at least 2 V, even if the switch is enabled. Upon reinsertion, the power switch will be turned ON, with a controlled rise time to reduce EMI and voltage overshoots.

Power supply considerations

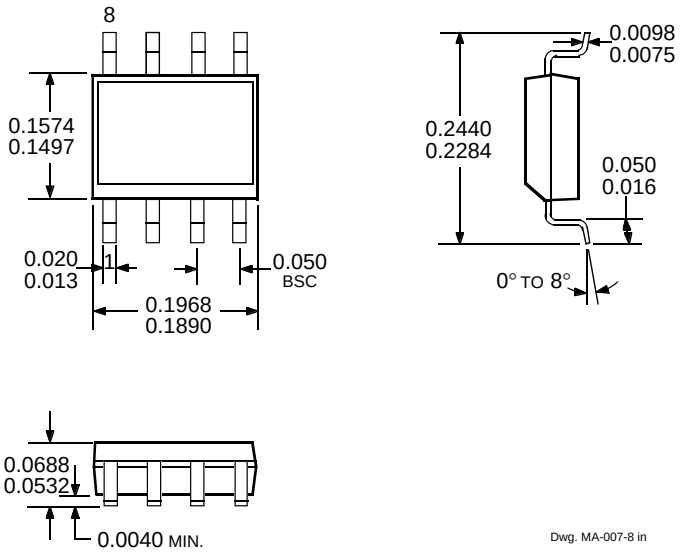
A 0.1 µF ceramic bypass capacitor between IN and GND, close to the device, is recommended. Placing a high-value electrolytic capacitor on the output terminals is also desirable when the output load is heavy. The capacitor reduces power supply transients that may cause ringing on the input. Also, bypassing the output with a 0.01 µF to 0.1 µF ceramic capacitor improves the immunity of the device to short-circuit transients.

Other

It is recommended that terminals 6 and 8 be externally tied together to ensure interchangeability with similar devices.

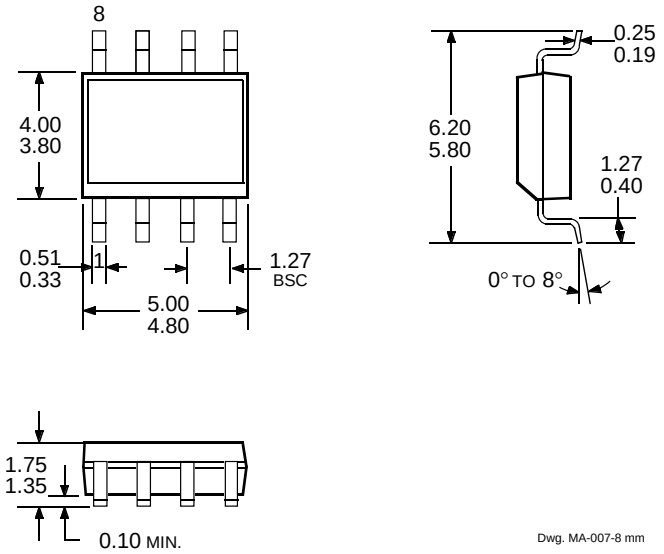
A2525EL and A2535EL

Dimensions in Inches
(for reference only)



Dwg. MA-007-8 in

Dimensions in Millimeters
(controlling dimensions)

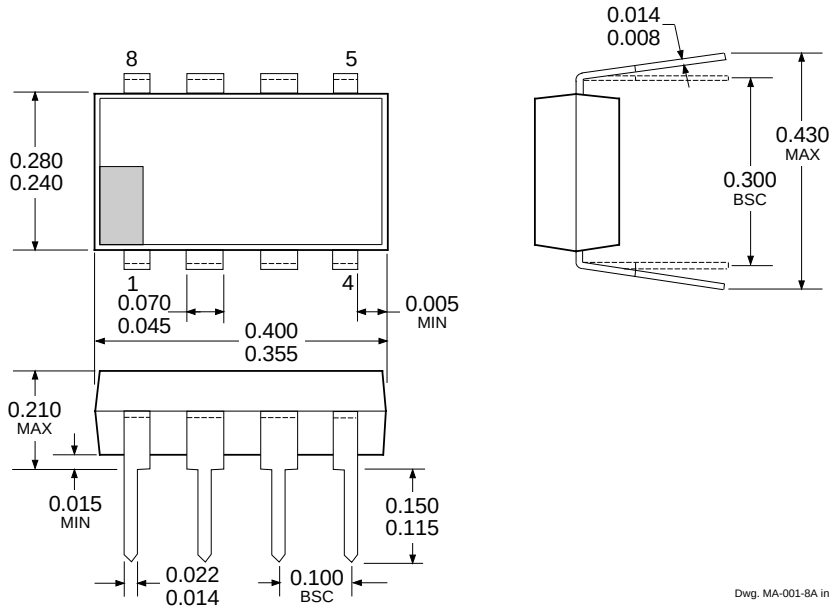


Dwg. MA-007-8 mm

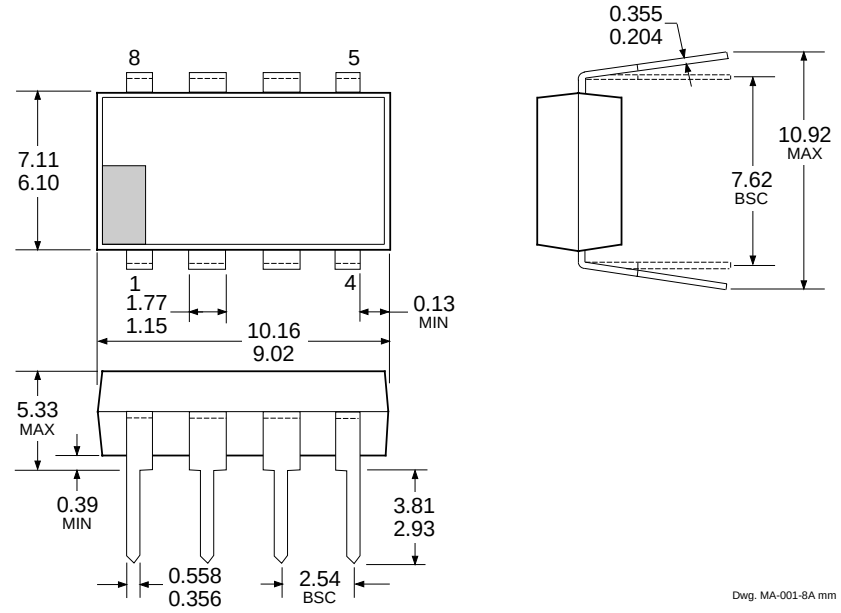
NOTES: 1. Lead spacing tolerance is non-cumulative.
2. Exact body and lead configuration at vendor's option within limits shown.

A2525EM and A2535EM

Dimensions in Inches
(controlling dimensions)



Dimensions in Millimeters
(for reference only)



NOTES: 1. Leads 1, 4, 5, and 8 may be half leads at vendor's option.
2. Lead thickness is measured at seating plane or below.
3. Lead spacing tolerance is non-cumulative.
4. Exact body and lead configuration at vendor's option within limits shown.

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POWER CONTROL
SWITCHES

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