

# 12-BIT, 2 ANALOG INPUT, 8 MSPS, SIMULTANEOUS SAMPLING ANALOG-TO-DIGITAL CONVERTER

SLAS288 – JULY 2000

## features

- Simultaneous Sampling of 2 Single-Ended Signals or 1 Differential Signal
- Signal-to-Noise Ratio: 68 dB at  $f_1 = 2$  MHz
- Differential Nonlinearity Error:  $\pm 1$  LSB
- Integral Nonlinearity Error:  $\pm 1.5$  LSB
- Auto-Scan Mode for 2 Inputs
- 3-V or 5-V Digital Interface Compatible
- Low Power: 218 mW Max at 5 V
- Power Down: 1 mW Max
- 5-V Analog Single Supply Operation
- Internal Voltage References . . . 50 PPM/ $^{\circ}$ C and  $\pm 5\%$  Accuracy
- Glueless DSP Interface
- Parallel  $\mu$ C/DSP Interface

## applications

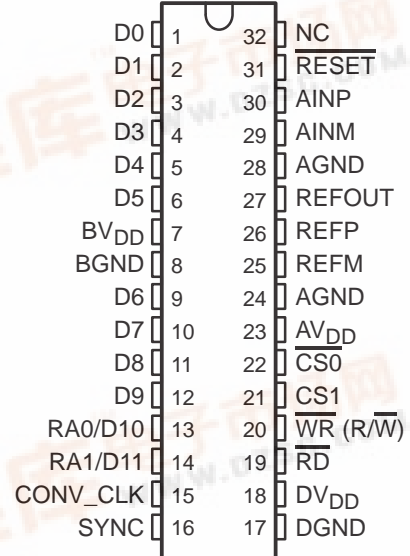
- Radar Applications
- Communications
- Control Applications
- High-Speed DSP Front-End
- Automotive Applications

## description

The THS1209 is a CMOS, low-power, 12-bit, 8 MSPS analog-to-digital converter (ADC). The speed, resolution, bandwidth, and single-supply operation are suited for applications in radar, imaging, high-speed acquisition, and communications. A multistage pipelined architecture with output error correction logic provides for no missing codes over the full operating temperature range. Internal control registers allow for programming the ADC into the desired mode. The THS1209 consists of two analog inputs, which are sampled simultaneously. These inputs can be selected individually and configured to single-ended or differential inputs. Internal reference voltages for the ADC (1.5 V and 3.5 V) are provided. An external reference can also be chosen to suit the dc accuracy and temperature drift requirements of the application.

The THS1209C is characterized for operation from  $0^{\circ}$ C to  $70^{\circ}$ C, and the THS1209I is characterized for operation from  $-40^{\circ}$ C to  $85^{\circ}$ C.

## DA PACKAGE (TOP VIEW)



## AVAILABLE OPTIONS

T <sub>A</sub>	PACKAGED DEVICE
	TSSOP (DA)
$0^{\circ}$ C to $70^{\circ}$ C	THS1209CDA
$-40^{\circ}$ C to $85^{\circ}$ C	THS1209IDA

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

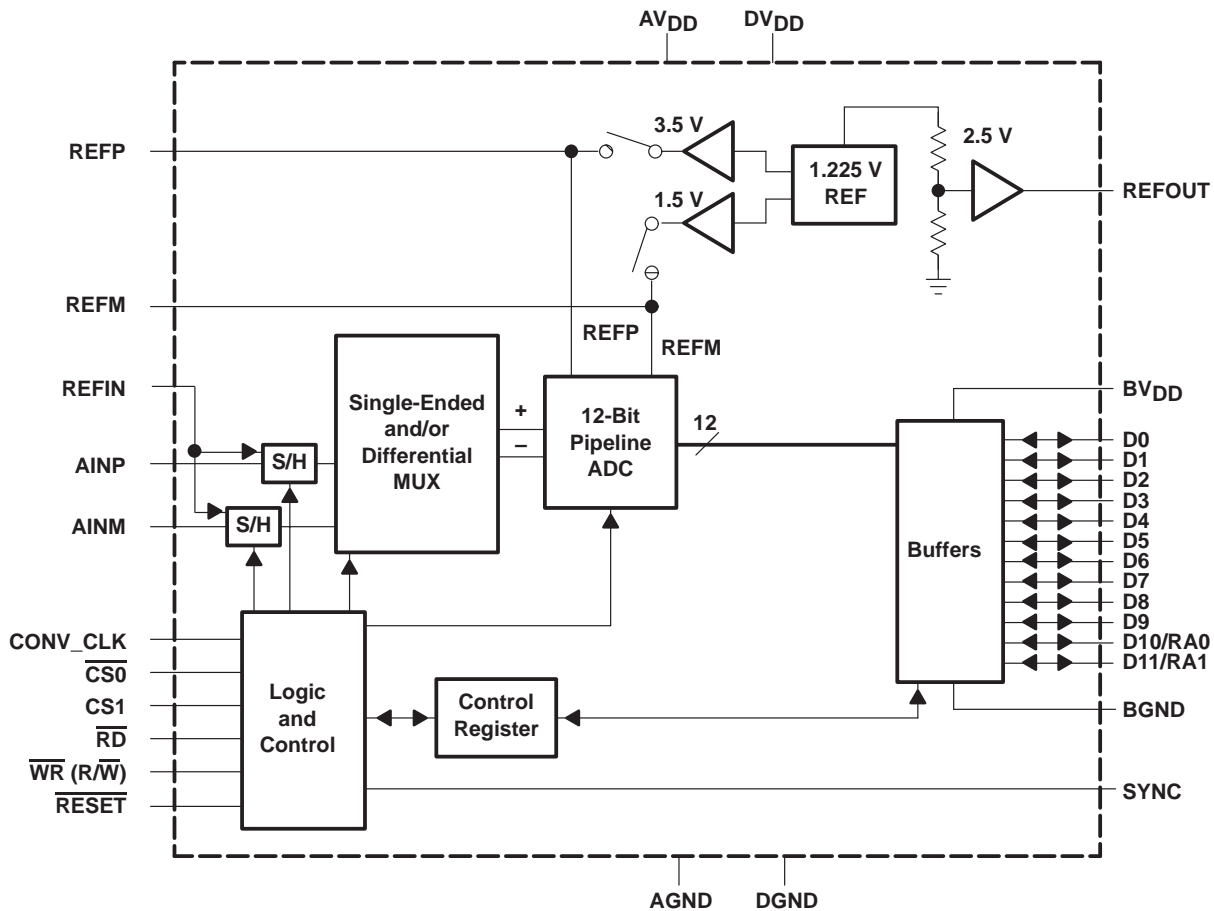


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**THS1209**  
**12-BIT, 2 ANALOG INPUT, 8 MSPS, SIMULTANEOUS SAMPLING**  
**ANALOG-TO-DIGITAL CONVERTER**

SLAS288 – JULY 2000

**functional block diagram**



THS1209  
**12-BIT, 2 ANALOG INPUT, 8 MSPS, SIMULTANEOUS SAMPLING  
 ANALOG-TO-DIGITAL CONVERTER**

SLAS288 – JULY 2000

**Terminal Functions**

TERMINAL NAME NO.		I/O	DESCRIPTION
AINP	30	I	Analog input, single-ended or positive input of differential channel A
AINM	29	I	Analog input, single-ended or negative input of differential channel A
AV <sub>DD</sub>	23	I	Analog supply voltage
AGND	24	I	Analog ground
BV <sub>DD</sub>	7	I	Digital supply voltage for buffer
BGND	8	I	Digital ground for buffer
CONV_CLK	15	I	Digital input. This input is the conversion clock input
CS0	22	I	Chip select input (active low)
CS1	21	I	Chip select input (active high)
SYNC	16	O	Synchronization output. This signal indicates in a multi-channel operation that data of channel A is brought to the digital output and can therefore be used for synchronization.
DGND	17	I	Digital ground. Ground reference for digital circuitry.
DV <sub>DD</sub>	18	I	Digital supply voltage
D0 – D9	1–6, 9–12	I/O/Z	Digital input, output; D0 = LSB
RA0/D10	13	I/O/Z	Digital input, output. The data line D10 is also used as an address line (RA0) for the control register. This is required for writing to control register 0 and control register 1. See Table 8.
RA1/D11	14	I/O/Z	Digital input, output (D11 = MSB). The data line D11 is also used as an address line (RA1) for the control register. This is required for writing to control register 0 and control register 1. See Table 8.
NC	32	O	Not connected
REFIN	28	I	Common-mode reference input for the analog input channels. It is recommended that this pin be connected to the reference output REFOUT.
REFP	26	I	Reference input, requires a bypass capacitor of 10 μF to AGND in order to bypass the internal reference voltage. An external reference voltage at this input can be applied. This option can be programmed through control register 0. See Table 9.
REFM	25	I	Reference input, requires a bypass capacitor of 10 μF to AGND in order to bypass the internal reference voltage. An external reference voltage at this input can be applied. This option can be programmed through control register 0. See Table 9.
RESET	31	I	Hardware reset of the THS1209. Sets the control register to default values.
REFOUT	27	O	Analog fixed reference output voltage of 2.5 V. Sink and source capability of 250 μA. The reference output requires a capacitor of 10 μF to AGND for filtering and stability.
RD <sup>†</sup>	19	I	The RD input is used only if the WR input is configured as a write only input. In this case, it is a digital input, active low as a data read select from the processor. See timing section.
WR (R/W) <sup>†</sup>	20	I	This input is programmable. It functions as a read-write input (R/W) and can also be configured as a write-only input (WR), which is active low and used as data write select from the processor. In this case, the RD input is used as a read input from the processor. See timing section.

<sup>†</sup> The start-conditions of RD and WR (R/W) are unknown. The first access to the ADC has to be a write access to initialize the ADC.

# THS1209

## 12-BIT, 2 ANALOG INPUT, 8 MSPS, SIMULTANEOUS SAMPLING ANALOG-TO-DIGITAL CONVERTER

SLAS288 – JULY 2000

### absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range: DGND to DV <sub>DD</sub>	–0.3 V to 8.5 V
BGND to BV <sub>DD</sub>	–0.3 V to 8.5 V
AGND to AV <sub>DD</sub>	–0.3 V to 8.5 V
Analog input voltage range	AGND – 0.3 V to AV <sub>DD</sub> + 1.5 V
Reference input voltage	–0.3 + AGND to AV <sub>DD</sub> + 0.3 V
Digital input voltage range	–0.3 V to BV <sub>DD</sub> /DV <sub>DD</sub> + 0.3 V
Operating virtual junction temperature range, T <sub>J</sub>	–40°C to 150°C
Operating free-air temperature range: THS1209C	0°C to 70°C
THS1209I	–40°C to 85°C
Storage temperature range, T <sub>stg</sub>	–85°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### recommended operating conditions

#### power supply

		MIN	NOM	MAX	UNIT
Supply voltage	AV <sub>DD</sub>	4.75	5	5.25	V
	DV <sub>DD</sub>	4.75	5	5.25	
	BV <sub>DD</sub>	3		5.25	

#### analog and reference inputs

	MIN	NOM	MAX	UNIT
Analog input voltage in single-ended configuration	V <sub>REFM</sub>		V <sub>REFP</sub>	V
Common-mode input voltage V <sub>CM</sub> in differential configuration	1	2.5	4	V
External reference voltage, V <sub>REFP</sub> (optional)		3.5	AV <sub>DD</sub> –1.2	V
External reference voltage, V <sub>REFM</sub> (optional)	1.4	1.5		V
Input voltage difference, REFP – REFM		2		V

#### digital inputs

		MIN	NOM	MAX	UNIT
High-level input voltage, V <sub>IH</sub>	BV <sub>DD</sub> = 3.3 V	2			V
	BV <sub>DD</sub> = 5.25 V	2.8			V
Low-level input voltage, V <sub>IL</sub>	BV <sub>DD</sub> = 3.3 V			0.8	V
	BV <sub>DD</sub> = 5.25 V			0.8	V
Input CONV_CLK frequency	DV <sub>DD</sub> = 4.75 V to 5.25 V	0.1		8	MHz
CONV_CLK pulse duration, clock high, t <sub>w</sub> (CONV_CLKH)	DV <sub>DD</sub> = 4.75 V to 5.25 V	62	62	5000	ns
CONV_CLK pulse duration, clock low, t <sub>w</sub> (CONV_CLKL)	DV <sub>DD</sub> = 4.75 V to 5.25 V	62	62	5000	ns
Operating free-air temperature, T <sub>A</sub>	THS1209CDA	0		70	°C
	THS1209IDA	–40		85	

THS1209  
**12-BIT, 2 ANALOG INPUT, 8 MSPS, SIMULTANEOUS SAMPLING  
 ANALOG-TO-DIGITAL CONVERTER**

SLAS288 – JULY 2000

electrical characteristics over recommended operating conditions,  $AV_{DD} = DV_{DD} = 5\text{ V}$ ,  
 $BV_{DD} = 3.3\text{ V}$  (unless otherwise noted)

**digital specifications**

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>Digital inputs</b>						
$I_{IH}$	High-level input current	$DV_{DD} = \text{digital inputs}$	-50		50	$\mu\text{A}$
$I_{IL}$	Low-level input current	Digital input = 0 V	-50		50	$\mu\text{A}$
$C_i$	Input capacitance			5		pF
<b>Digital outputs</b>						
$V_{OH}$	High-level output voltage	$I_{OH} = -50\ \mu\text{A}$ , $BV_{DD} = 3.3\text{ V}, 5\text{ V}$	$BV_{DD}-0.5$			V
$V_{OL}$	Low-level output voltage	$I_{OL} = 50\ \mu\text{A}$ , $BV_{DD} = 3.3\text{ V}, 5\text{ V}$			0.4	V
$I_{OZ}$	High-impedance-state output current	$CS1 = \text{DGND}$ , $CS0 = DV_{DD}$	-10		10	$\mu\text{A}$
$C_O$	Output capacitance			5		pF
$C_L$	Load capacitance at databus D0 – D11				30	pF

**THS1209**  
**12-BIT, 2 ANALOG INPUT, 8 MSPS, SIMULTANEOUS SAMPLING**  
**ANALOG-TO-DIGITAL CONVERTER**

SLAS288 – JULY 2000

electrical characteristics over recommended operating conditions,  $A_{VDD} = DV_{DD} = 5\text{ V}$ ,  
 $BV_{DD} = 3.3\text{ V}$ ,  $f_s = 8\text{ MSPS}$ ,  $V_{REF} = \text{internal}$  (unless otherwise noted)

**dc specifications**

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
Resolution			12			Bits	
<b>Accuracy</b>							
Integral nonlinearity, INL			±1.5			LSB	
Differential nonlinearity, DNL			±1			LSB	
Offset error		After calibration in single-ended mode	20			LSB	
		After calibration in differential mode	-20	20		LSB	
Gain error			-20	20		LSB	
<b>Analog input</b>							
Input capacitance			15			pF	
Input leakage current		$V_{AIN} = V_{REFM}$ to $V_{REFP}$	±10			µA	
<b>Internal voltage reference</b>							
Accuracy, $V_{REFP}$			3.3	3.5	3.7	V	
Accuracy, $V_{REFM}$			1.4	1.5	1.6	V	
Temperature coefficient			50			PPM/°C	
Reference noise			100			µV	
Accuracy, $REF_{OUT}$			2.475	2.5	2.525	V	
<b>Power supply</b>							
$I_{DDA}$	Analog supply current	$A_{VDD} = DV_{DD} = 5\text{ V}$ , $BV_{DD} = 3.3\text{ V}$	38			40	mA
$I_{DDD}$	Digital supply voltage	$A_{VDD} = DV_{DD} = 5\text{ V}$ , $BV_{DD} = 3.3\text{ V}$	0.5			1	mA
$I_{DDB}$	Buffer supply voltage	$A_{VDD} = DV_{DD} = 5\text{ V}$ , $BV_{DD} = 3.3\text{ V}$	1.5			4	mA
Power dissipation		$A_{VDD} = DV_{DD} = 5\text{ V}$ , $BV_{DD} = 3.3\text{ V}$	188			218	mW
Power dissipation in power down with conversion clock inactive		$A_{VDD} = DV_{DD} = 5\text{ V}$ , $BV_{DD} = 3.3\text{ V}$	0.25				mW

THS1209  
**12-BIT, 2 ANALOG INPUT, 8 MSPS, SIMULTANEOUS SAMPLING  
 ANALOG-TO-DIGITAL CONVERTER**

SLAS288 – JULY 2000

electrical characteristics over recommended operating conditions,  $V_{REF}$  = internal,  $f_s$  = 8 MSPS,  $f_I$  = 2 MHz at  $-1$ dBFS (unless otherwise noted)

ac specifications,  $AV_{DD} = DV_{DD} = 5$  V,  $BV_{DD} = 3.3$  V,  $C_L < 30$  pF

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SINAD	Signal-to-noise ratio + distortion	Differential mode	63	65		dB
		Single-ended mode	62	64		dB
SNR	Signal-to-noise ratio	Differential mode	64	69		dB
		Single-ended mode	64	68		dB
THD	Total harmonic distortion	Differential mode		-70	-67	dB
		Single-ended mode		-68	-64	dB
ENOB (SNR)	Effective number of bits	Differential mode	10.17	10.5		Bits
		Single-ended mode	10	10.3		Bits
SFDR	Spurious free dynamic range	Differential mode	67	71		dB
		Single-ended mode	65	69		dB
<b>Analog Input</b>						
	Full-power bandwidth with a source impedance of 150 $\Omega$ in differential configuration.	Full scale sinewave, $-3$ dB		98		MHz
	Full-power bandwidth with a source impedance of 150 $\Omega$ in single-ended configuration.	Full scale sinewave, $-3$ dB		54		MHz
	Small-signal bandwidth with a source impedance of 150 $\Omega$ in differential configuration.	100 mVpp sinewave, $-3$ dB		98		MHz
	Small-signal bandwidth with a source impedance of 150 $\Omega$ in single-ended configuration.	100 mVpp sinewave, $-3$ dB		54		MHz

timing specifications,  $AV_{DD} = DV_{DD} = 5$  V,  $BV_{DD} = 3.3$  V,  $V_{REF}$  = Internal,  $C_L < 30$  pF

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_d(\text{pipe})$	Latency			5		CONV CLK
$t_{su}(\text{CONV\_CLKL-READL})$	Setup time, CONV_CLK low before CS valid		10			ns
$t_{su}(\text{READH-CONV\_CLKL})$	Setup time, CS invalid to CONV_CLK low		20			ns
$t_d(\text{CONV\_CLKL-SYNCL})$	Delay time, CONV_CLK low to SYNC low				10	ns
$t_d(\text{CONV\_CLKL-SYNCH})$	Delay time, CONV_CLK low SYNC high				10	ns

# THS1209

## 12-BIT, 2 ANALOG INPUT, 8 MSPS, SIMULTANEOUS SAMPLING ANALOG-TO-DIGITAL CONVERTER

SLAS288 – JULY 2000

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### detailed description

#### reference voltage

The THS1209 has a built-in reference, which provides the reference voltages for the ADC. VREFP is set to 3.5 V and VREFM is set to 1.5 V. An external reference can also be used through two reference input pins, REFP and REFM, if the reference source is programmed as external. The voltage levels applied to these pins establish the upper and lower limits of the analog inputs to produce a full-scale and zero-scale reading respectively.

#### analog inputs

The THS1209 consists of two analog inputs, which are sampled simultaneously. These inputs can be selected individually and configured as single-ended or differential inputs. The desired analog input channel can be programmed.

#### converter

The THS1209 uses a 12-bit pipelined multistaged architecture which achieves a high sample rate with low power consumption. The THS1209 distributes the conversion over several smaller ADC sub-blocks, refining the conversion with progressively higher accuracy as the device passes the results from stage to stage. This distributed conversion requires a small fraction of the number of comparators used in a traditional flash ADC. A sample-and-hold amplifier (SHA) within each of the stages permits the first stage to operate on a new input sample while the second through the eighth stages operate on the seven preceding samples.

#### conversion

An external clock signal with a duty cycle of 50% has to be applied to the clock input (CONV\_CLK). A new conversion is started with every falling edge of the applied clock signal. The conversion values are available at the output with a latency of 5 clock cycles.

#### sampling rate

The maximum possible conversion rate per channel is dependent on the selected analog input channels. Table 1 shows the maximum conversion rate for different combinations.

**Table 1. Maximum Conversion Rate**

CHANNEL CONFIGURATION	NUMBER OF CHANNELS	MAXIMUM CONVERSION RATE PER CHANNEL
1 single-ended channel	1	8 MSPS
2 single-ended channels	2	4 MSPS
1 differential channel	1	8 MSPS
2 differential channels	2	4 MSPS
1 single-ended and 1 differential channel	2	4 MSPS

The maximum conversion rate in the continuous conversion mode per channel,  $f_c$ , is given by:

$$f_c = \frac{8 \text{ MSPS}}{\# \text{ channels}}$$



# THS1209

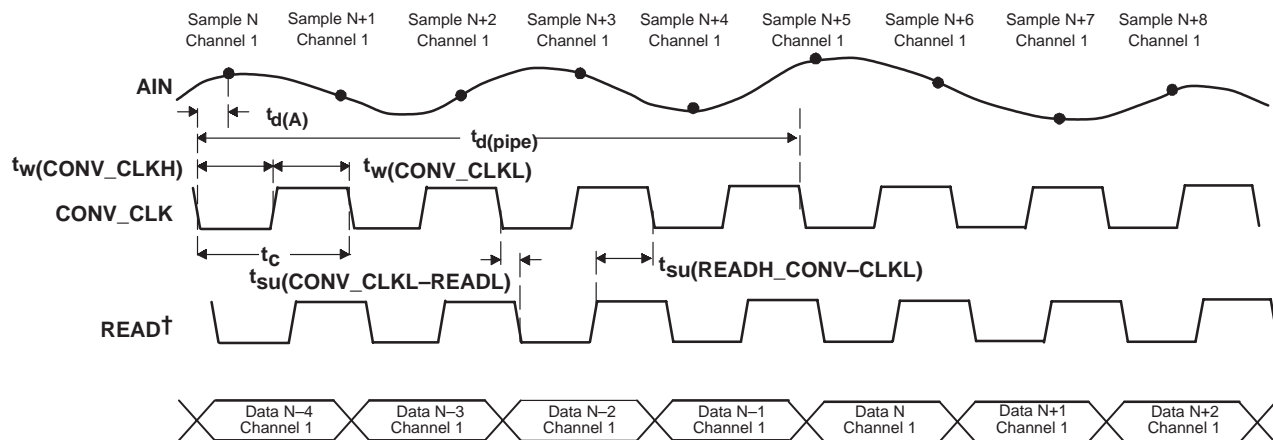
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SLAS288 – JULY 2000

### conversion mode

During conversion, the ADC operates with a free running external clock signal applied to the input CONV\_CLK. With every falling edge of the CONV\_CLK signal a new converted value is available to the databus with the corresponding read signal. The THS1209 offers up to two analog inputs to be selected. It is important to provide the channel information to the system, this means to know which channel is available to the databus. To maintain this channel integrity, the THS1209 an output signal SYNC, which is always active low if data of channel 1 is applied to the databus.

Figure 3 shows the timing of the conversion when one analog input channel is selected. The maximum throughput rate is 8 MSPS in this mode. The signal SYNC is disabled for the selection of one analog input since this information is not required for one analog input. There is a certain timing relationship required for the read signal with respect to the conversion clock. This can be seen in Figure 2 and Table 2. A more detailed description of the timing is given in the section timing and signal description of the THS1209.



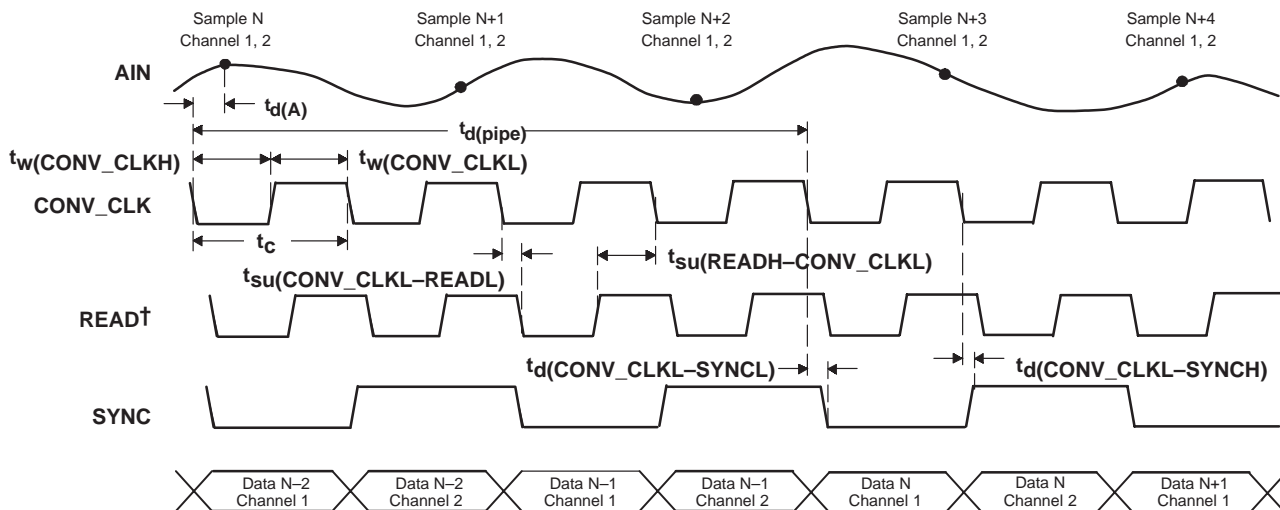
† READ is the logical combination from  $\overline{\text{CS0}}$ , CS1, and  $\overline{\text{RD}}$

**Figure 1. Conversion Timing in 1-Channel Operation**

# THS1209 12-BIT, 2 ANALOG INPUT, 8 MSPS, SIMULTANEOUS SAMPLING ANALOG-TO-DIGITAL CONVERTER

SLAS288 – JULY 2000

Figure 3 shows the conversion timing when two analog input channels are selected. The maximum throughput rate per channel is 4 MSPS in this mode. The data flow in the bottom of the figure shows the order the converted data is available to the data bus. The SYNC signal is always active low if data of channel 1 is available to the data bus. There is a certain timing relationship required for the read signal with respect to the conversion clock. This can be seen in Figure 2 and Table 2. A more detailed description of the timing is given in the section timing and signal description of the THS1209.



† READ is the logical combination from  $\overline{CS0}$ , CS1, and  $\overline{RD}$

Figure 2. Conversion Timing in 2 Channel Operation

**THS1209**  
**12-BIT, 2 ANALOG INPUT, 8 MSPS, SIMULTANEOUS SAMPLING**  
**ANALOG-TO-DIGITAL CONVERTER**

SLAS288 – JULY 2000

**digital output data format**

The digital output data format of the THS1209 can be in either binary format or in twos complement format. The following tables list the digital outputs for the analog input voltages.

**Table 2. Binary Output Format for Single-Ended Configuration**

SINGLE-ENDED, BINARY OUTPUT	
ANALOG INPUT VOLTAGE	DIGITAL OUTPUT CODE
$A_{IN} = V_{REFP}$	FFFh
$A_{IN} = (V_{REFP} + V_{REFM})/2$	800h
$A_{IN} = V_{REFM}$	000h

**Table 3. Twos Complement Output Format for Single-Ended Configuration**

SINGLE-ENDED, TWOS COMPLEMENT	
ANALOG INPUT VOLTAGE	DIGITAL OUTPUT CODE
$A_{IN} = V_{REFP}$	7FFh
$A_{IN} = (V_{REFP} + V_{REFM})/2$	000h
$A_{IN} = V_{REFM}$	800h

**Table 4. Binary Output Format for Differential Configuration**

DIFFERENTIAL, BINARY OUTPUT	
ANALOG INPUT VOLTAGE	DIGITAL OUTPUT CODE
$V_{in} = A_{INP} - A_{INM}$ $V_{REF} = V_{REFP} - V_{REFM}$	
$V_{in} = V_{REF}$	FFFh
$V_{in} = 0$	800h
$V_{in} = -V_{REF}$	000h

**Table 5. Twos Complement Output Format for Differential Configuration**

DIFFERENTIAL, BINARY OUTPUT	
ANALOG INPUT VOLTAGE	DIGITAL OUTPUT CODE
$V_{in} = A_{INP} - A_{INM}$ $V_{REF} = V_{REFP} - V_{REFM}$	
$V_{in} = V_{REF}$	7FFh
$V_{in} = 0$	000h
$V_{in} = -V_{REF}$	800h

**THS1209**  
**12-BIT, 2 ANALOG INPUT, 8 MSPS, SIMULTANEOUS SAMPLING**  
**ANALOG-TO-DIGITAL CONVERTER**

SLAS288 – JULY 2000

**ADC control register**

The THS1209 contains two 10-bit wide control registers (CR0, CR1) in order to program the device into the desired mode. The bit definitions of both control registers are shown in Table 7.

**Table 6. Bit Definitions of Control Register CR0 and CR1**

BIT	BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
<b>CR0</b>	TEST1	TEST0	SCAN	DIFF1	DIFF0	CHSEL1	CHSEL0	PD	RES	VREF
<b>CR1</b>	RBACK	OFFSET	BIN/2's	R/W	RES	RES	RES	RES	RES	RESET

**writing to control register 0 and control register 1**

The 10-bit wide control register 0 and control register 1 can be programmed by addressing the desired control register and writing the register value to the ADC. The addressing is performed with the upper data bits D10 and D11, which function in this case as address lines RA0 and RA1. During this write process, the data bits D0 to D9 contain the desired control register value. Table 8 shows the addressing of each control register.

**Table 7. Control Register Addressing**

D0 – D9	D10/RA0	D11/RA1	Addressed Control Register
Desired register value	0	0	Control register 0
Desired register value	1	0	Control register 1
Desired register value	0	1	Reserved for future
Desired register value	1	1	Reserved for future

initialization of the THS1209

The initialization of the THS1209 should be done according to the configuration flow shown in Figure 3.

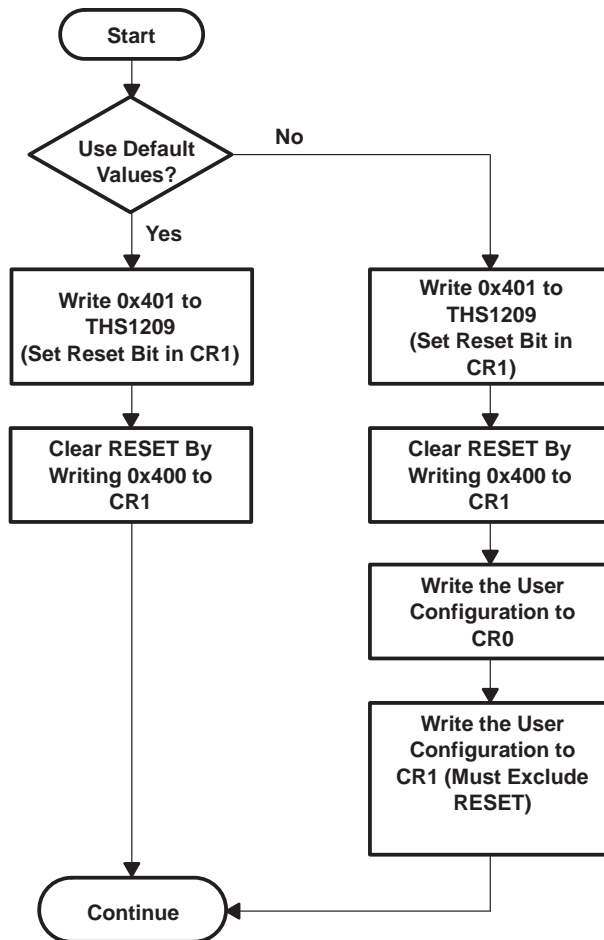


Figure 3. THS1209 Configuration Flow

**THS1209**  
**12-BIT, 2 ANALOG INPUT, 8 MSPS, SIMULTANEOUS SAMPLING**  
**ANALOG-TO-DIGITAL CONVERTER**

SLAS288 – JULY 2000

**ADC control registers**

**control register 0 (see Table 8)**

-	-	BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
-	-	TEST1	TEST0	SCAN	DIFF1	DIFF0	CHSEL1	CHSEL0	PD	RES	VREF

**Table 8. Control Register 0 Bit Functions**

BITS	RESET VALUE	NAME	FUNCTION
0	0	VREF	Vref select: Bit 0 = 0 → The internal reference is selected. Bit 0 = 1 → The external reference voltage is selected.
1	0	RES	Reserved
2	0	PD	Power down. Bit 2 = 0 → The ADC is active. Bit 2 = 1 → Power down The reading and writing to and from the digital outputs is possible during power down.
3, 4	0,0	CHSEL0, CHSEL1	Channel select Bit 3 and bit 4 select the analog input channel of the ADC. Refer to Table 8.
5,6	1,0	DIFF0, DIFF1	Number of differential channels Bit 5 and bit 6 contain information about the number of selected differential channels. Refer to Table 8.
7	0	SCAN	Autoscan enable Bit 7 enables or disables the autoscan function of the ADC. Refer to Table 8.
8,9	0,0	TEST0, TEST1	Test input enable Bit 8 and bit 9 control the test function of the ADC. Three different test voltages can be measured. This feedback allows the check of all hardware connections and the ADC operation. Refer to Table 8 for selection of the three different test voltages.

**THS1209**  
**12-BIT, 2 ANALOG INPUT, 8 MSPS, SIMULTANEOUS SAMPLING**  
**ANALOG-TO-DIGITAL CONVERTER**

SLAS288 – JULY 2000

**analog input channel selection**

The analog input channels of the THS1209 can be selected via bits 3 to 7 of control register 0. One single channel (single-ended or differential) is selected via bit 3 and bit 4 of control register 0. Bit 5 controls the selection between single-ended and differential configuration. Bit 6 and bit 7 select the autoscan mode, if more than one input channel is selected. Table 10 shows the possible selections.

**Table 9. Analog Input Channel Configurations**

BIT 7 AS	BIT 6 DF1	BIT 5 DF0	BIT 4 CHS1	BIT 3 CHS0	DESCRIPTION OF THE SELECTED INPUTS
0	0	0	0	0	Analog input AINP (single ended)
0	0	0	0	1	Analog input AINM (single ended)
0	0	0	1	0	Reserved
0	0	0	1	1	Reserved
0	0	1	0	0	Differential channel (AINP–AINM)
0	0	1	0	1	Reserved
1	0	0	0	1	Autoscan two single ended channels: AINP, AINM, AINP, ...
1	0	0	1	0	Reserved
1	0	0	1	1	Reserved
1	1	0	0	1	Reserved
1	0	1	0	1	Reserved
1	0	1	1	0	Reserved
0	0	1	1	0	Reserved
0	0	1	1	1	Reserved
1	0	0	0	0	Reserved
1	0	1	0	0	Reserved
1	0	1	1	1	Reserved
1	1	0	0	0	Reserved
1	1	0	1	0	Reserved
1	1	0	1	1	Reserved
1	1	1	0	0	Reserved
1	1	1	0	1	Reserved
1	1	1	1	0	Reserved
1	1	1	1	1	Reserved

**test mode**

The test mode of the ADC is selected via bit 8 and bit 9 of control register 0. The different selections are shown in Table 11.

**Table 10. Test Mode**

BIT 9 TEST1	BIT 8 TEST0	OUTPUT RESULT
0	0	Normal mode
0	1	$V_{REFP}$
1	0	$((V_{REFM})+(V_{REFP}))/2$
1	1	$V_{REFM}$

Three different options can be selected. This feature allows support testing of hardware connections between the ADC and the processor.

**THS1209**  
**12-BIT, 2 ANALOG INPUT, 8 MSPS, SIMULTANEOUS SAMPLING**  
**ANALOG-TO-DIGITAL CONVERTER**

SLAS288 – JULY 2000

**analog input channel selection (continued)**

**control register 1 (see Table 8)**

–	–	<b>BIT 9</b>	<b>BIT 8</b>	<b>BIT 7</b>	<b>BIT 6</b>	<b>BIT 5</b>	<b>BIT 4</b>	<b>BIT 3</b>	<b>BIT 2</b>	<b>BIT 1</b>	<b>BIT 0</b>
–	–	RBACK	OFFSET	BIN/2s	R/W	RES	RES	RES	RES	RES	RESET

**Table 11. Control Register 1 Bit Functions**

<b>BITS</b>	<b>RESET VALUE</b>	<b>NAME</b>	<b>FUNCTION</b>
0	0	RESET	Reset Writing a 1 into this bit resets the device and sets the control register 0 and control register 1 to the reset values. To bring the device out of reset, a 0 has to be written into this bit.
1	0	RES	Always write 0
2, 3	0,0	RES	Always write 0
4	1	RES	Always write 0
5	1	RES	Always write 0
6	0	R/W	R/W, RD/WR selection Bit 6 of control register 1 controls the function of the inputs RD and WR. When bit 6 in control register 1 is set to 1, WR becomes a R/W input and RD is disabled. From now on a read is signalled with R/W high and a write with R/W as a low signal. If bit 6 in control register 1 is set to 0, the input RD becomes a read input and the input WR becomes a write input.
7	0	BIN/2s	Complement select If bit 7 of control register 1 is set to 0, the output value of the ADC is in twos complement. If bit 7 of control register 1 is set to 1, the output value of the ADC is in binary format. Refer to Table 20 through Table 23.
8	0	OFFSET	Offset cancellation mode Bit 8 = 0 → normal conversion mode Bit 8 = 1 → offset calibration mode If a 1 is written into bit 8 of control register 1, the device internally sets the inputs to zero and does a conversion. The conversion result is stored in an offset register and subtracted from all conversions in order to reduce the offset error.
9	0	RBACK	Debug mode Bit 9 = 0 → normal conversion mode Bit 9 = 1 → enable debug mode When bit 9 of control register 1 is set to 1, debug mode is enabled. In this mode, the contents of control register 0 and control register 1 can be read back. The first read after bit 9 is set to 1 contains the value of control register 0. The second read after bit 9 is set to 1 contains the value of control register 1. To bring the device back into normal conversion mode, this bit has to be set back to 0 by writing again to control register 1.



THS1209  
12-BIT, 2 ANALOG INPUT, 8 MSPS, SIMULTANEOUS SAMPLING  
ANALOG-TO-DIGITAL CONVERTER

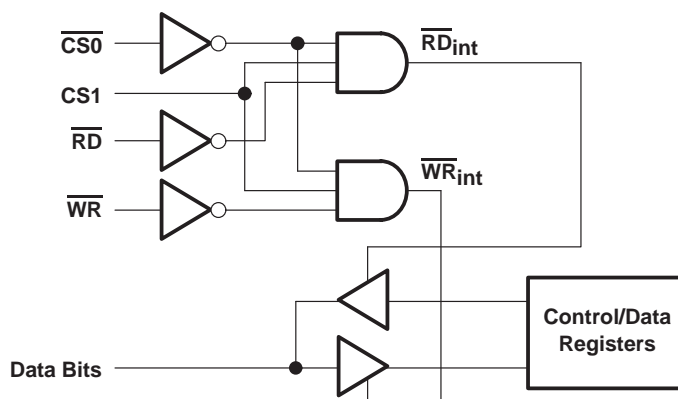
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**timing and signal description of the THS1209**

The reading from the THS1209 and writing to the THS1209 is performed by using the chip select inputs ( $\overline{CS0}$ ,  $CS1$ ), the write input  $\overline{WR}$  and the read input  $\overline{RD}$ . The write input is configurable to a combined read/write input ( $\overline{R/\overline{W}}$ ). This is desired in cases where the connected processor consists of a combined read/write output signal ( $\overline{R/\overline{W}}$ ). The two chip select inputs can be used to interface easily to a processor.

Reading from the THS1209 takes place by an internal  $\overline{RD}_{int}$  signal, which is generated from the logical combination of the external signals  $\overline{CS0}$ ,  $CS1$  and  $\overline{RD}$  (see Figure 4). This signal is then used to strobe the words out and to enable the output buffers. The last external signal (either  $\overline{CS0}$ ,  $CS1$  or  $\overline{RD}$ ) to become valid will make  $\overline{RD}_{int}$  active while the write input ( $\overline{WR}$ ) is inactive. The first of those external signals going to its inactive state will then deactivate  $\overline{RD}_{int}$  again.

Writing to the THS1209 takes place by an internal  $\overline{WR}_{int}$  signal, which is generated from the logical combination of the external signals  $\overline{CS0}$ ,  $CS1$  and  $\overline{WR}$ . This signal is then used to strobe the control words into the control registers 0 and 1. The last external signal (either  $\overline{CS0}$ ,  $CS1$  or  $\overline{WR}$ ) to become valid will make  $\overline{WR}_{int}$  active while the read input ( $\overline{RD}$ ) is inactive. The first of those external signals going to its inactive state will then deactivate  $\overline{WR}_{int}$  again.



**Figure 4. Logical Combination of  $\overline{CS0}$ ,  $CS1$ ,  $\overline{RD}$ , and  $\overline{WR}$**

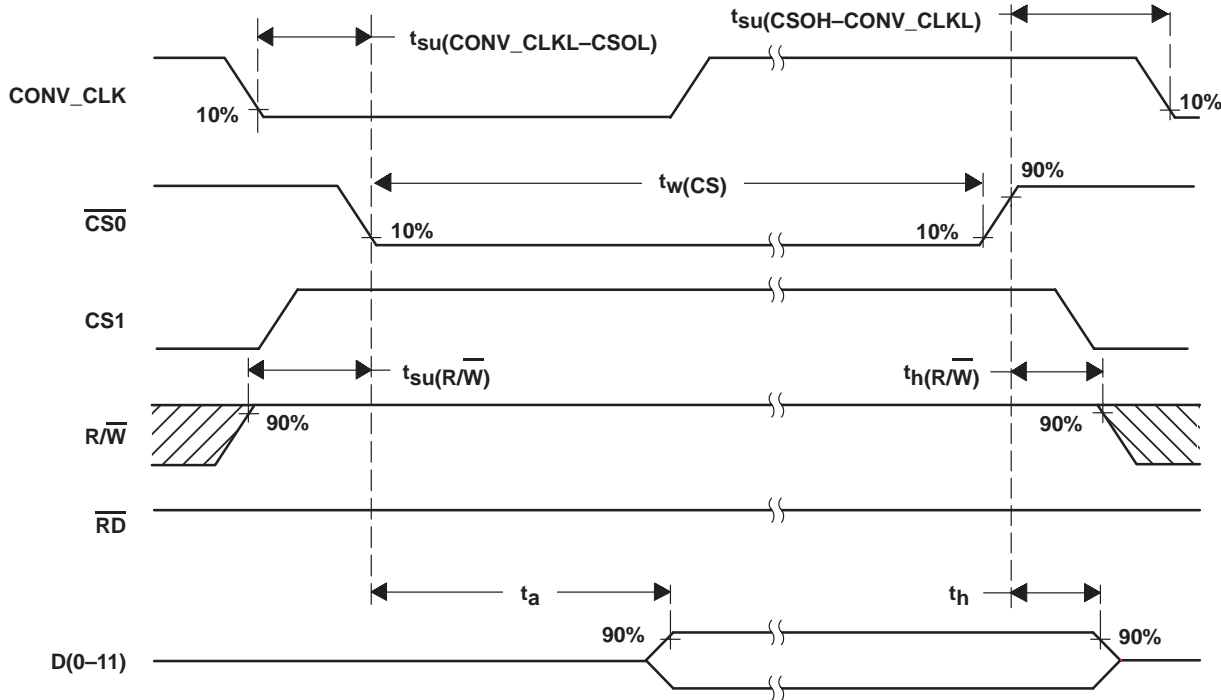
**THS1209**  
**12-BIT, 2 ANALOG INPUT, 8 MSPS, SIMULTANEOUS SAMPLING**  
**ANALOG-TO-DIGITAL CONVERTER**

SLAS288 – JULY 2000

**timing and signal description of the THS1209 (continued)**

**read timing (using  $\overline{R/\overline{W}}$ ,  $\overline{CS0}$ -controlled)**

Figure 5 shows the read-timing behavior when the  $\overline{WR}(\overline{R/\overline{W}})$  input is programmed as a combined read-write input  $\overline{R/\overline{W}}$ . The  $\overline{RD}$  input has to be tied to high-level in this configuration. This timing is called  $\overline{CS0}$ -controlled because  $\overline{CS0}$  is the last external signal of  $\overline{CS0}$ , CS1, and  $\overline{R/\overline{W}}$  which becomes valid. The reading of the data should be done with a certain timing relative to the conversion clock CONV\_CLK, as illustrated in Figure 5.



**Figure 5. Read Timing Diagram Using  $\overline{R/\overline{W}}$  ( $\overline{CS0}$ -controlled)**

**read timing parameter ( $\overline{CS0}$ -controlled)†**

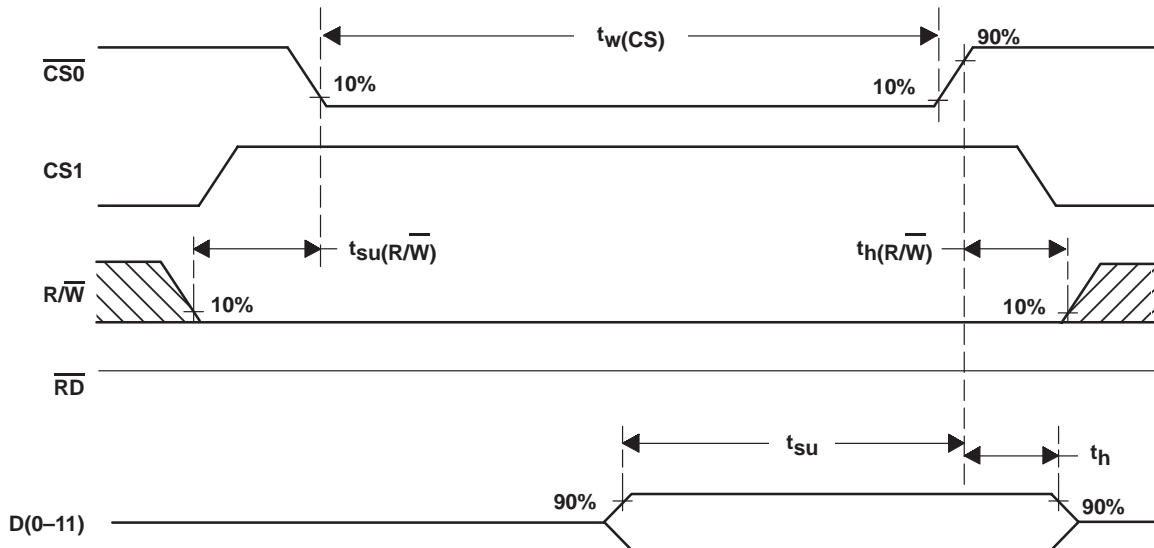
PARAMETER	MIN	TYP	MAX	UNIT
$t_{su}(CONV\_CLKL\_CSOL)$	10			ns
$t_{su}(CSOH-CONV\_CLKL)$	20			ns
$t_{su}(R/\overline{W})$	0			ns
$t_a$	0		10	ns
$t_h$	0		5	ns
$t_h(R/\overline{W})$	5			ns
$t_w(CS)$	10			ns

† CS =  $\overline{CS0}$

**timing and signal description of the THS1209 (continued)**

**write timing (using  $\overline{R/\overline{W}}$ ,  $\overline{CS0}$ -controlled)**

Figure 12 shows the write-timing behavior when the  $\overline{WR}(\overline{R/\overline{W}})$  input is programmed as a combined read-write input  $\overline{R/\overline{W}}$ . The  $\overline{RD}$  input has to be tied to high-level in this configuration. This timing is called  $\overline{CS0}$ -controlled because  $\overline{CS0}$  is the last external signal of  $\overline{CS0}$ ,  $\overline{CS1}$ , and  $\overline{R/\overline{W}}$  which becomes valid. The writing to the THS1209 can be performed irrespective of the conversion clock signal  $\text{CONV\_CLK}$ .



**Figure 6. Write Timing Diagram Using  $\overline{R/\overline{W}}$  ( $\overline{CS0}$ -controlled)**

**write timing parameter ( $\overline{CS0}$ -controlled)**

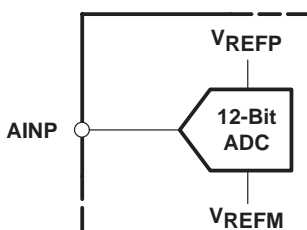
PARAMETER		MIN	TYP	MAX	UNIT
$t_{su}(\overline{R/\overline{W}})$	Setup time, $\overline{R/\overline{W}}$ stable to last CS valid	0			ns
$t_{su}$	Setup time, data valid to first CS invalid	5			ns
$t_h$	Hold time, first CS invalid to data invalid	2			ns
$t_h(\overline{R/\overline{W}})$	Hold time, first CS invalid to $\overline{R/\overline{W}}$ change	5			ns
$t_w(\overline{CS})$	Pulse duration, CS active	10			ns

**THS1209**  
**12-BIT, 2 ANALOG INPUT, 8 MSPS, SIMULTANEOUS SAMPLING**  
**ANALOG-TO-DIGITAL CONVERTER**  
 SLAS288 – JULY 2000

**analog input configuration and reference voltage**

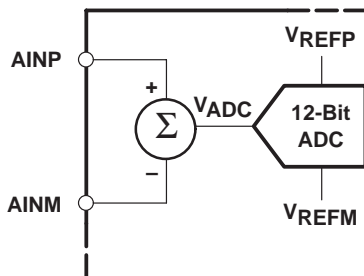
The THS1209 features two analog input channels. These can be configured for either single-ended or differential operation. Figure 7 shows a simplified model, where a single-ended configuration for channel AINP is selected. The reference voltages for the ADC itself are  $V_{REFP}$  and  $V_{REFM}$  (either internal or external reference voltage). The analog input voltage range goes from  $V_{REFM}$  to  $V_{REFP}$ . This means that  $V_{REFM}$  defines the minimum voltage, and  $V_{REFP}$  defines the maximum voltage, which can be applied to the ADC. The internal reference source provides the voltage  $V_{REFM}$  of 1.5 V and the voltage  $V_{REFP}$  of 3.5 V. The resulting analog input voltage swing of 2 V can be expressed by:

$$V_{REFM} \leq AINP \leq V_{REFP} \tag{1}$$



**Figure 7. Single-Ended Input Stage**

A differential operation is desired for many applications due to a better signal-to-noise ratio. Figure 8 shows a simplified model for the analog inputs AINM and AINP, which are configured for differential operation. The differential operation mode provides in terms of performance benefits over the single-ended mode and is therefore recommended for best performance. The THS1209 offers 1 differential analog input and in the single-ended mode 2 analog inputs. If the analog input architecture is differential, common-mode noise and common-mode voltages can be rejected. Additional details for both modes are given below.



**Figure 8. Differential Input Stage**

In comparison to the single-ended configuration it can be seen that the voltage,  $V_{ADC}$ , which is applied at the input of the ADC, is the difference between the input AINP and AINM. The voltage  $V_{ADC}$  can be calculated as follows:

$$V_{ADC} = \text{ABS}(AINP - AINM) \tag{2}$$

An advantage to single-ended operation is that the common-mode voltage

### analog input configuration and reference voltage (continued)

$$V_{CM} = \frac{AINM + AINP}{2} \quad (3)$$

can be rejected in the differential configuration, if the following condition for the analog input voltages is true:

$$AGND \leq AINM, \quad AINP \leq AV_{DD} \quad (4)$$

$$1 \text{ V} \leq V_{CM} \leq 4 \text{ V} \quad (5)$$

### single-ended mode of operation

The THS1209 can be configured for single-ended operation using dc or ac coupling. In every case, the input of the THS1209 should be driven from an operational amplifier that does not degrade the ADC performance. Because the THS1209 operates from a 5-V single supply, it is necessary to level-shift ground-based bipolar signals to comply with its input requirements. This can be achieved with dc- and ac-coupling.

# THS1209 12-BIT, 2 ANALOG INPUT, 8 MSPS, SIMULTANEOUS SAMPLING ANALOG-TO-DIGITAL CONVERTER

SLAS288 – JULY 2000

## dc coupling

An operational amplifier can be configured to shift the signal level according to the analog input voltage range of the THS1209. The analog input voltage range of the THS1209 goes from 1.5 V to 3.5 V. An op-amp can be used as shown in Figure 9.

Figure 9 shows an example where the analog input signal in the range from  $-1\text{ V}$  up to  $1\text{ V}$  is shifted by an operational amplifier to the analog input range of the THS1209 ( $1.5\text{ V}$  to  $3.5\text{ V}$ ). The operational amplifier is configured as an inverting amplifier with a gain of  $-1$ . The required dc voltage of  $1.25\text{ V}$  at the noninverting input is derived from the  $2.5\text{-V}$  output reference REFOUT of the THS1209 by using a resistor divider. Therefore, the op-amp output voltage is centered at  $2.5\text{ V}$ . The  $10\text{ }\mu\text{F}$  tantalum capacitor is required for bypassing REFOUT. REFIN of the THS1209 must be connected directly to REFOUT in single-ended mode. The use of ratio matched, thin-film resistor networks minimizes gain and offset errors.

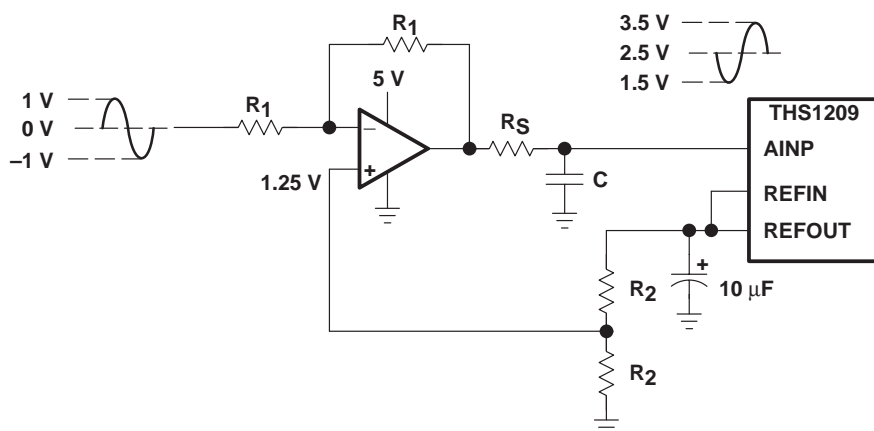


Figure 9. Level-Shift for DC-Coupled Input

## differential mode of operation

For the differential mode of operation, a conversion from single-ended to differential is required. A conversion to differential signals can be achieved by using an RF-transformer, which provides a center tap. Best performance is achieved in differential mode.

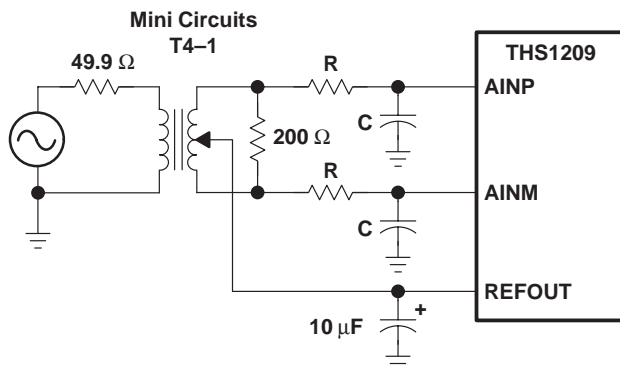


Figure 10. Transformer Coupled Input

THS1209  
12-BIT, 2 ANALOG INPUT, 8 MSPS, SIMULTANEOUS SAMPLING  
ANALOG-TO-DIGITAL CONVERTER

SLAS288 – JULY 2000

TYPICAL CHARACTERISTICS

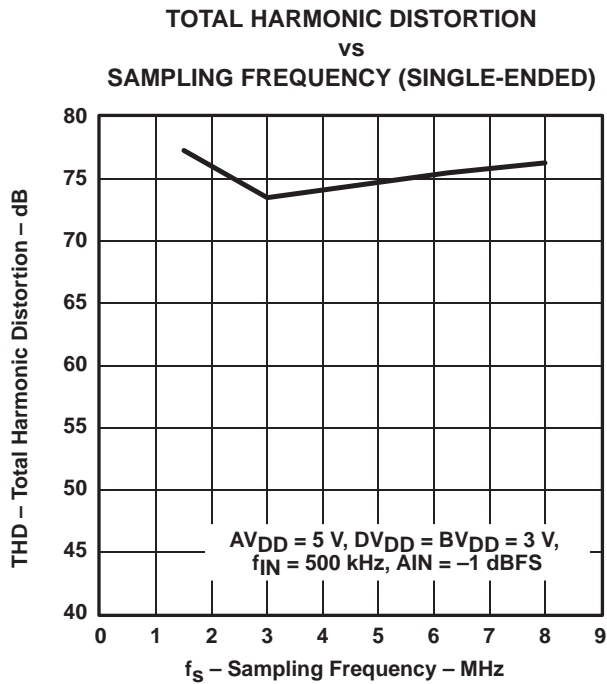


Figure 11

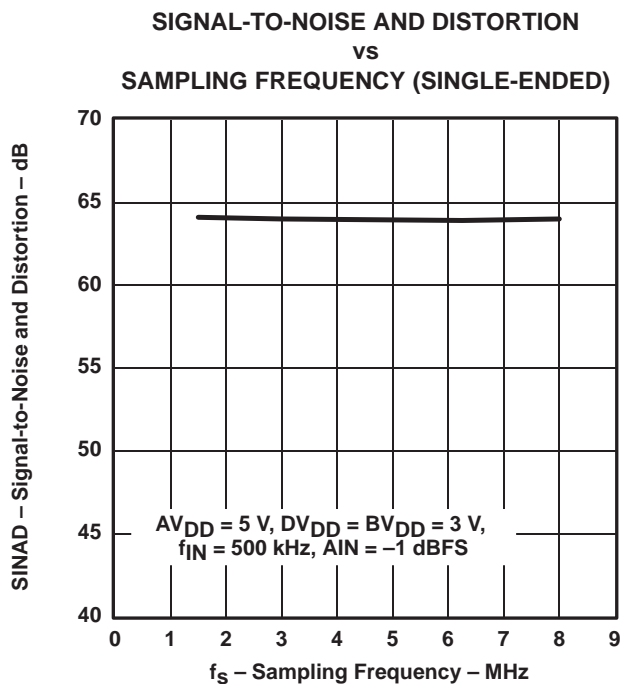


Figure 12

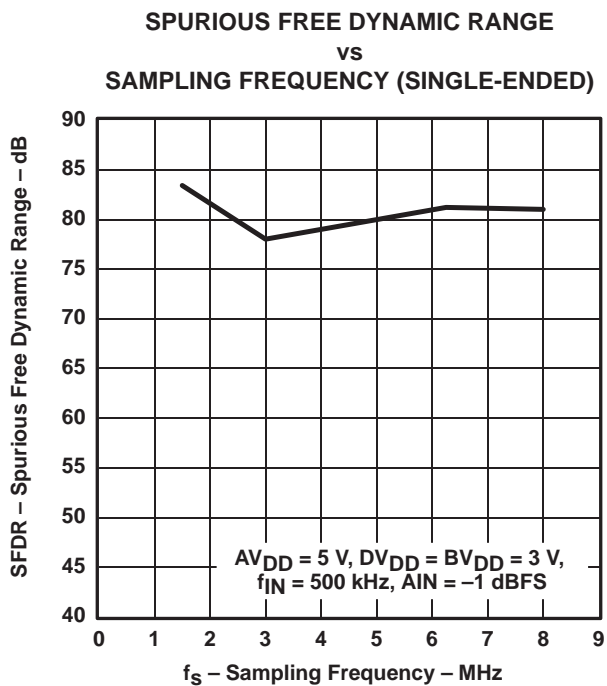


Figure 13

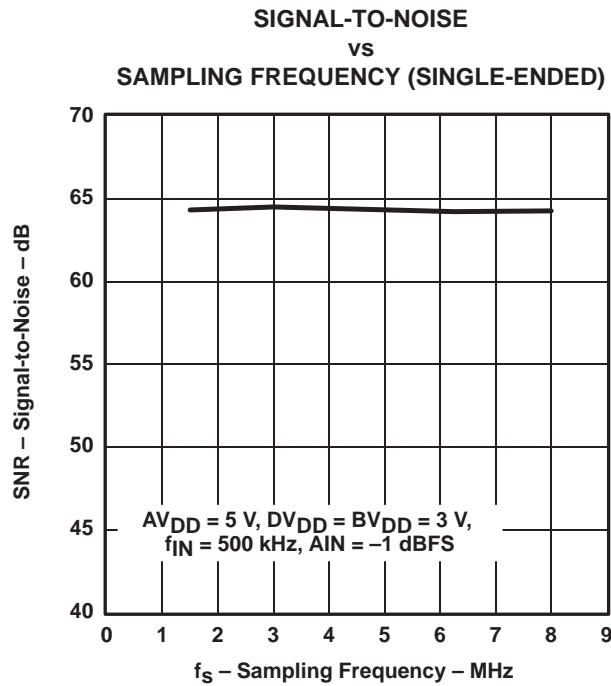
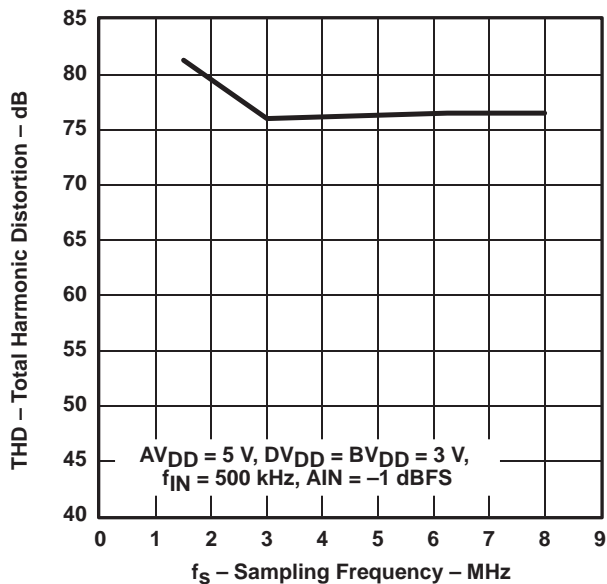


Figure 14

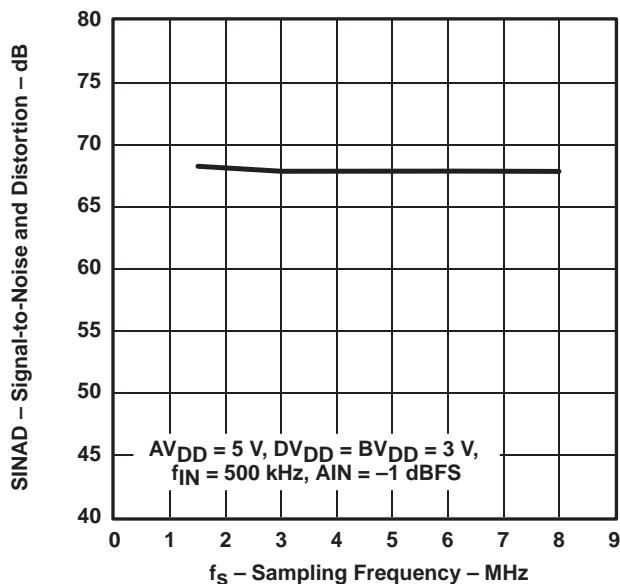
**TYPICAL CHARACTERISTICS**

**TOTAL HARMONIC DISTORTION**  
 vs  
**SAMPLING FREQUENCY (DIFFERENTIAL)**



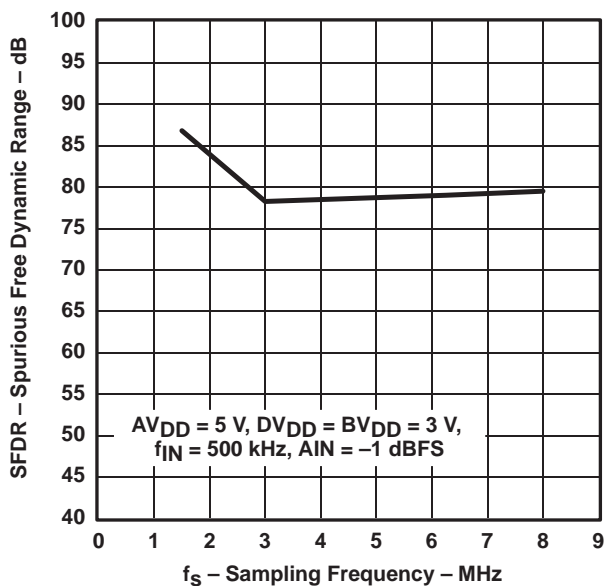
**Figure 15**

**SIGNAL-TO-NOISE AND DISTORTION**  
 vs  
**SAMPLING FREQUENCY (DIFFERENTIAL)**



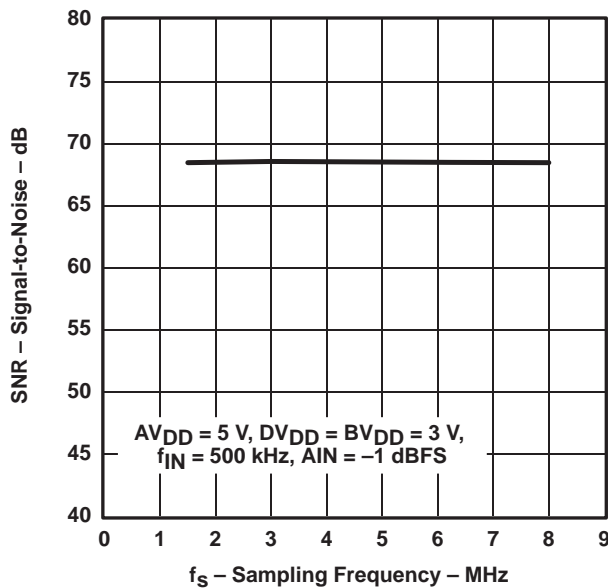
**Figure 16**

**SPURIOUS FREE DYNAMIC RANGE**  
 vs  
**SAMPLING FREQUENCY (DIFFERENTIAL)**



**Figure 17**

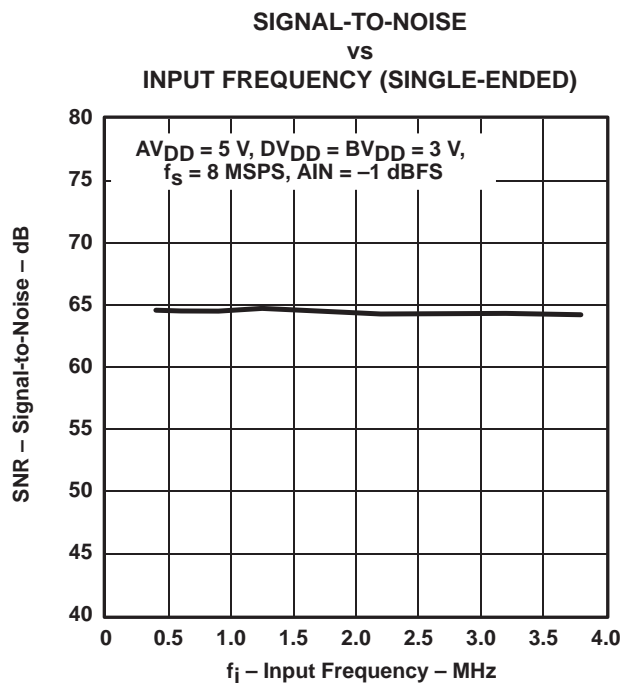
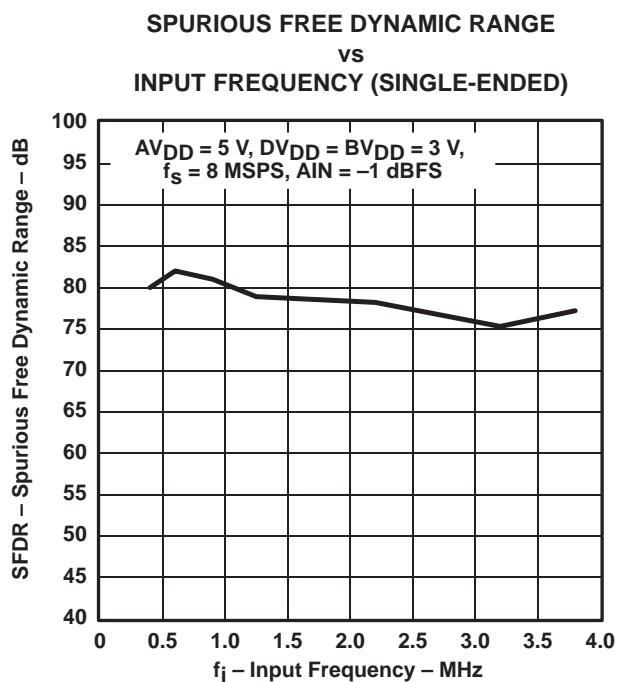
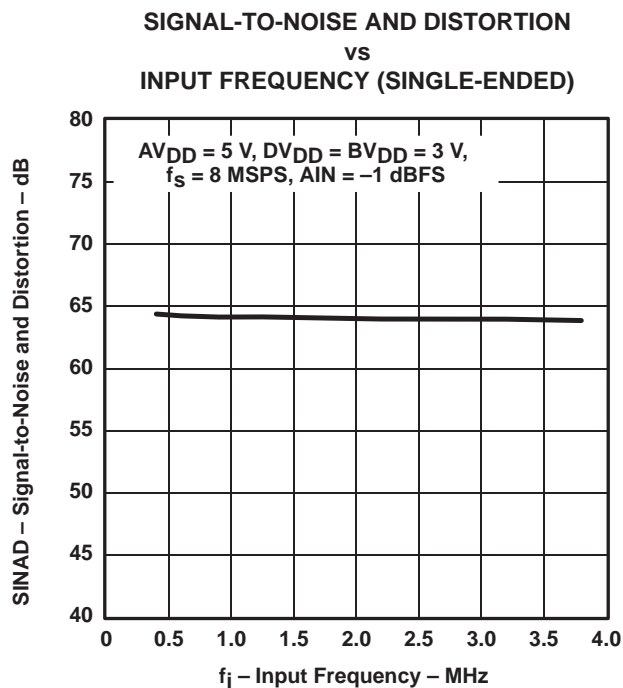
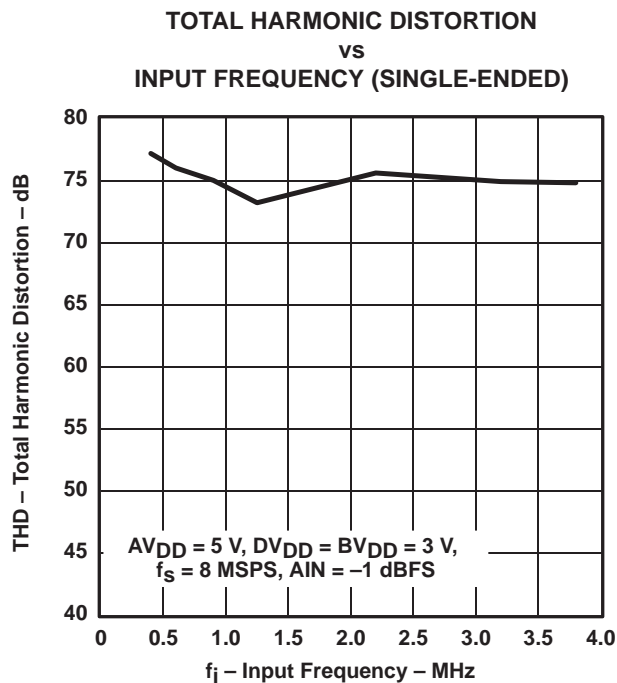
**SIGNAL-TO-NOISE**  
 vs  
**SAMPLING FREQUENCY (DIFFERENTIAL)**



**Figure 18**



**TYPICAL CHARACTERISTICS**

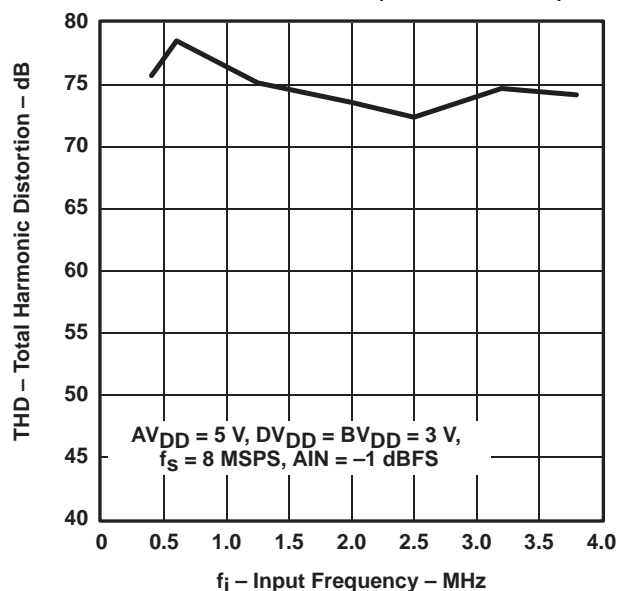


**THS1209**  
**12-BIT, 2 ANALOG INPUT, 8 MSPS, SIMULTANEOUS SAMPLING**  
**ANALOG-TO-DIGITAL CONVERTER**

SLAS288 – JULY 2000

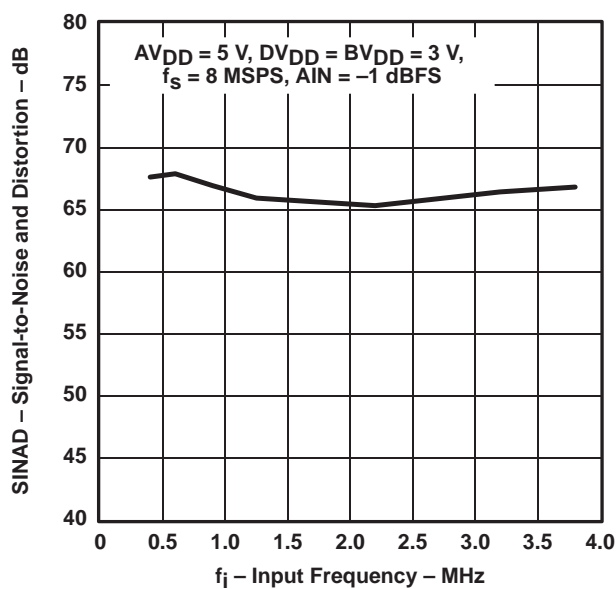
**TYPICAL CHARACTERISTICS**

**TOTAL HARMONIC DISTORTION**  
**vs**  
**INPUT FREQUENCY (DIFFERENTIAL)**



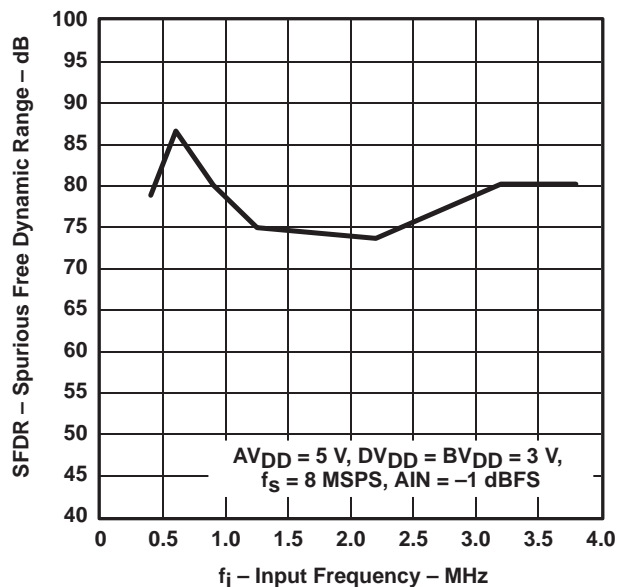
**Figure 23**

**SIGNAL-TO-NOISE AND DISTORTION**  
**vs**  
**INPUT FREQUENCY (DIFFERENTIAL)**



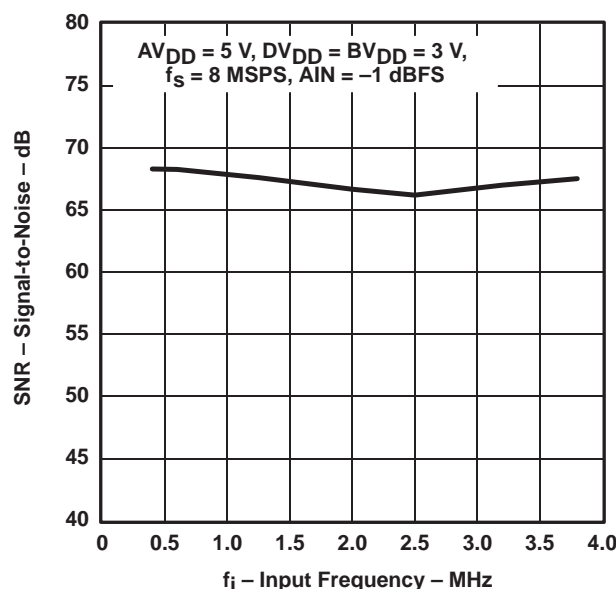
**Figure 24**

**SPURIOUS FREE DYNAMIC RANGE**  
**vs**  
**INPUT FREQUENCY (DIFFERENTIAL)**



**Figure 25**

**SIGNAL-TO-NOISE**  
**vs**  
**INPUT FREQUENCY (DIFFERENTIAL)**



**Figure 26**

THS1209  
12-BIT, 2 ANALOG INPUT, 8 MSPS, SIMULTANEOUS SAMPLING  
ANALOG-TO-DIGITAL CONVERTER

SLAS288 – JULY 2000

TYPICAL CHARACTERISTICS

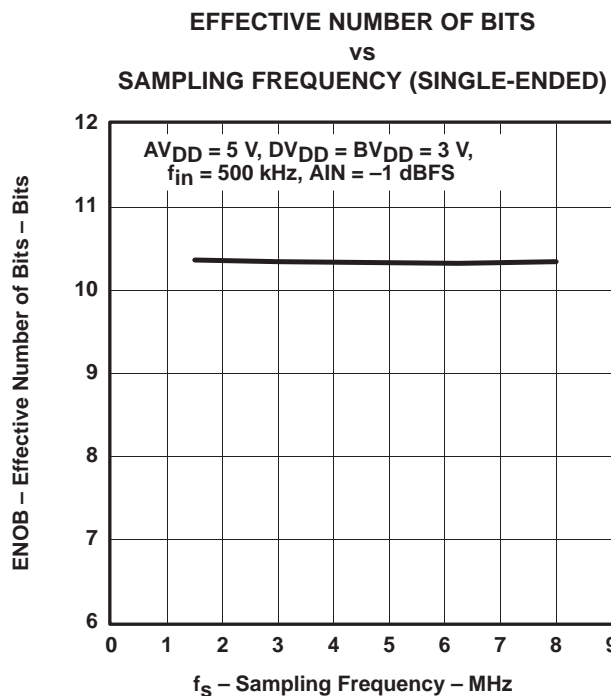


Figure 27

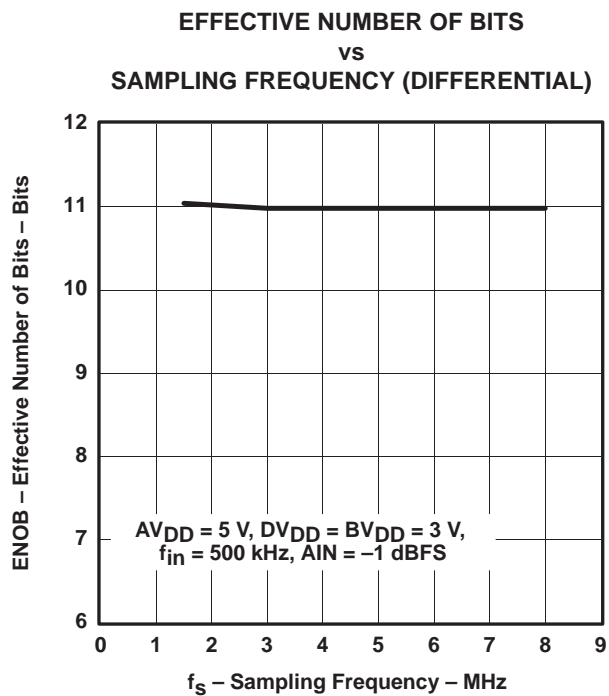


Figure 28

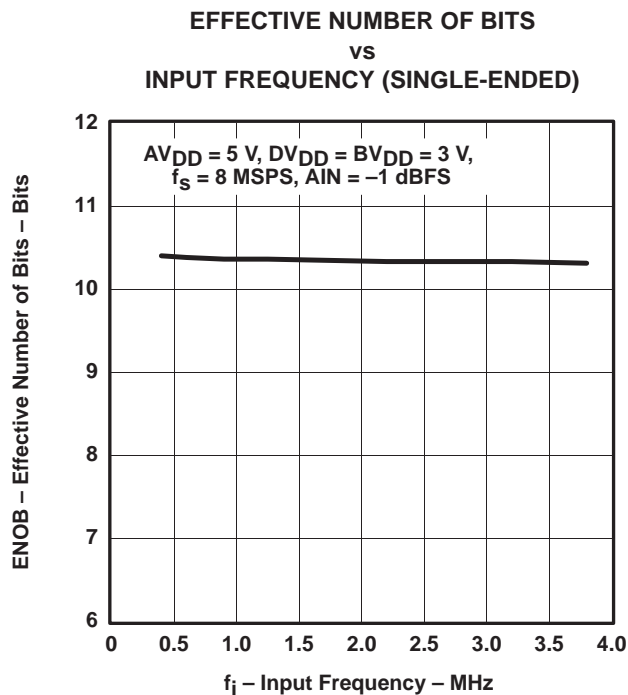


Figure 29

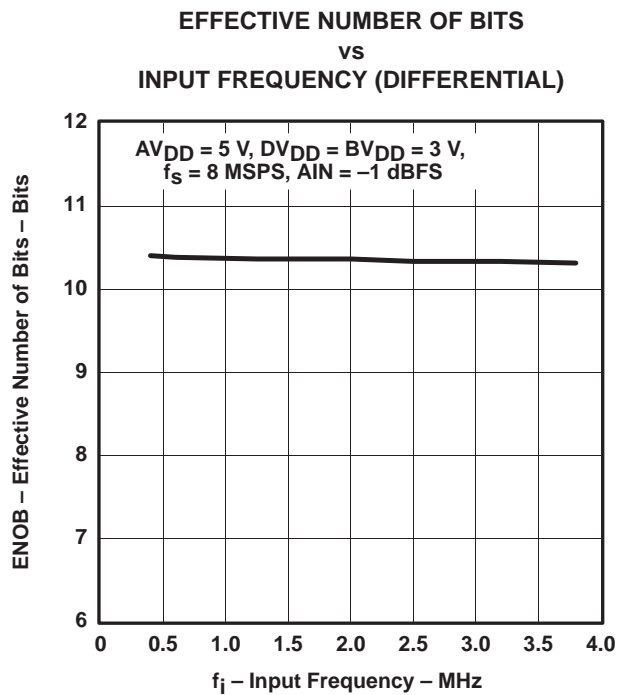
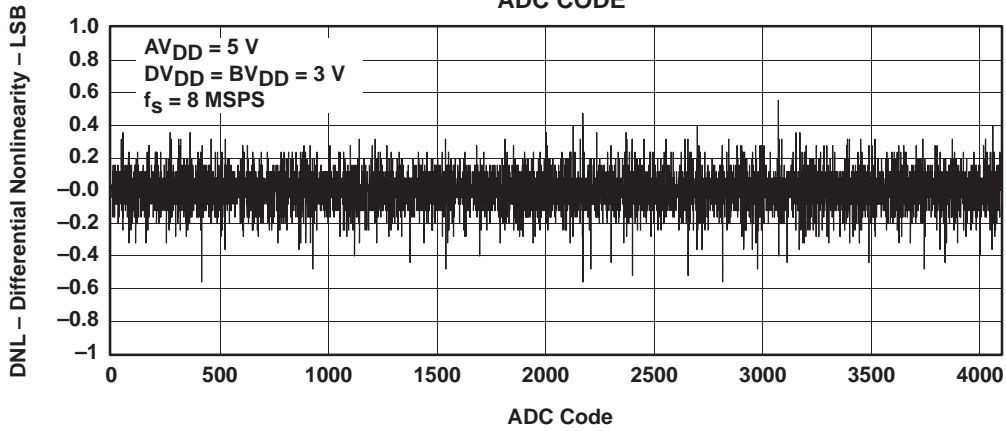


Figure 30

**THS1209**  
**12-BIT, 2 ANALOG INPUT, 8 MSPS, SIMULTANEOUS SAMPLING**  
**ANALOG-TO-DIGITAL CONVERTER**  
SLAS288 – JULY 2000

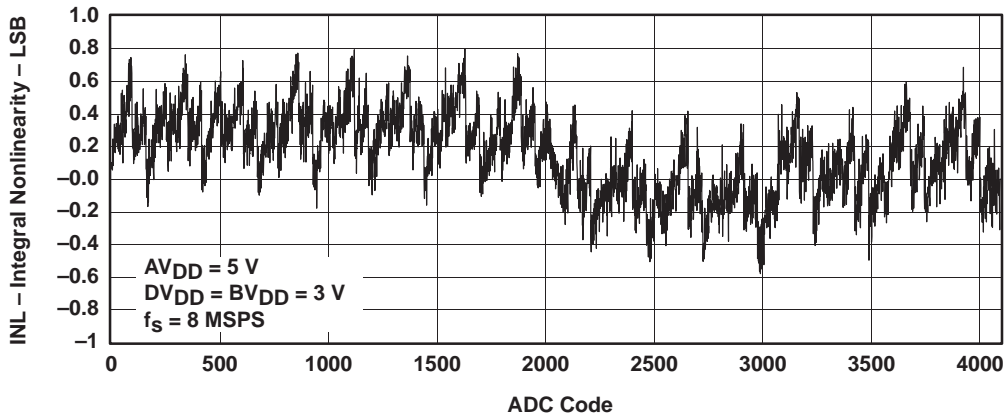
**TYPICAL CHARACTERISTICS**

**DIFFERENTIAL NONLINEARITY**  
**vs**  
**ADC CODE**



**Figure 31**

**INTEGRAL NONLINEARITY**  
**vs**  
**ADC CODE**



**Figure 32**

THS1209  
12-BIT, 2 ANALOG INPUT, 8 MSPS, SIMULTANEOUS SAMPLING  
ANALOG-TO-DIGITAL CONVERTER

SLAS288 – JULY 2000

**TYPICAL CHARACTERISTICS**

FAST FOURIER TRANSFORM (4096 POINTS)  
(SINGLE-ENDED)  
vs  
FREQUENCY

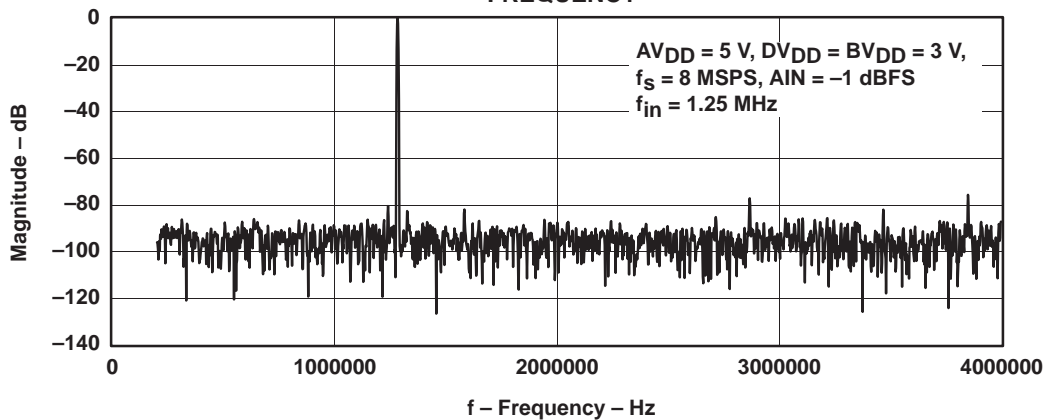


Figure 33

FAST FOURIER TRANSFORM (4096 POINTS)  
(DIFFERENTIAL)  
vs  
FREQUENCY

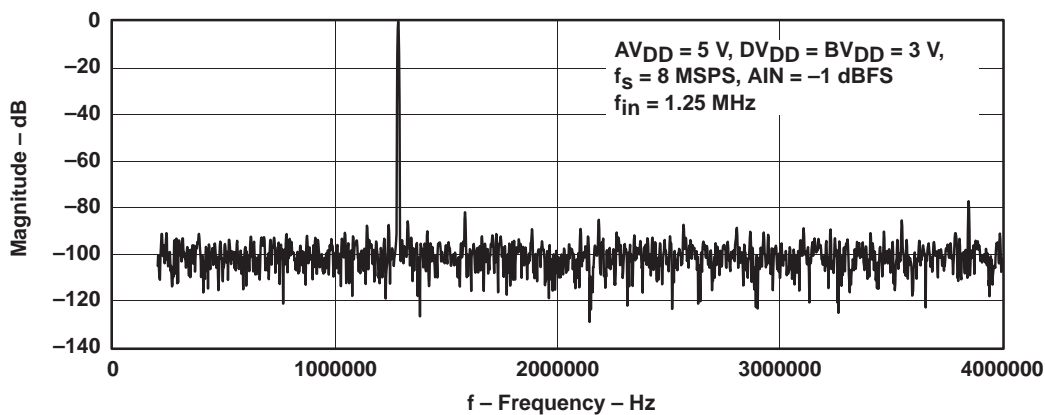


Figure 34

# THS1209

## 12-BIT, 2 ANALOG INPUT, 8 MSPS, SIMULTANEOUS SAMPLING ANALOG-TO-DIGITAL CONVERTER

SLAS288 – JULY 2000

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### definitions of specifications and terminology

#### integral nonlinearity

Integral nonlinearity refers to the deviation of each individual code from a line drawn from zero through full scale. The point used as zero occurs 1/2 LSB before the first code transition. The full-scale point is defined as level 1/2 LSB beyond the last code transition. The deviation is measured from the center of each particular code to the true straight line between these two points.

#### differential nonlinearity

An ideal ADC exhibits code transitions that are exactly 1 LSB apart. DNL is the deviation from this ideal value. A differential nonlinearity error of less than  $\pm 1$  LSB ensures no missing codes.

#### zero offset

The major carry transition should occur when the analog input is at zero volts. Zero error is defined as the deviation of the actual transition from that point.

#### gain error

The first code transition should occur at an analog value 1/2 LSB above negative full scale. The last transition should occur at an analog value 1 1/2 LSB below the nominal full scale. Gain error is the deviation of the actual difference between first and last code transitions and the ideal difference between first and last code transitions.

#### signal-to-noise ratio + distortion (SINAD)

SINAD is the ratio of the rms value of the measured input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for SINAD is expressed in decibels.

#### effective number of bits (ENOB)

For a sine wave, SINAD can be expressed in terms of the number of bits. Using the following formula,

$$N = \frac{(\text{SINAD} - 1.76)}{6.02}$$

it is possible to get a measure of performance expressed as N, the effective number of bits. Thus, effective number of bits for a device for sine wave inputs at a given input frequency can be calculated directly from its measured SINAD.

#### total harmonic distortion (THD)

THD is the ratio of the rms sum of the first six harmonic components to the rms value of the measured input signal and is expressed as a percentage or in decibels.

#### spurious free dynamic range (SFDR)

SFDR is the difference in dB between the rms amplitude of the input signal and the peak spurious signal.

THS1209  
**12-BIT, 2 ANALOG INPUT, 8 MSPS, SIMULTANEOUS SAMPLING  
 ANALOG-TO-DIGITAL CONVERTER**

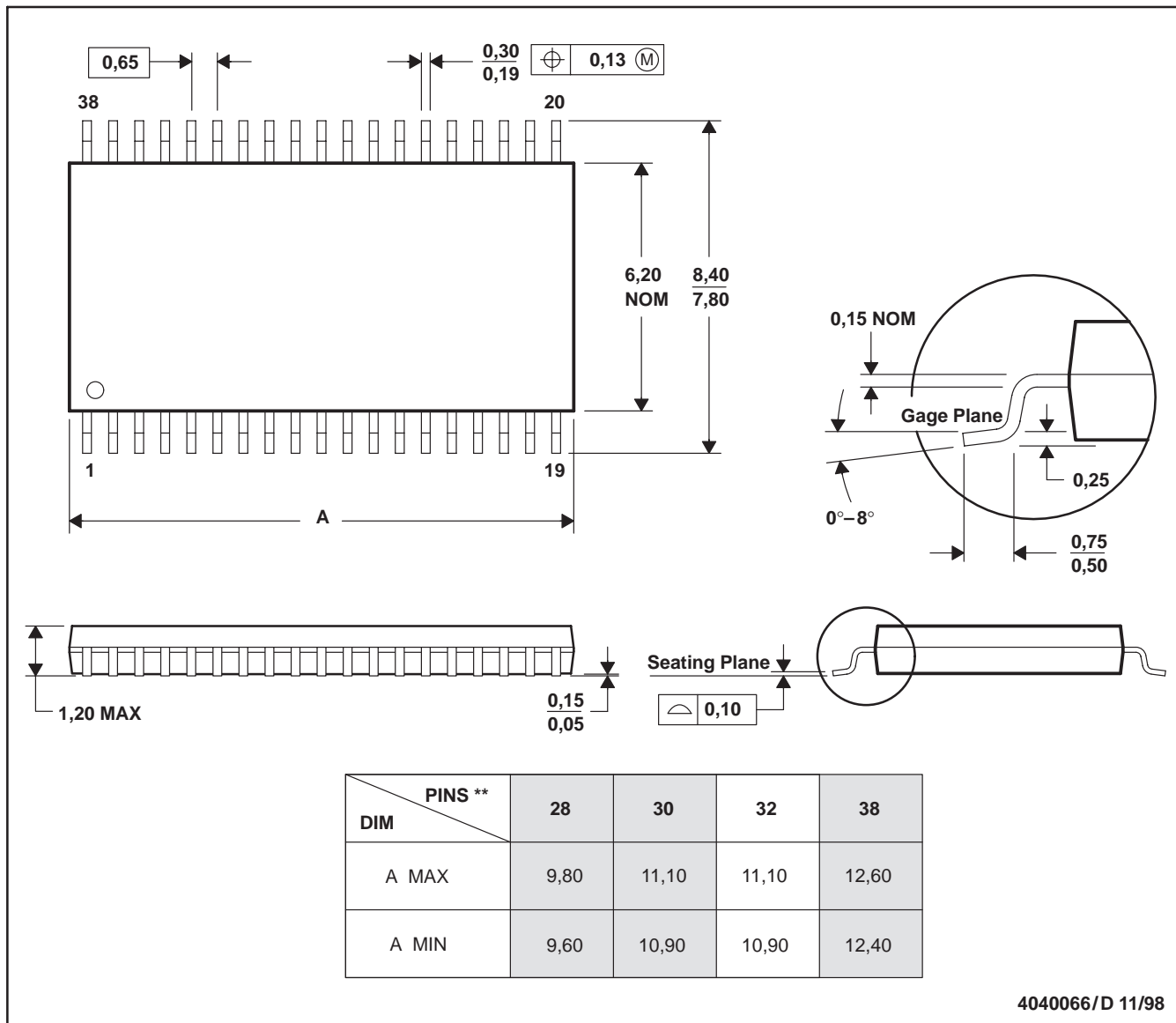
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**MECHANICAL DATA**

**DA (R-PDSO-G\*\*)**

**PLASTIC SMALL-OUTLINE PACKAGE**

**38 PINS SHOWN**



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion.  
 D. Falls within JEDEC MO-153

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TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

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