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TLV2543 Evaluation Module

Technical Reference

1999

Mixed-Signal Products

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TLV2543
Evaluation Module
Technical Reference

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Preface

Read This First

About This Manual

The purpose of this users guide is to serve as a reference manual for the TLV2543 12-bit analog-to-digital converter evaluation module (EVM). This document provides information to assist hardware and software engineers in application development.

How to Use This Manual

This document contains the following chapters and appendixes:
Chapter 1 – Overview
Chapter 2 – Hardware Description and Operation
Chapter 3 – Software Program and Flowcharts
Appendix A – TLC2543 Data Sheet

Notational Conventions

- Program listings, program examples, and interactive displays are shown in a `special typeface` similar to a typewriter. Examples use a **`bold version`** of the special typeface for emphasis; interactive displays use a **`bold version`** of the special typeface to distinguish commands that you enter from items that the system displays (such as prompts, command output, error messages, etc.).

  Here is a sample program listing:

  ```
  0011  0005  0001          .field    1, 2
  0012  0005  0003          .field    3, 4
  0013  0005  0006          .field    6, 3
  0014  0006                .even
  ```

  Here is an example of a system prompt and a command that you might enter:

  ```
  C:  csr –a /user/ti/simuboard/utilities
  ```

- In syntax descriptions, the instruction, command, or directive is in a **bold typeface** font and parameters are in an *italic typeface*. Portions of a syntax that are in **bold** should be entered as shown; portions of a syntax that are in *italics* describe the type of information that should be entered. Here is an example of a directive syntax:

.asect **”***section name***”,** *address*

.asect is the directive. This directive has two parameters, indicated by *section name* and *address*. When you use .asect, the first parameter must be an actual section name, enclosed in double quotes; the second parameter must be an address.

- Square brackets (**[** and **]**) identify an optional parameter. If you use an optional parameter, you specify the information within the brackets; you don’t enter the brackets themselves. Here’s an example of an instruction that has an optional parameter:

  LALK *16–bit constant [, shift]*

  The LALK instruction has two parameters. The first parameter, *16-bit constant*, is required. The second parameter, *shift*, is optional. As this syntax shows, if you use the optional second parameter, you must precede it with a comma.

  Square brackets are also used as part of the pathname specification for VMS pathnames; in this case, the brackets are actually part of the pathname (they are not optional).

- Braces ({ and }) indicate a list. The symbol **|** (read as *or*) separates items within the list. Here’s an example of a list:

  `{ * | *+ | *– }`

  This provides three choices: `*`, `*+`, or `*–`.

  Unless the list is enclosed in square brackets, you must choose one item from the list.

- Some directives can have a varying number of parameters. For example, the .byte directive can have up to 100 parameters. The syntax for this directive is:

  .byte *value*$_1$ *[, ... , value*$_n$*]*

  This syntax shows that .byte must have at least one value parameter, but you have the option of supplying additional value parameters, separated by commas.

Information About Cautions and Warnings

This book may contain cautions and warnings.

CAUTION

This is an example of a caution statement.

A caution statement describes a situation that could potentially damage your software or equipment.

WARNING

This is an example of a warning statement.

A warning statement describes a situation that could potentially cause harm to <u>you</u>.

The information in a caution or a warning is provided for your protection. Please read each caution and warning carefully.

Related Documentation From Texas Instruments

TLV2543 12-Bit Analog-to-digital Converters With Serial Control and 11 Analog Inputs data sheet (literature number SLAS079C) is included in Appendix A of this book. It contains electrical specifications, available temperature options general overview of the device, and application information.

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Chapter 1

Overview

The TLV2543 evaluation module (EVM) provides a platform for evaluating the TLV2543 analog-to-digital converter (ADC). For ease of evaluation, the ADC is interfaced with a microcontroller, three sensors, and a display. The onboard sensors provided are:

- An optical sensor
- A temperature sensor
- A variable resistor

Eight additional analog inputs are available for user-provided signals. Provisions are made for attaching these signal lines to a user-supplied connector. Terminals for an external power supply are also provided. This chapter includes the following topic:

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1.1 Introduction

The TLV2543 evaluation module consists of a TLV2543 12-bit ADC interfaced with a TSL250 optical sensor, a transistor based temperature sensor, a TL1431 voltage reference, a TLV2264 quad op-amp to provide 4 analog signal buffers, a TL7726 hex clamping circuit for signal over-voltage protection, a TMS370C712 microcontroller, three TIL311 hex display characters, and a TPS7233 3.3 volt regulator powering the TLV2543, TLC2264, 74LVC244A and the sensors.

The microcontroller reads the user-programmed dip switches and communicates with the TLV2543 to select the desired analog input, initiate the conversion process, and transfer the converted data back to the microcontroller. The microcontroller then transforms the data into hex form and transfers the result to the three TIL311 displays. A 74LVC244A octal buffer is used as a buffer between the microcontroller and the displays.

A TL7705 power supply voltage monitor resets the processor at power-on or if the power supply voltage drops below the proper operating level.

Jumper provisions are made to connect the TLV2543 reference voltage to 3.3-V power for ratiometric measurements or to an absolute voltage provided by a TL1431 voltage reference device.

A connector pattern is provided for the user to install an interface connector. An uncommitted breadboard area is also provided. An external 5-V power supply (4.75 V to 5.25 V at 0.5 A) is required for operation.

Chapter 2

Hardware Description and Operation

This chapter contains descriptions of the hardware and operation of the TLCV2543EVM. This chapter includes the following topics:

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2.1 Setup and Operation

The power supply terminals (J2) on the TLV2543 EVM module must be connected to a regulated 4.75-V to 5.25-V power supply capable of providing at least 0.5 A.

CAUTION

This evaluation module is designed to have power supplied from an external regulated 5-V power supply. No form of power supply regulation is included on the module. Damage to the components can and will occur if the voltage exceeds the maximum specified level. Under voltage can cause improper operation.

When the power supply is switched on, the microcontroller is initialized and the displays flash to indicate proper operation. The displays then show a two or three digit hex value of the voltage generated by the optical sensor and digitized by the TLV2543. The value on the displays varies with the intensity of the light striking the TSL250 sensor (See the *Optical Sensor* section).

The input select switch (S1) is set to the hex address (LSB on the right) which selects the desired TLV2543 input (See the *Input Select Switch* section). The desired A/D converter reference voltage for a given sensor is selected by moving the Ref Select jumper (JP9) to the onboard reference (REF V) position or the power supply (V_{CC}) position.

The TLV2543 EVM module is shipped with the settings listed in the following table:

Table 2–1. EVM Default Settings

Function	Setting
Input select switch (S1)	0000 hex (optical sensor selected)
Reference select jumper (JP9)	REF V
Input jumpers (JP1, JP2, JP3, JP11, JP12)	Ground
Output jumpers (JP4, JP5, JP6, JP7, JP8)	Shorted
Ref– jumper (JP10)	Shorted

NOTE: The input and output jumpers and the REF– jumper on the TLV2543 EVM are formed by a top side copper trace on the PC board between two plated through holes. If desired, the trace can be carefully cut to remove the jumper. The two through holes allow the user to restore the jumper with a wire or connector.

A hole pattern is provided for a user-supplied connector to allow easy application of external analog signals for additional evaluation (See the *Interface Connector Provisions* section).

The following sections give more specific information about each selected sensor input and selected reference.

2.2 Input Select Switch

The four position dip switch (S1) labeled input select allows the user to select the desired analog input of the TLV2543. The switch is treated as a hex address command (MSB on left, LSB on right) as listed in the following table:

Table 2–2. Input Select Switch Descriptions

Hex	Binary	Function Selected	Typical Response
0h	0000	Optical sensor input	User controlled light intensity
1h	0001	Temperature sensor input	588h + temperature change
2h	0010	Potentiometer input	User adjusted
3h	0011	IN3 buffer input	000h or user input
4h	0100	IN4 buffer input	000h or user input
5h	0101	IN5 buffer input	000h or user input
6h–Ah	0110–1010	IN6 through IN10 inputs	000h or user input
Bh	1011	(V_{ref} input)/2 test	800h
Ch	1100	–V_{ref} input (ground) test	000h
Dh	1101	V_{ref} input test	FFFh
Eh	1110	Enter power down mode	Display blank
Fh	1111	Fast conversion rate on IN4 input	User input

Note: Inputs IN3 through IN10 are made available to a user supplied connector (see the *Interface Connector Provisions* section).

2.3 Microcontroller

The TMS370C712 microcontroller (U4) samples the status of the input select switch on ports A4 through A7. This sample data, which is sent to the TLV2543 through the serial peripheral interface ports SPICLK, SPISIM0, and SPISOM1, determines which specific multiplexer input is converted. The microcontroller then reads back the converted 12 bits and changes the data into three hexidecimal digit values. The hexidecimal data is transferred to the three hexidecimal displays U7, U8, and U9. Five sections of the 74LVC244A octal buffer are used to drive the common bused TTL inputs of the displays.

For all input select positions except Fh, the microcontroller instructs the TLV2543 to perform the analog-to-digital conversions and display the results at a rate of approximately 2 conversions per second. When the Input Select position is Fh, the microcontroller selects input IN4 and the conversions from the TLV2543 are at a rate of approximately 30k conversions per second (See the *Fast Conversion Rate* section).

NOTE: The following information applies to the TMS370C712 serial peripheral interface (SPI) to the TLV2543.

The TLV2543 strobes in the command data bits from the microcontroller on the DIN port at the rising edge of the clock pulse on the I/O CLK terminal. The TMS370C712 generates a clock rising edge on the SPICLK port and also at that time, while conforming to the SPI interface requirements, the data output on the SPISIM0 port changes to reflect the next serial bit to be transferred.

If the SPICLK output is connected directly to the TLV2543 I/O CLK input, the required data setup time for the data to be present before a rising clock edge is applied cannot be less than 100 ns (see the *TLV2543* data sheet). To solve this race condition, a resistor (R24) and capacitor (C21) provide a delay to the rising clock edge. One buffer section of the 74LVC244A octal buffer (U6) is used to buffer the delayed clock signal. If only one TLV2543 is being used (as with this EVM), the buffer is not normally required. If several TLV2543 devices are being driven in a bus configuration, using this buffer is advised.

2.4 Power Supply Supervisor

Power supply voltage is monitored by the TL7705 (U5). When power is first applied, a microprocessor reset is held until the power supply voltage exceeds 4.55 V (nominal). The reset is then released and the microprocessor begins operation.

During normal operation, if the power supply voltage falls below 4.55 V, a reset is activated again.

2.5 Optical Sensor

The TSL250 (U1) optical sensor is connected to the AIN0 multiplexer analog input port of the TLV2543. This sensor converts light intensity to an output voltage ranging from less than 10 mV (dark) to about 2 V (at 2 mW/sq cm illumination intensity).

The output of the optical sensor can be varied by placing an object such as a dark colored plastic marker pen cap over the sensor.

A practical application such as sorting can be demonstrated by holding similar objects of differing shades within the optical viewing range of the sensor (under a uniform intensity light) and noting the displayed values. A simple optical hood to mask ambient light (e.g. drill a hole in the side of the marker pen cap) provides more uniform results.

NOTE: Office light generated by typical artificial lighting contains a high component of ac line frequency intensity variations not normally perceived by the human eye. These variations are detected by the optical sensor. Since the ADC is commanded to make measurements at random times with respect to the ac line frequency, the converted values appear to be unstable in the lower order bits, even though each individual measurement is accurate. This line frequency light intensity variation can be minimized by using dc power to drive the dominate light source (light emitting diodes work well) in addition to shielding the sensor from the ac driven room lighting.

An extension of the sorting concept can yield a simple color sorting sensor system. This system requires three optical sensors, each masked by a red, blue, or green optical filter. The individual readings from the three sensors can then be calibrated to the specific color of the object to be identified. For repeatable results, the intensity and color content of the illuminating light source must be uniform.

2.6 Temperature Sensor

When a single transistor and the 12-bit A/D conversion range of the TLV2543 are used, the following characteristics can be seen:

- A simple temperature sensor
- The textbook temperature variation of a transistor base-emitter junction
- The dc temperature instability of a simple one-transistor amplifier

The 2N2222A transistor (Q1) is connected in a classical feedback amplifier configuration that forces the collector voltage to a base-emitter junction voltage of 2 V_{be}. The base-emitter junction (essentially a forward biased diode) voltage is about 0.7 V at room temperature (25C°) and has a temperature variation of about –2.2 mV/C°. Therefore at room temperature, the collector voltage is approximately 1.4 V with a decrease of approximately 4.4 mV for each degree of temperature increase.

If the REF select jumper is set to the on-board reference (REF V) position, the conversion reference is set to approximately 2500 mV or 2.5 V. This setting allows the display to decrement approximately 1.6 counts for each mV or about 7 counts per C° of temperature increase.

If the ambient room temperature is approximately 25C° and human body temperature is approximately 38C°, the display should reduce about 91 counts when the transistor is held firmly between two fingers. For a more exact analysis, exact transistor characteristics, absolute reference voltage levels, exact room and finger temperatures, etc. would have to be taken into account.

2.7 Voltage Variable Input (Potentiometer)

The IN2 input is controlled by a potentiometer (R13). One section of the TLC2264 (U2) serves as a buffer amplifier for the AIN2 TLV2543 input port. When the potentiometer is adjusted over its range, the input voltage changes from 0 to $V_{CC}/2$ (approximately 3.3 V/2 = 1.65 V). Since the buffer amplifier has a gain of 2, the input to the TLV2543 port varies from 0 to V_{CC}.

For ratiometric measurements, the REF select jumper should be set to the V_{CC} position. Then the TLV2543 reference becomes V_{CC} and all A/D conversions are made relative to the value of V_{CC}. The potentiometer output voltage, by its connection, is also relative to V_{CC}. An A/D conversion of that voltage yields a value proportional to the setting of the potentiometer and independent of the power supply voltage.

2.8 Buffered User Inputs

The IN3 input is connected to the TLV2543 input port through unity gain configured buffer amplifiers (one section of the TLC2264, U2). Although providing unity gain (gain = +1), the input signal can only be within approximately 1.5 V (see the common mode input voltage range specifications of the TLC2264) of the power supply voltage to maintain predictable operation. As long as the power supply voltage to the TLC2264 remains at 3.3 V, this restricts the usable signal input voltage range from 0 V to 1.8 V, however this range can be acceptable for some input level requirements.

The input impedance is dictated by the 10 kΩ value of resistor R14 and can be changed to almost any suitable value due to the extremely high input impedance of the TLC2264.

Inputs IN4 and IN5 are connected to the TLV2543 input ports, each through a buffer stage of the TLC2264, and each with a gain of 2. The full output voltage swing of 0 V to 3.5 V to the ADC inputs is achieved with signal inputs of 0 V to 1.65 V as listed in Table 2–3.

Table 2–3. Buffered User Input Descriptions

Input	Gain	Unbuffered	Input Range
IN3	×1	N	0 V – 1.8 V (input to ADC is 1.8/3.3 of full scale)
IN4	×2	N	0 V – 1.65 V
IN5	×2	N	0 V – 1.65 V
IN6		Y	0 V – 3.3 V
IN7		Y	0 V – 3.3 V
IN8		Y	0 V – 3.3 V
IN9		Y	0 V – 3.3 V
IN10		Y	0 V – 3.3 V

2.9 Unbuffered Inputs

The IN6 through IN10 inputs are connected to ground by the top side circuit board etch jumpers JP1, JP2, JP3, JP12, and JP11, respectively. Any etch jumper can be removed by carefully cutting the copper trace between the feed-through holes at the JP marking, allowing that input to be connected to an external signal.

When these unbuffered inputs are used, the required TLV2543 specifications such as a low source impedance (see the *Driving the Input of a Switched Cpacitor ADC* section) and input voltage range (0 V to 3.3 V) must be used. The signal grounds should not be improperly connected to the high current power supply grounds (see the *Grounding Considerations* section).

2.10 Reference Select

The REF select jumper is provided to allow ratiometric measurements (jumper set to V_{CC}) or allow absolute measurements (jumper set to REF V) relative to a voltage reference established by the TL1431 (D1). This voltage reference is approximately 2.5 V.

Ratiometric measurements are made relative to the 3.3-V power supply voltage. If a sensor or input signal voltage is used that varies proportional to the 3.3-V power supply voltage (such as the potentiometer R13), then the signal becomes a ratio of the absolute value of the power supply voltage. Then, if the reference voltage is connected to 3.3 V (REF SELECT jumper position at V_{CC}), the TLV2543 tracks the power supply voltage and provides a converted result independent of the power supply voltage variations.

Absolute measurements are required if the sensor or input analog signal does not change with the power supply voltage. The previously described optical and temperature sensors are in this category. For these sensors, the REF select jumper is set to the REF V position.

2.11 Fast Conversion Rate

When the input select switch is set to Fh, the EVM module operates in a fast conversion rate mode. In this mode, the conversion rate is approximately 30k conversions per second from the IN4 input. The displays are updated once every 20 conversions.

2.12 Input Voltage Clamp

The TL7726 (VZ1) is connected to inputs IN3 through IN8. The TL7726 clamps an input signal voltage in excess of the power supply voltage level to prevent damage to the semiconductor inputs. Signal voltages below 0 V (ground) are clamped to ground. Signal inputs between 3.3 V and ground are not affected. The TL7726 provides protection for inputs from incidental transients due to static discharge, excessive signals, etc. Transient current protection is limited to 25 mA.

2.13 Interface Connector Provisions

A hole pattern for a user-supplied interface connector is provided at J1. A standard 8 × 2 set of header posts (such as an AMP 87215-5 or Molex 10-89-1161) can be soldered in place. This arrangement allows several different styles of connector to be installed as necessary to satisfy user requirements.

Figure 2–1. Interface Connector Hole Pattern

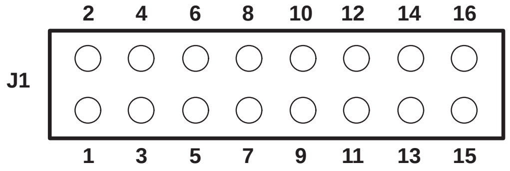


Table 2–4. Interface Connector Hole Pattern Descriptions

Hole	Circuit Function
1	NC
2	NC
3	IN3 input (buffered with +1X gain)
4	IN4 input (buffered with +2X gain)
5	IN5 input (buffered with +2X gain)
6	IN6 input
7	IN7 input
8	IN8 input
9	IN9 input
10	IN10 input
11	5 V
12	Signal ground
13	5 V
14	Power ground
15	5 V
16	Power ground

Note: Hole 12 can be used as a signal ground return to avoid the higher current ground return paths that are associated with a power supply ground.

2.14 Grounding Considerations

When designing analog circuits that share a ground with digital and high current power supplies, the voltage drop along the high current paths must be taken into account. This voltage drop is a result of the current flowing through the greater-than-zero resistance of the current path, and/or high frequency current transients flowing through the greater-than-zero inductance of a current path.

If the signal ground is connected to the power supply ground at the improper location, this voltage drop is injected into the signal ground and appears as part of the signal, causing an error.

The solution is to establish a single ground point on the PC board and connect all grounds individually to that point (the EVM single ground point is at the GND terminal of the power supply connector). By using this method, currents flowing along any one path to ground do not inject error voltages in any other ground path.

As a practical implementation, however, it may not be reasonable to run a separate ground trace for each component that connects to ground. Therefore, the next best approach is to group the higher current grounds (such as the power supply and digital grounds) together and run them to the central PC board ground point, while still maintaining separate ground paths for the analog grounds.

An analysis of current flow paths within the analog section will give an indication of which grounded components could be lumped together into a common ground path and which should be kept separate. For instance, on the EVM, it would be reasonable to use a common path for the TLV2543 REF– terminal and the TL1431 anode. This is because the only significant current flow is through the TL1431 (only about 1 mA) and is not enough to cause a significant error. A 1/2 LSB error at a reference voltage of 2.5 V would be about 0.3 mV, so the ground trace would have to be in excess of 0.3 Ω to cause such an error.

If all of the input signals are low current, such as the optical sensor (about 2 mA), the temperature sensor (about 1 mA) and the potentiometer (about 0.25 mA), it may be reasonable to use a common ground trace. As always, wider trace widths are desirable to keep the resistance low. If high currents are associated with any input signal, always use a separate PC board trace directly to the central ground point location.

Even though the operating current of the TLV2543 is low (2.5 mA max), some high speed current transients due to the internal digital switching are present and a separate ground trace is reasonable.

Note:

Always keep the power supply decoupling capacitor as close as possible to the supply pins. This means that the separate ground trace would actually be for the decoupling capacitor and the TLV2543 ground pin.

If free area is available, or if the PC board is multilayer, a large ground plane may be acceptable to connect all the analog side ground connections providing that any one signal ground connection is not carrying a large current. That ground plane should be connected directly to the central ground point without touching any of the digital or power supply ground locations along its path.

Treating the distribution of the digital and analog 5-V and 3.3 V current paths on the PC board in a similar manner to the grounds is also a good practice. The designated central power point location is the 5-V terminal of the power supply connector (J2) on the EVM board.

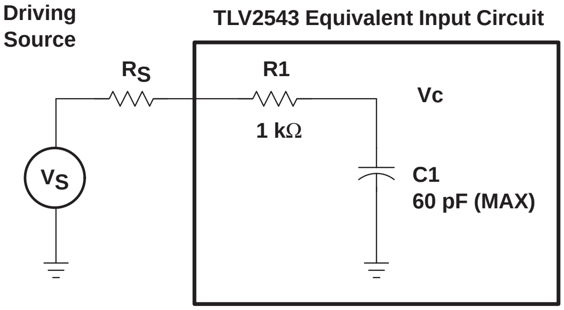
2.15 Driving the Input of a Switched Capacitor ADC

When applying an analog signal to the input of a switched capacitor ADC such as the TLV2543, care must be taken to provide a low enough impedance to the input terminal to charge the internal capacitor enough for an accurate conversion during the sampling phase of the converter. The sampling time will depend on the period of the I/O clock rate being used to drive the converter and the number of transfer bits commanded. With the maximum I/O clock frequency of 4.1 MHz and a 12-bit transfer mode, the TLV2543 uses 8 clock cycles (or about 2 µs) for the sampling time.

The input equivalent circuit of the TLV2543 looks like a series resistance and a capacitor to ground during sampling and an open circuit during conversion.

For accurate operation the input capacitor must be charged to the required accuracy of 1/2 LSB (or more, depending on the required system error budget) during the sampling phase of the ADC cycle.

Figure 2–2. Equivalent Input Circuit



The voltage on capacitor C1 is given by:

$$Vc = Vs\left(1 - e^{-t/TC}\right) \tag{1}$$

Where TC is the time constant C1(Rs+R1)

The final voltage value of Vc within 1/2 LSB of Vs is

$$Vc\ (1/2\ \mathrm{LSB}) = Vs - Vs/2^{n+1} \tag{2}$$

Where n is the resolution of the converter.

So equating equation 1 to equation 2 then

$$Vs - Vs/2^{n+1} = Vs\left(1 - e^{-t/TC}\right)$$

therefore the charging time in terms of the circuit time constants is

$$t\ (1/2\ \mathrm{LSB}) = TC\ln\left(2^{n+1}\right)$$

For a 12-bit converter this would be:

$$t_S = TC \times \ln(8192) = 9\ TC$$

The internal capacitance for the TLV2543 is 60 pF max and the internal series resistance is 1 KΩ. Therefore, with an I/O clock at 4.1 MHz, and a 12-bit transfer mode (sample period = 2 µs), the time constant should be no more than:

1/9 x 2 µs = 0.22 µs

Therefore

C1(Rs+R1) = 0.22 µs

So

(Rs+R1) = 3.67 KΩ

Since Rs = 1K, then the source impedance should be less than 2.67 KΩ to stay within 1/2 LSB error. Good design practice dictates that the source impedance be as low as possible, such as the output of an op-amp. However in an application where fast conversion time is not critical, slow I/O clock rates can allow the driving source impedance to be relatively large.

2.16 Board Schematic

The schematic of the EVM is shown in the following figure.

Figure 2–3. Board Schematic

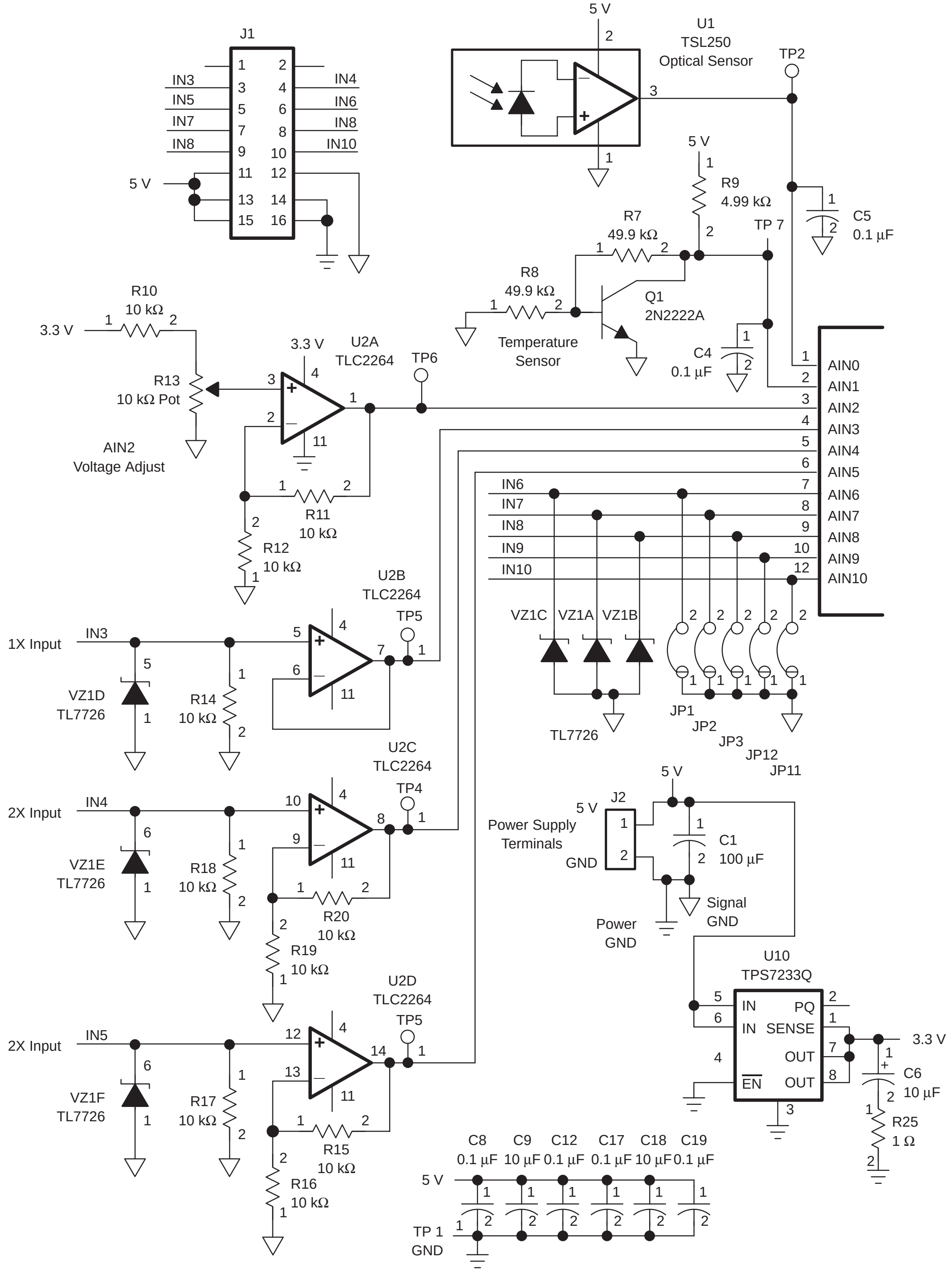
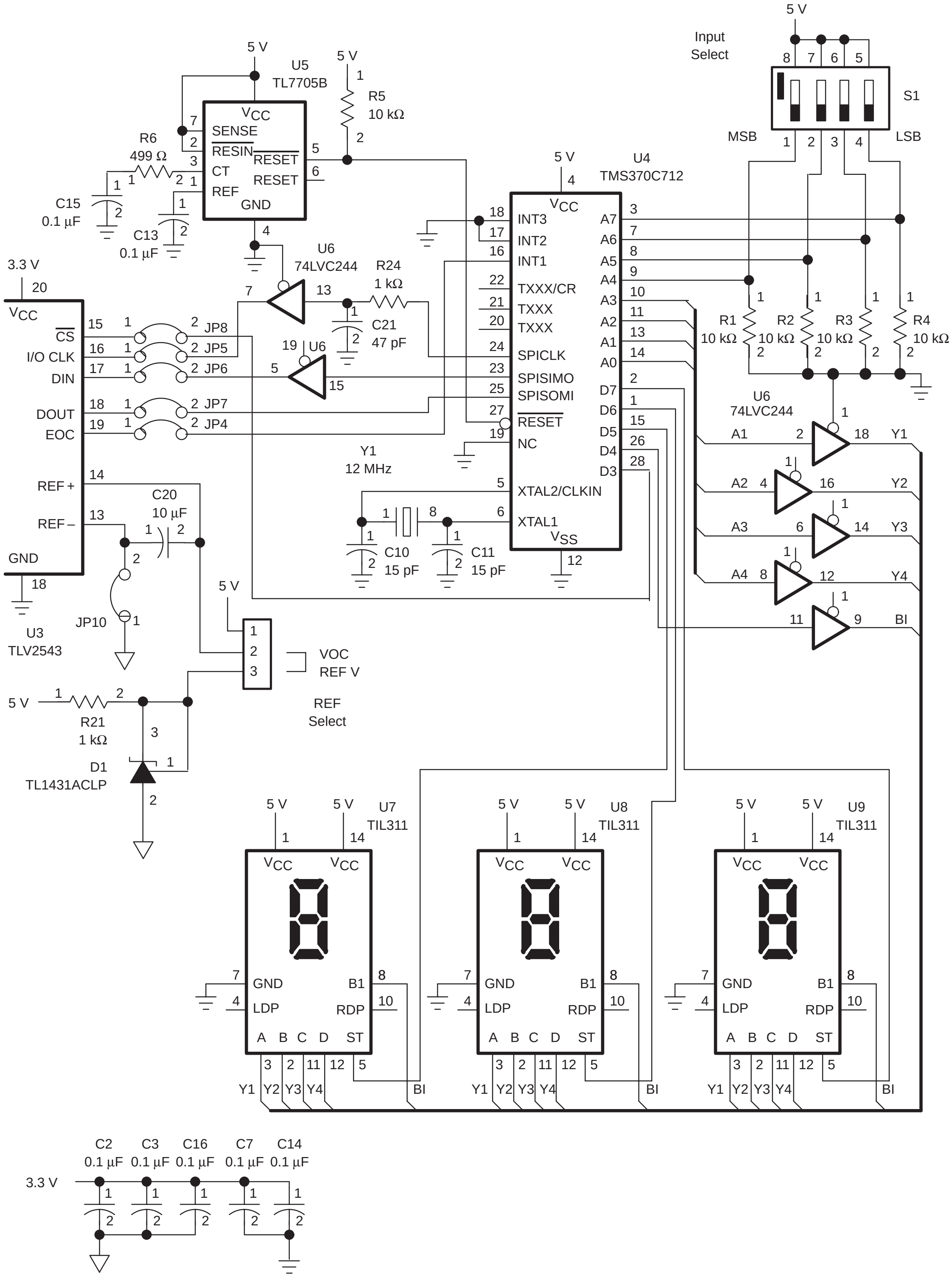


Figure 2–3 Board Schematic (continued)



2.17 Part Descriptions

A list of the TLV2543 EVM parts are listed in the following table.

Table 2–5. Part Descriptions

Number	Quantity	Reference	Description
1	1	C1	100 µF, 16V Aluminum
2	14	C2, C3, C4, C5, C7, C8, C12, C13, C14, C15, C16, C17, C18, C19	0.1 µF Ceramic, Z5U, 0.2 Inch
3	2	C20	10 µF, 6.3 V Tantalum, 0.2 Inch
4	2	C9, C6	10 µF, 10 V Alum
5	2	C10, C11	15 pF Ceramic, NPO, 0.2 Inch
6	1	C21	47 pF
7	1	D1	TL1431ACLP
8	1	JP9	3 Pin Header
9	1	JP9	Shorting jumper, 2 Pin
10	1	J2	Terminal block, 2 Pos, 5 mm, side entry (OST ED1601)
11	1	Q1	2N2222A (T0-18 metal can)
12	16	R1, R2, R3, R4, R5, R10, R11, R12, R14, R15, R16, R17, R18, R19, R20	10K Ω, 1%, 0.25 W
13	1	R6	499 ΩO
14	2	R7, R8	49.9K Ω
15	1	R9	4.99K Ω
16	1	R21, R24	1K Ω
17	1	R25	1 Ω
18	1	R13	10K Ω Pot, single turn, top adj, 3/8 inch sq (Bourns 3386 P)
19	1	S1	DIP switch, 4 pos, Gold
20	1	U1	TSL250
21	1	U2	TLC2264
22	1	U3	TLV2543 (3V)
23	1	U4	TMS370C712
24	1	U5	TL7705B
25	1	U6	74LVC244A
26	3	U7, U8, U9	TIL311
27	1	U10	TPS7233Q (SOJC)
28	1	VZ1	TL7726
29	1	Y1	12 MHz crystal, HC-49/µs
30	1		PC board, TLV2543 EVM

R22, R23, C4, C5 designations unused

Chapter 3

Software Program and Flowcharts

The TLV2543 EVM uses a TI TMS370C712 microcontroller to interface with the TLV2543 ADC. The program reads a four position DIP switch to determine which input is selected to be digitized. The program then uses the onboard SPI interface to communicate with the TLV2543. Sixteen bits of data (12 significant bits and 4 fill bits) are read into the processor and output on the three LED displays. This is repeated approximately every 0.5 seconds.

A fast mode can also be selected with the DIP switch. In this mode, channel four is selected as input and 20 samples are taken at about a 30 kHz rate, data is converted and displayed, and the process is repeated until another input is selected with the DIP switch. A power-down mode can also be selected which places the TLV2543 in a power-down mode and blanks the display.

This chapter includes the following topics.

Topic **Page**

3.1 Software Program 3-2
3.2 Flowcharts 3-8

3.1 Software Program

```
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adc_evm.asm                                                          PAGE    1

                   ;;;;;;;;;;;;;;;;;;;;;;;;
                   ;
                   ; TLV2543 EVALUATION MODULE PROGRAM
                   ;
                   ;       VERSION 1.2   8/17/95
                   ;
                   ;       THIS PROGRAM READS A FOUR POSITION DIP
                   ;       SWITCH WHICH IS USED TO SELECT THE INPUT
                   ;       SIGNAL CHANNEL TO THE ADC.  THE PROGRAM
                   ;       THEN SELECTS THIS CHANNEL ON THE ADC AND
                   ;       CONVERTS THE ANALOG INPUT TO A 12 BIT
                   ;       HEX NUMBER AND OUTPUTS THE RESULTS ON
                   ;       3 7–SEGMENT DISPLAYS. POSITIONS ARE ALSO
                   ;       PROVIDED TO PUT THE ADC IN A POWER DOWN
                   ;     MODE AND A FAST MODE (APPROX 26 KHZ RATE).
                   ;
                   ;;;;;;;;;;;;;;;;;;;;;;;;
                   ;;;;;;;;;;;;;;;;;;;;;;;;
                   ;
                   ; SYSTEM EQUATES
                   ;
                   ;;;;;;;;;;;;;;;;;;;;;;;;
                   ;
                   ; SERIAL PERIPHERAL INTERFACE (SPI) REGISTERS
                   ;
           0030    SPICCR  .EQU    P030    ;SPI CONFIG REG
           0031    SPICTL  .EQU    P031    ;SPI OPERATION CONTROL REG
           0037    SPIBUF  .EQU    P037    ;SPI INPUT BUFFER
           0039    SPIDAT  .EQU    P039    ;SPI SERIAL DATA REG
           003d    SPIPC1  .EQU    P03D    ;SPI PORT CONTROL REG1
           003e    SPIPC2  .EQU    P03E    ;SPI PORT CONTROL REG2
           003f    SPIPRI  .EQU    P03F    ;SPI INTERRUPT CONTROL REG
                   ;
                   ; PORT A AND D REGISTERS
                   ;
           0021    APORT2  .EQU    P021    ;PORT A CONTROL REG
           0022    ADATA   .EQU    P022    ;PORT A DATA
           0023    ADIR    .EQU    P023    ;PORT A DIRECTION
           002c    DPORT1  .EQU    P02C    ;PORT D CONTROL REG1
           002d    DPORT2  .EQU    P02D    ;PORT D CONTROL REG 2
           002e    DDATA   .EQU    P02E    ;PORT D DATA
           002f    DDIR    .EQU    P02F    ;PORT D DIRECTION
                   ;
                   ; TIMER 1 DEFINITIONS
                   ;
           0040    T1CNTR1 .EQU    P040    ;MSB OF COUNTER
           0041    T1CNTR2 .EQU    P041    ;LSB OF COUNTER
           0042    TC11    .EQU    P042    ;MSB OF COMPARE REGISTER
           0043    TC12    .EQU    P043    ;LSB OF COMPARE REGISTER
           0049    T1CTL1  .EQU    P049    ;TIMER 1 CONTROL REG 1
           004a    T1CTL2  .EQU    P04A    ;TIMER 1 CONTROL REG 2
           004b    T1CTL3  .EQU    P04B    ;TIMER 1 CONTROL REG 3
                   ;
                   ; BIT DEFINITIONS
                   ;
```

```
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adc_evm.asm                                                          PAGE    2

 56        2e        CSBIT   .DBIT   3,DDATA   ;ADC CHIP SELECT BIT
 57        31        SPIF    .DBIT   6,SPICTL  ;SPI INTR FLAF
 58        2e        DOUT1   .DBIT   5,DDATA   ;STROBE FOR DISPLAY 1
 59        2e        DOUT2   .DBIT   6,DDATA   ;STROBE FOR DISPLAY 2
 60        2e        DOUT3   .DBIT   7,DDATA   ;STROBE FOR DISPLAY 3
 61        2e        DBLANK  .DBIT   4,DDATA   ;BLANK STROBE
 62        4a        RST     .DBIT   0,T1CTL2  ;SW TIMER RESET
 63        4b        TOUT    .DBIT   5,T1CTL3  ;TIMER 1 TIME OUT
 64                  ;
 65                  ;;;;;;;;;;;;;;;;;;;;;;;;
 66                  ;
 67 6000                     .TEXT   6000H   ;START OF PROGRAM
 68                  ;
 69                  ;;;;;;;;;;;;;;;;;;;;;;;;
 70                  ;
 71                  ; MAIN PROGRAM
 72                  ;
 73 6000   5260      START   MOV     #60H,B
 74 6002   fd                LDSP            ;SET STACK POINTER TO 60H
 75 6003  ’8e6014            CALL    INIT    ;INITIALIZE SYSTEM
 76                  ;
 77 6006  ’8e6056    LOOP    CALL    READSW  ;READ INPUT DIP SWITCH
 78 6009  ’8e60ed            CALL    ADC     ;DIGITIZE INPUT
 79 600c  ’8e614d            CALL    DISPLAY ;DISPLAY VALUE
 80 600f  ’8e6126            CALL    DELAY   ;DELAY .5 SEC
 81 6012  ’00f2              JMP     LOOP
 82                  ;
 83                  ;;;;;;;;;;;;;;;;;;;;;;;;
 84                  ;;;;;;;;;;;;;;;;;;;;;;;;
 85                  ;
 86                  ; INIT
 87                  ;
 88                  ;       THIS ROUTINE INITIALIZES PORTS A AND
 89                  ;       D, SETS UP THE SPI, AND INITIALIZES
 90                  ;       THE DISPLAYS BY FLASHING 8 AND 0 THREE
 91                  ;       TIMES.
 92                  ;
 93 6014   f70021    INIT    MOV     #0,APORT2  ;SET PORT A TO I/O
 94 6017   f70f23            MOV     #0FH,ADIR  ;SET A4–A7=INPUT, A0–A3=OUTPUT
 95 601a   f7002c            MOV     #0,DPORT1  ;SET PORT D TO I/O
 96 601d   f7002d            MOV     #0,DPORT2
 97 6020   f7f82f            MOV     #0F8H,DDIR ;SET D3–D7 OUTPUTS
 98                  ;
 99 6023   f78030            MOV  #80H,SPICCR ;INIT SPI
100 6026   f70730            MOV  #07H,SPICCR ;SET CLOCK, 8BIT CHAR LEN
101 6029   f7033d            MOV  #03H,SPIPC1 ;SET SPI CLK TO OUTPUT
102 602c   f7223e            MOV  #22H,SPIPC2 ;SET SPISOMI AND SPISIMO TO SPI DATA
103                  ;
104 602f   720019            MOV  #0,R25      ;CLR CHANNEL REGS
105 6032   72001d            MOV  #0,R29
106                  ;
107                  ;       FLASH DISPLAY
108                  ;
109 6035   720314            MOV  #03,R20 ;SET LOOP CTR TO 3 CYCLES
110 6038   2208              MOV  #08H,A  ;SET DISPLAY REGS TO 8
```

```
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adc_evm.asm                                                          PAGE    3

603a   d01a              MOV     A,R26
603c   d01b              MOV     A,R27
603e   d01c              MOV     A,R28
6040  ’8e614d    LOOP1   CALL    DISPLAY
6043   720218            MOV     #02H,R24 ;SET DELAY TO .5 SEC
6046  ’8e6126            CALL    DELAY
6049   a4102e            SBIT1   DBLANK   ;BLANK DISPLAY
604c  ’8e6126            CALL    DELAY
604f   a3ef2e            SBIT0   DBLANK   ;TURN OFF BLANK
6052  ’da14eb            DJNZ    R20,LOOP1  ;JMP BACK IF NOT DONE
6055   f9        RTS
                 ;
                 ;;;;;;;;;;;;;;;;;;;;;;;;
                 ;;;;;;;;;;;;;;;;;;;;;;;;
                 ;
                 READSW
                 ;
                 ;       THIS ROUTINE READS THE 4 POSITION DIP
                 ;       SWITCH FOR THE CHANNEL NUMBER AND SAVES
                 ;       IT IN R29.  IF 0EH IS SELECTED THE ADC
                 ;       IS PLACED IN A POWER DOWN MODE. IF 0FH
                 ;       IS SELECTED THE INPUT ON CHANNEL 4 IS
                 ;       CONVERTED IN FAST MODE. ADC CHANNEL NUMBER
                 ;       IS STORED IN R25.
                 ;
                 ;
6056   8022      READSW  MOV     ADATA,A ;READ SWITCHES
6058   b7                SWAP    A       ;SWAP NIBBLES
6059   230f              AND     #0FH,A
605b   1d1d              CMP     R29,A
605d  ’0601              JNE     READ1   ;JMP IF ADC INPUT CHANGED
605f   f9                RTS
                 ;
                 ; ADC INPUT CHANGED – WAIT FOR COMPLETE
                 ;
6060   d01d      READ1   MOV     A,R29   ;SAVE IT
6062   720318            MOV     #03,R24 ;SET DELAY FLAG TO 2 SEC
6065  ’8e6126            CALL    DELAY
6068   8022              MOV     ADATA,A ;CHECK AGAIN
606a   b7                SWAP    A
606b   230f              AND     #0FH,A
606d   1d1d              CMP     R29,A
606f  ’06ef              JNE     READ1
                 ;
                 ;SEE IF POWER DOWM MODE
                 ;
6071   7d0e1d            CMP     #0EH,R29
6074  ’061b              JNE     READ2   ;JMP IF NOT POWER DOWN
6076   a4102e            SBIT1   DBLANK  ;BLANK DISPLAY
6079   a3f72e            SBIT0   CSBIT   ;ENABLE ADC
607c   f70631            MOV     #06H,SPICTL
607f   f7ec39            MOV     #0ECH,SPIDAT
6082   8022      READ3   MOV     ADATA,A ;WAIT FOR CHANGE
6084   b7                SWAP    A
6085   230f              AND     #0FH,A
```

```
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adc_evm.asm                                                          PAGE    4

166 6087 * 4d001d            CMP     A,R29
167 608a  '02f6              JEQ     READ3
168 608c   a3ef2e            SBIT0   DBLANK  ;CLEAR BLANK
169 608f  '00cf              JMP     READ1
170                  ;
171                  ; SEE IF FAST MODE
172                  ;
173 6091   7d0f1d    READ2   CMP     #0FH,R29 ;IS IT FAST MODE
174 6094  '0650              JNE     READ4
175 6096   a3f72e    RLOOP1  SBIT0   CSBIT    ;ENABLE ADC
176 6099   720419            MOV     #04H,R25 ;CHANNEL 4 – FAST MODE
177 609c   224c              MOV     #4CH,A   ;CHANNEL 4,16BITS,MSB 1ST
178 609e   721414            MOV     #20,R20  ;DO 20 FAST THEN UPDATE
179 60a1   f70631            MOV     #06H,SPICTL
180 60a4   2139      RLOOP2  MOV     A,SPIDAT
181 60a6  'a74031fc  RFLG1   JBIT0   SPIF,RFLG1 ;WAIT FOR DATA
182 60aa   a21537            MOV     SPIBUF,R21
183 60ad   2139              MOV     A,SPIDAT
184 60af  'a74031fc  RFLG2   JBIT0   SPIF,RFLG2 ;WAIT FOR DATA
185 60b3   a21637            MOV     SPIBUF,R22
186 60b6   ff                NOP               ;GIVE TIME FOR
187 60b7   ff                NOP               ; CONVERSION TO
188 60b8   ff                NOP               ;  COMPLETE
189 60b9  'da14e8            DJNZ    R20,RLOOP2
190                  ;DISPLAY VALUE
191 60bc   42151a            MOV     R21,R26
192 60bf   d71a              SWAP    R26
193 60c1   730f1a            AND     #0FH,R26   ;SAVE MSDIGIT IN R26
194 60c4   42151b            MOV     R21,R27
195 60c7   730f1b            AND     #0FH,R27   ;SAVE MIDDLE DIGIT IN R27
196 60ca   42161c            MOV     R22,R28
197 60cd   d71c              SWAP    R28
198 60cf   730f1c            AND     #0FH,R28      ;SAVE LSDIGIT IN R28
199 60d2  '8e614d            CALL    DISPLAY
200 60d5   a4082e            SBIT1   CSBIT         ;DISABLE ADC
201                  ;SEE IF FAST MODE STILL SELECTED
202 60d8   8022              MOV     ADATA,A ;WAIT FOR CHANGE
203 60da   b7                SWAP    A
204 60db   230f              AND     #0FH,A
205 60dd * 4d001d            CMP     A,R29
206 60e0  '02b4              JEQ     RLOOP1
207 60e2 *'89ff7b            JMP     READ1
208 60e5   f9                RTS
209                  ;
210                  ; SETUP CHANNEL # IN R25
211                  ;
212 60e6   421d19    READ4   MOV     R29,R25
213 60e9   720218            MOV     #02,R24  ;SET DELAY TO .5SEC
214 60ec   f9                RTS
215                  ;
216                  ;;;;;;;;;;;;;;;;;;;;;;;;
217                  ;;;;;;;;;;;;;;;;;;;;;;;;
218                  ;
219                  ; ADC
220                  ;
```

```
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adc_evm.asm                                                          PAGE    5

221                    ;       THIS ROUTINE DIGITIZES THE INPUT ON
222                    ;       THE CHANNEL SPECIFIED IN R25.  THE RESULTS
223                    ;       ARE PLACED IN REGISTERS R26, R27, AND R28.
224                    ;
225 60ed   1219        ADC     MOV     R25,A
226 60ef   b7                  SWAP    A
227 60f0   23f0                AND     #0F0H,A ;CHANNEL # IN MS NIBBLE
228 60f2   240c                OR      #0CH,A  ;16 BITS, MSB 1ST, BINARY
229 60f4   a3f72e              SBIT0   CSBIT   ;ENABLE ADC
230 60f7   f70631              MOV     #06H,SPICTL
231 60fa   2139                MOV     A,SPIDAT
232 60fc  ’a74031fc    ADCFLG1 JBIT0   SPIF,ADCFLG1  ;WAIT FOR DATA
233 6100   a21537              MOV     SPIBUF,R21    ;SAVE MSBYTE
234 6103   2139                MOV     A,SPIDAT
235 6105  ’a74031fc    ADCFLG2 JBIT0   SPIF,ADCFLG2  ;WAIT FOR DATA
236 6109   a21637              MOV     SPIBUF,R22    ;SAVE LSBYTE
237                    ;
238                    ; SAVE DATA
239                    ;
240 610c   42151a              MOV     R21,R26
241 610f   d71a                SWAP    R26
242 6111   730f1a              AND     #0FH,R26    ;SAVE MSDIGIT IN R26
243 6114   42151b              MOV     R21,R27
244 6117   730f1b              AND     #0FH,R27    ;SAVE MIDDLE DIGIT IN R27
245 611a   42161c              MOV     R22,R28
246 611d   d71c                SWAP    R28
247 611f   730f1c              AND     #0FH,R28      ;SAVE LSDIGIT IN R28
248 6122   a4082e              SBIT1   CSBIT         ;DISABLE ADC
249 6125   f9                  RTS
250                    ;
251                    ;;;;;;;;;;;;;;;;;;;;;;;;
252                    ;;;;;;;;;;;;;;;;;;;;;;;;
253                    ;
254                    ; DELAY
255                    ;       THIS ROUTINE USES TIMER 1 AS
256                    ;       A GENERAL PURPOSE TIMER TO
257                    ;       DELAY 0, .5, OR 2 SECONDS.
258                    ;       R24 IS SET AS FOLLOWS:
259                    ;               1=0 SEC.
260                    ;               2=.5 SEC.
261                    ;               3=2 SEC.
262                    ;
263 6126   7d0118      DELAY   CMP     #1,R24        ;SEE IF NO DELAY
264 6129  ’0601                JNE     DELAY1
265 612b   f9                  RTS
266 612c   7d0218      DELAY1  CMP     #2,R24        ;SEE IF .5 SEC DELAY
267 612f  ’0614                JNE     DELAY2
268 6131   f71642              MOV     #16H,TC11     ;.5 SEC COMPARE VALUE
269 6134   f7e343              MOV     #0E3H,TC12
270 6137   a40749      DLOOP   OR      #07H,T1CTL1   ;SET PRESCALER TO 256
271 613a   a4014a              OR      #1,T1CTL2     ;START COUNTER AT ZERO
272 613d   a3df4b              SBIT0   TOUT          ;CLR CMP FLAG
273 6140  ’a7204bfc    DFLAG1  JBIT0   TOUT,DFLAG1   ;WAIT FOR TIMEOUT
274 6144   f9                  RTS
275 6145   f75b42      DELAY2  MOV     #5BH,TC11     ;2 SEC COMPARE VALUE
```

```
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adc_evm.asm                                                          PAGE    6

276 6148   f78d43           MOV     #8DH,TC12
277 614b  ’00ea             JMP     DLOOP
278                  ;
279                  ;;;;;;;;;;;;;;;;;;;;;;;;
280                  ;;;;;;;;;;;;;;;;;;;;;;;;
281                  ;
282                  ; DISPLAY
283                  ;
284                  ;       THIS ROUTINE DISPLAYS THE HEX
285                  ;       DIGITS STORED IN REGS R26, R27,
286                  ;       AND R28.
287                  ;
288 614d   321a      DISPLAY MOV     R26,B      ;OUTPUT LSD
289 614f  ’aa6175           MOV     *DTBL[B],A
290 6152   2122             MOV     A,ADATA
291 6154   a3df2e           SBIT0   DOUT1      ;STROBE IT
292 6157   a4202e           SBIT1   DOUT1
293 615a   321b             MOV     R27,B      ;OUTPUT MIDDLE DIGIT
294 615c  ’aa6175           MOV     *DTBL[B],A
295 615f   2122             MOV     A,ADATA
296 6161   a3bf2e           SBIT0   DOUT2
297 6164   a4402e           SBIT1   DOUT2
298 6167   321c             MOV     R28,B      ;OUTPUT MSD
299 6169  ’aa6175           MOV     *DTBL[B],A
300 616c   2122             MOV     A,ADATA
301 616e   a37f2e           SBIT0   DOUT3
302 6171   a4802e           SBIT1   DOUT3
303 6174   f9               RTS
304 6175   00        DTBL    .BYTE   00H     ;0
305 6176   08               .BYTE   08H     ;1
306 6177   04               .BYTE   04H     ;2
307 6178   0c               .BYTE   0CH     ;3
308 6179   02               .BYTE   02H     ;4
309 617a   0a               .BYTE   0AH     ;5
310 617b   06               .BYTE   06H     ;6
311 617c   0e               .BYTE   0EH     ;7
312 617d   01               .BYTE   01H     ;8
313 617e   09               .BYTE   09H     ;9
314 617f   05               .BYTE   05H     ;A
315 6180   0d               .BYTE   0DH     ;B
316 6181   03               .BYTE   03H     ;C
317 6182   0b               .BYTE   0BH     ;D
318 6183   07               .BYTE   07H     ;E
319 6184   0f               .BYTE   0FH     ;F
320                  ;;;;;;;;;;;;;;;;;;;;;;;;
321                  ;;;;;;;;;;;;;;;;;;;;;;;;
322 7ffe                    .SECT   ”RESET”,7FFEH   ;RESET VECTOR ADDR
323 7ffe   6000             .WORD   6000H   ;PROGRAM START
324                  ;
325                         .END

 No Errors,  No Warnings
```

3.2 Flowcharts

The flowcharts for the TLV2543 EVM are shown in the following figures.

Figure 3–1. Main Program Flowchart

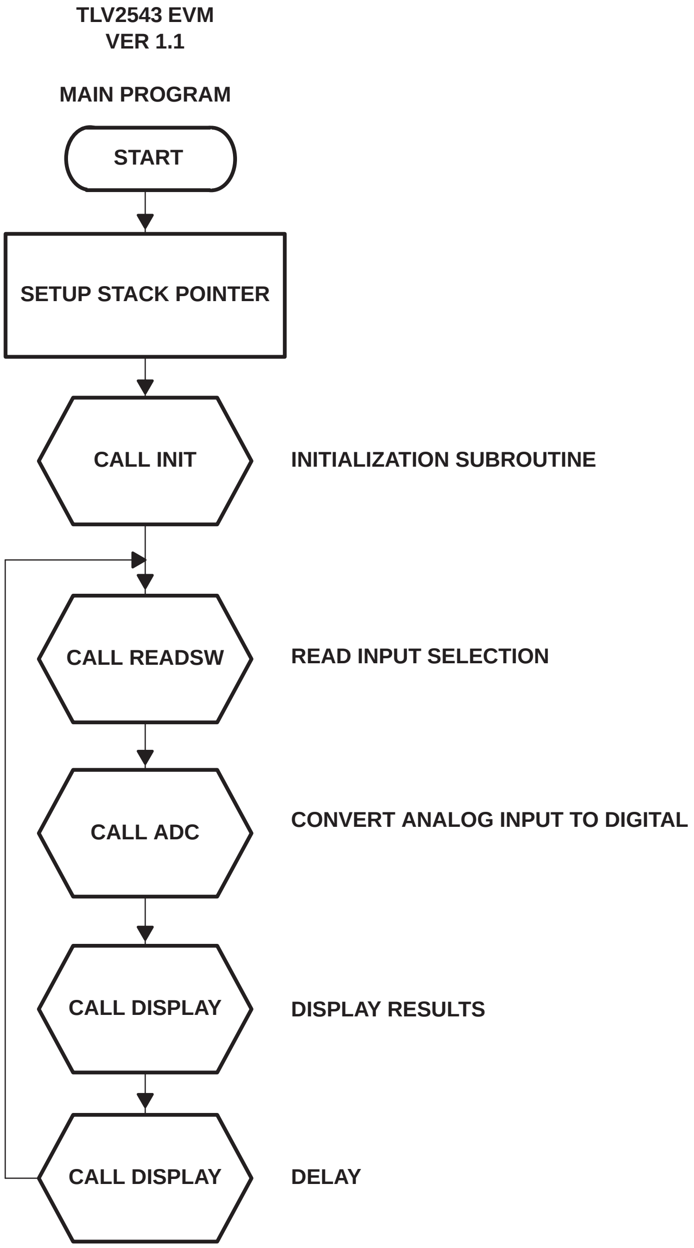


Figure 3–2. Initialization Subroutine Flowchart

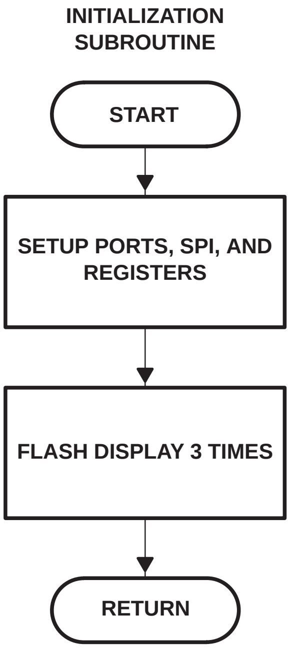


Figure 3–3. Read Input Switch Subroutine Flowchart

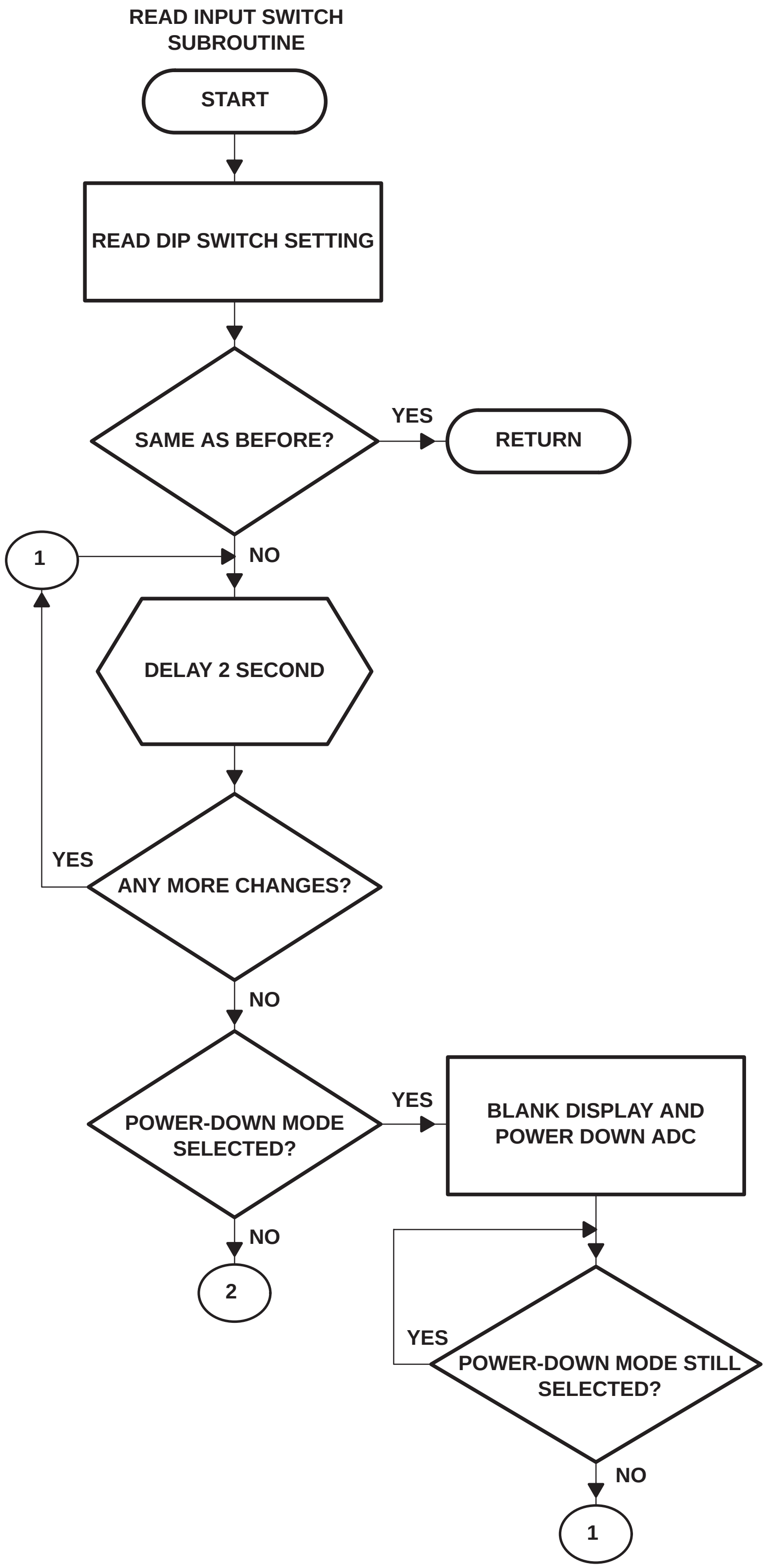


Figure 3–3 Read Input Switch Subroutine Flowchart (continued)

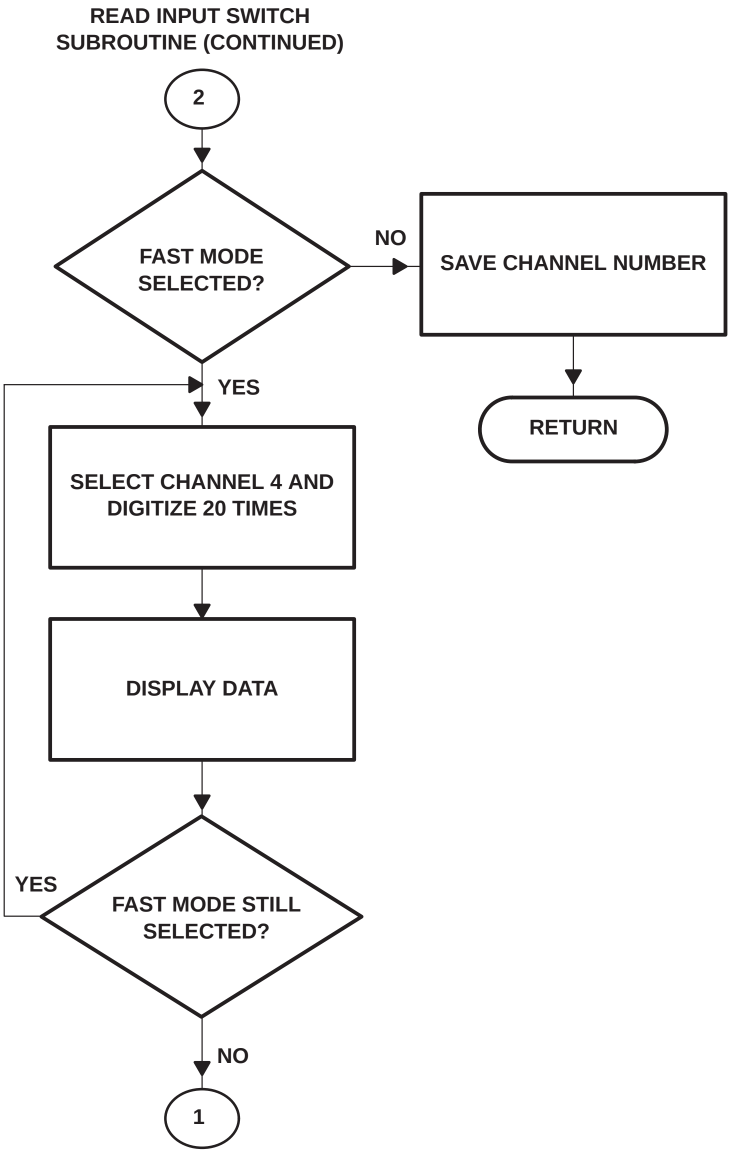


Figure 3–4. Analog-to-Digital Convert Subroutine Flowchart

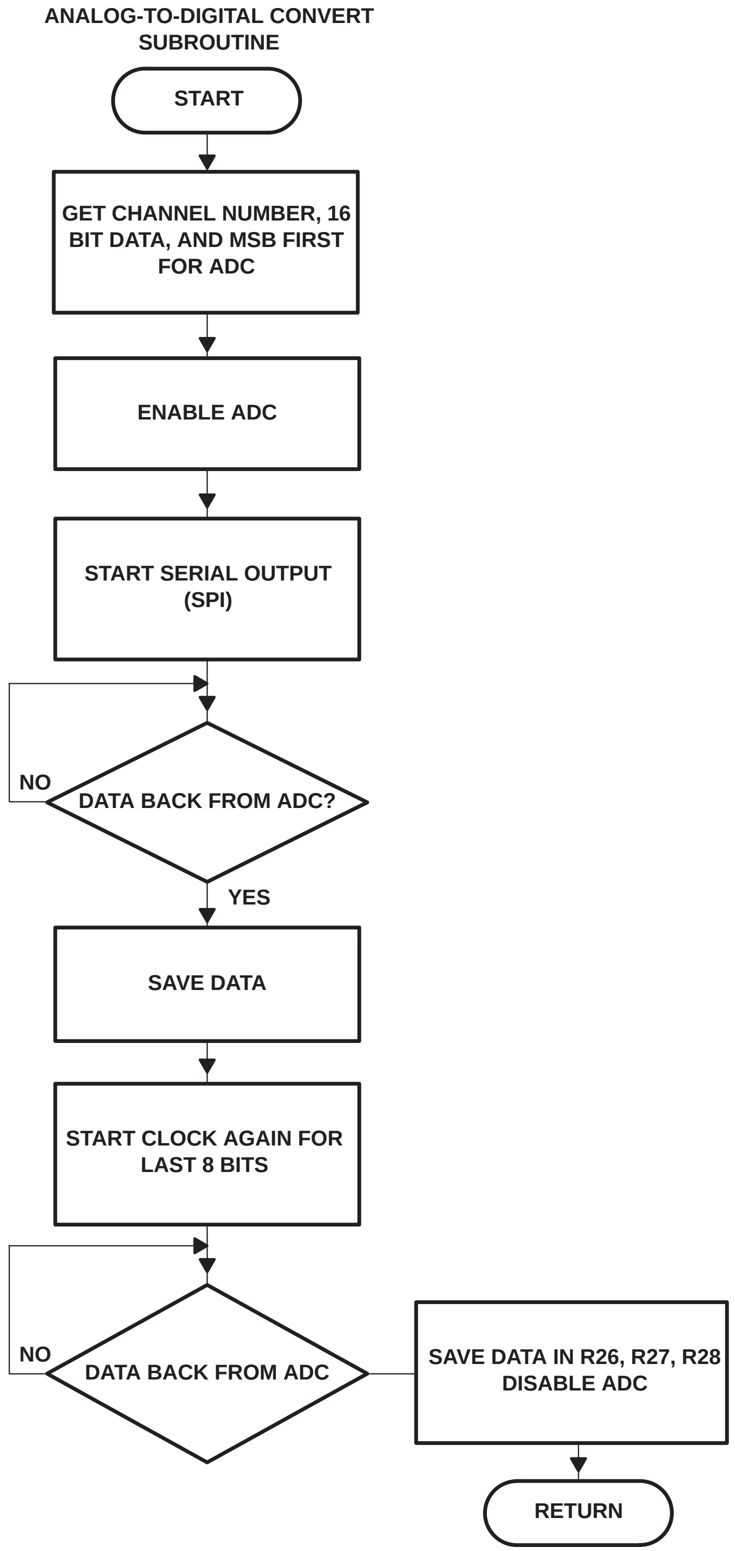


Figure 3–5. Delay Subroutine Flowchart

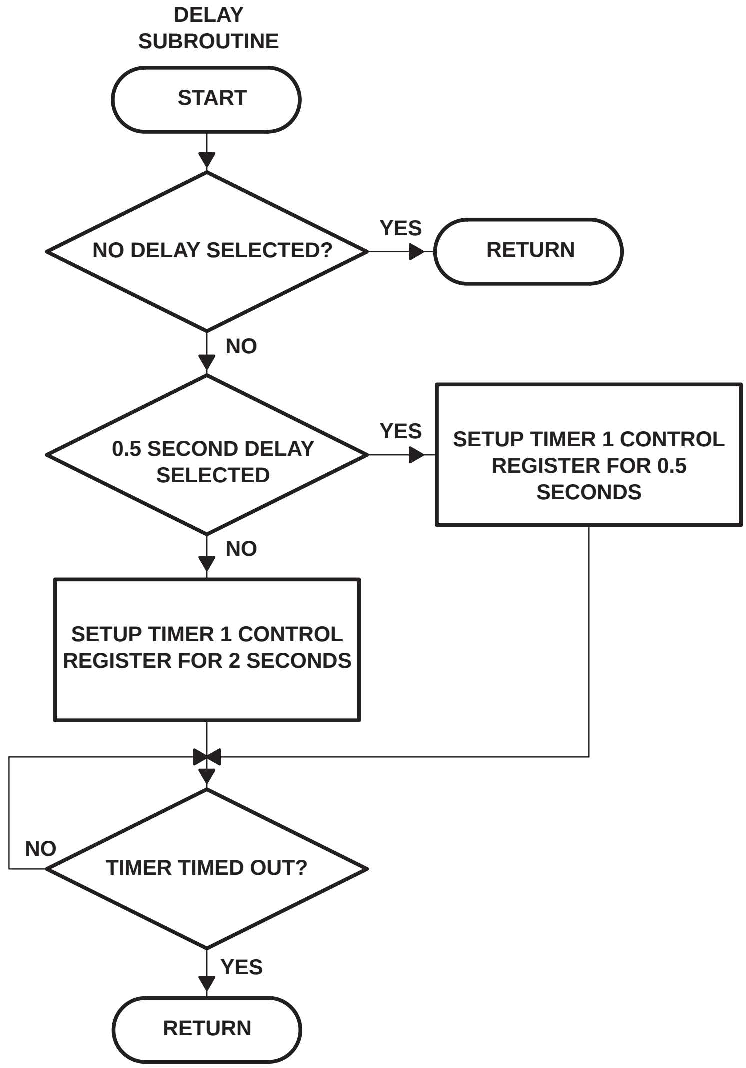
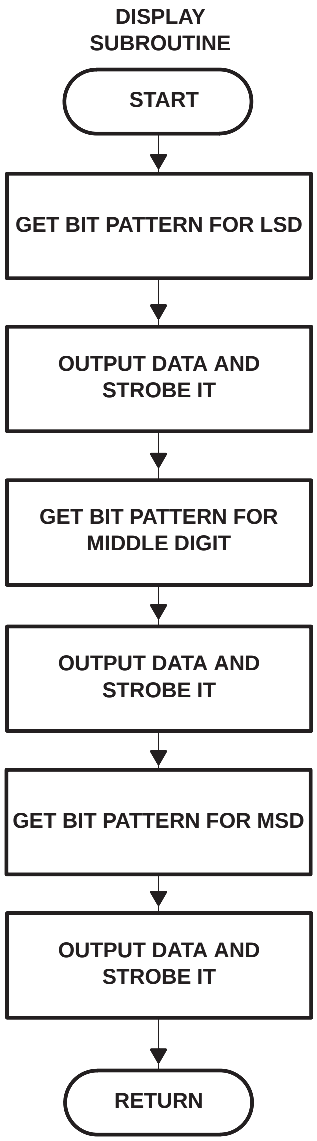


Figure 3–6. Display Subroutine Flowchart



Appendix A

TLC2543 Data Sheet

This appendix includes the TLV2543 data sheet.

Topic **Page**

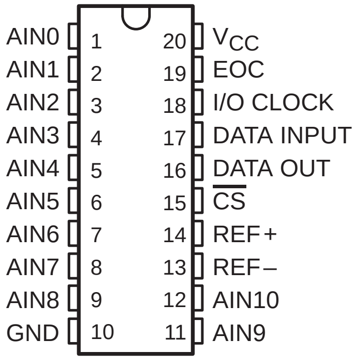
TVC2543 Data Sheet A-2

TLC2543C, TLC2543I
12-BIT ANALOG-TO-DIGITAL CONVERTERS WITH SERIAL CONTROL AND 11 ANALOG INPUTS

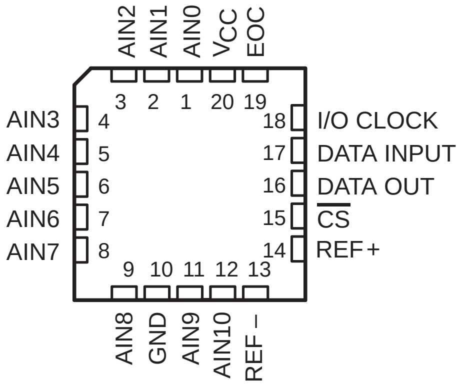
SLAS079C – DECEMBER 1993 – REVISED JUNE 1996

- **12-Bit-Resolution A/D Converter**
- **10-µs Conversion Time Over Operating Temperature**
- **11 Analog Input Channels**
- **3 Built-In Self-Test Modes**
- **Inherent Sample and Hold**
- **Linearity Error . . . ±1 LSB Max**
- **On-Chip System Clock**
- **End-of-Conversion (EOC) Output**
- **Unipolar or Bipolar Output Operation (Signed Binary With Respect to 1/2 the Applied Voltage Reference)**
- **Programmable MSB or LSB First**
- **Programmable Power Down**
- **Programmable Output Data Length**
- **CMOS Technology**
- **Application Report Available**†

DB, DW, OR N PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



description

The TLC2543C and TLC2543I are 12-bit, switched-capacitor, successive-approximation, analog-to-digital converters. Each device has three control inputs [chip select ($\overline{CS}$), the input-output clock (I/O CLOCK), and the address input (DATA INPUT)] and is designed for communication with the serial port of a host processor or peripheral through a serial 3-state output. The device allows high-speed data transfers from the host.

In addition to the high-speed converter and versatile control capability, the device has an on-chip 14-channel multiplexer that can select any one of 11 inputs or any one of three internal self-test voltages. The sample-and-hold function is automatic. At the end of conversion, the end-of-conversion (EOC) output goes high to indicate that conversion is complete. The converter incorporated in the device features differential high-impedance reference inputs that facilitate ratiometric conversion, scaling, and isolation of analog circuitry from logic and supply noise. A switched-capacitor design allows low-error conversion over the full operating temperature range.

The TLC2543 is available in the DB, DW, FN, and N packages. The TLC2543C is characterized for operation from 0°C to 70°C, and the TLC2543I is characterized for operation from –40°C to 85°C.

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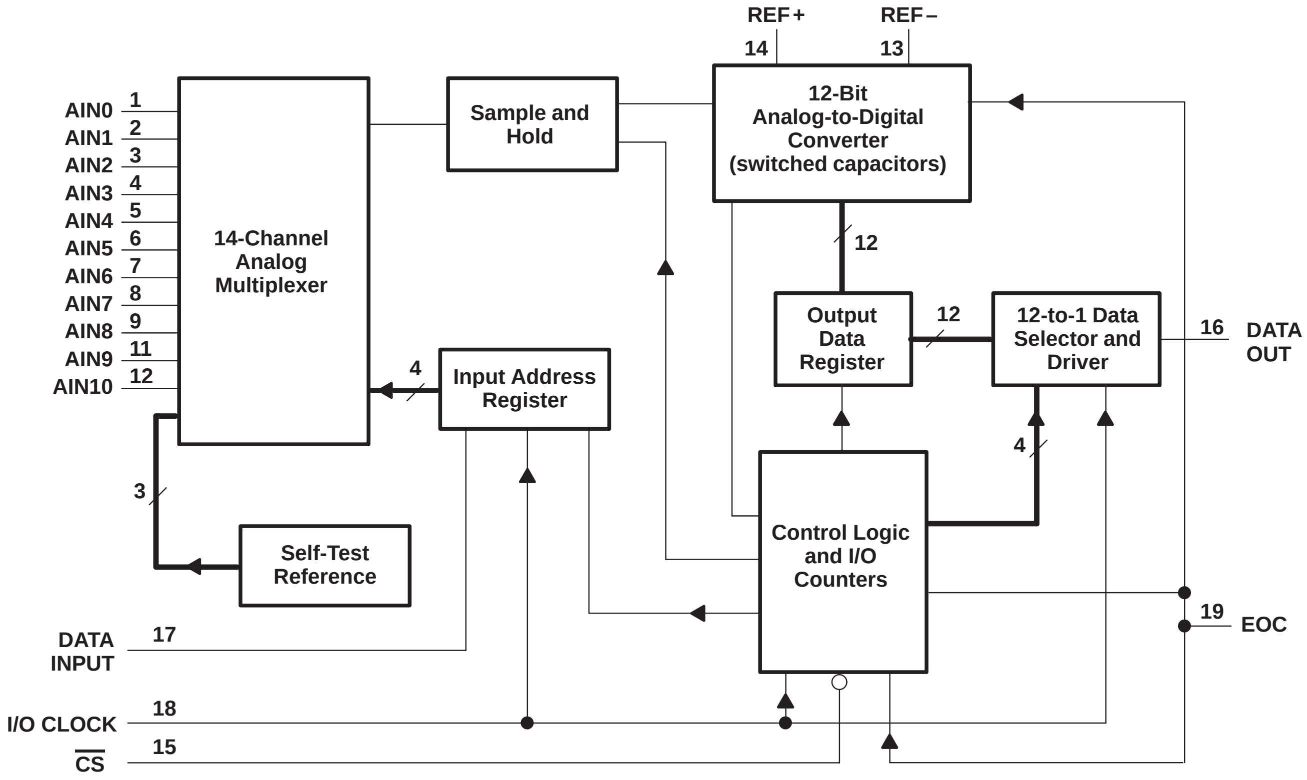
† Microcontroller Based Data Acquisition Using the TLC2543 12-bit Serial-Out ADC (SLAA012)

AVAILABLE OPTIONS

T_A	PACKAGE			
	SMALL OUTLINE (DB)‡	SMALL OUTLINE (DW)‡	PLASTIC CHIP CARRIER (FN)‡	PLASTIC DIP (N)
0°C to 70°C	TLC2543CDB	TLC2543CDW	TLC2543CFN	TLC2543CN
–40°C to 85°C	—	TLC2543IDW	TLC2543IFN	TLC2543IN

‡ Available in tape and reel and ordered as the TLC2543CDBLE, TLC2543CDWR, TLC2543IDWR, TLC2543CFNR, or TLC2543IFNR.

functional block diagram



Terminal Functions

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
AIN0 – AIN10	1 – 9, 11, 12	I	Analog input. These 11 analog-signal inputs are internally multiplexed. The driving source impedance should be less than or equal to 50 Ω for 4.1-MHz I/O CLOCK operation and capable of slewing the analog input voltage into a capacitance of 60 pF.
$\overline{\text{CS}}$	15	I	Chip select. A high-to-low transition on $\overline{\text{CS}}$ resets the internal counters and controls and enables DATA OUT, DATA INPUT, and I/O CLOCK. A low-to-high transition disables DATA INPUT and I/O CLOCK within a setup time.
DATA INPUT	17	I	Serial-data input. A 4-bit serial address selects the desired analog input or test voltage to be converted next. The serial data is presented with the MSB first and is shifted in on the first four rising edges of I/O CLOCK. After the four address bits are read into the address register, I/O CLOCK clocks the remaining bits in order.
DATA OUT	16	O	The 3-state serial output for the A/D conversion result. DATA OUT is in the high-impedance state when $\overline{\text{CS}}$ is high and active when $\overline{\text{CS}}$ is low. With a valid $\overline{\text{CS}}$, DATA OUT is removed from the high-impedance state and is driven to the logic level corresponding to the MSB/LSB value of the previous conversion result. The next falling edge of I/O CLOCK drives DATA OUT to the logic level corresponding to the next MSB / LSB, and the remaining bits are shifted out in order.
EOC	19	O	End of conversion. EOC goes from a high to a low logic level after the falling edge of the last I/O CLOCK and remains low until the conversion is complete and data are ready for transfer.
GND	10		Ground. GND is the ground return terminal for the internal circuitry. Unless otherwise noted, all voltage measurements are with respect to GND.
I/O CLOCK	18	I	Input/output clock. I/O CLOCK receives the serial input and performs the following four functions: 1. It clocks the eight input data bits into the input data register on the first eight rising edges of I/O CLOCK with the multiplexer address available after the fourth rising edge. 2. On the fourth falling edge of I/O CLOCK, the analog input voltage on the selected multiplexer input begins charging the capacitor array and continues to do so until the last falling edge of I/O CLOCK. 3. It shifts the 11 remaining bits of the previous conversion data out on DATA OUT. Data changes on the falling edge of I/O CLOCK. 4. It transfers control of the conversion to the internal state controller on the falling edge of the last I/O CLOCK.
REF +	14	I	Positive reference voltage The upper reference voltage value (nominally V_{CC}) is applied to REF+. The maximum input voltage range is determined by the difference between the voltage applied to this terminal and the voltage applied to the REF – terminal.
REF –	13	I	Negative reference voltage. The lower reference voltage value (nominally ground) is applied to REF –.
V_{CC}	20		Positive supply voltage

detailed description

Initially, with chip select ($\overline{\text{CS}}$) high, I/O CLOCK and DATA INPUT are disabled and DATA OUT is in the high-impedance state. $\overline{\text{CS}}$, going low begins the conversion sequence by enabling I/O CLOCK and DATA INPUT and removes DATA OUT from the high-impedance state.

The input data is an 8-bit data stream consisting of a 4-bit analog channel address (D7 – D4), a 2-bit data length select (D3 – D2), an output MSB or LSB first bit (D1), and a unipolar or bipolar output select bit (D0) that are applied to DATA INPUT. The I/O CLOCK sequence applied to the I/O CLOCK terminal transfers this data to the input data register.

During this transfer, the I/O CLOCK sequence also shifts the previous conversion result from the output data register to DATA OUT. I/O CLOCK receives the input sequence of 8, 12, or 16 clocks long depending on the data-length selection in the input data register. Sampling of the analog input begins on the fourth falling edge of the input I/O CLOCK sequence and is held after the last falling edge of the I/O CLOCK sequence. The last falling edge of the I/O CLOCK sequence also takes EOC low and begins the conversion.

converter operation

The operation of the converter is organized as a succession of two distinct cycles: 1) the I/O cycle and 2) the actual conversion cycle. The I/O cycle is defined by the externally provided I/O CLOCK and lasts 8, 12, or 16 clock periods, depending on the selected output data length.

1. I/O cycle

   During the I/O cycle, two operations take place simultaneously.

   a. An 8-bit data stream consisting of address and control information is provided to DATA INPUT. This data is shifted into the device on the rising edge of the first eight I/O CLOCKs. DATA INPUT is ignored after the first eight clocks during 12 or 16 clock I/O transfers.

   b. The data output, with a length of 8, 12, or 16 bits, is provided serially on DATA OUT. When $\overline{CS}$ is held low, the first output data bit occurs on the rising edge of EOC. When $\overline{CS}$ is negated between conversions, the first output data bit occurs on the falling edge of $\overline{CS}$. This data is the result of the previous conversion period, and after the first output data bit, each succeeding bit is clocked out on the falling edge of each succeeding I/O CLOCK.

2. Conversion cycle

   The conversion cycle is transparent to the user, and it is controlled by an internal clock synchronized to I/O CLOCK. During the conversion period, the device performs a successive-approximation conversion on the analog input voltage. The EOC output goes low at the start of the conversion cycle and goes high when conversion is complete and the output data register is latched. A conversion cycle is started only after the I/O cycle is completed, which minimizes the influence of external digital noise on the accuracy of the conversion.

power up and initialization

After power up, $\overline{CS}$ must be taken from high to low to begin an I/O cycle. EOC is initially high, and the input data register is set to all zeroes. The contents of the output data register are random, and the first conversion result should be ignored. To initialize during operation, $\overline{CS}$ is taken high and returned low to begin the next I/O cycle. The first conversion after the device has returned from the power-down state may not read accurately due to internal device settling.

operational terminology

Current (N) I/O cycle	The entire I/O CLOCK sequence that transfers address and control data into the data register and clocks the digital result from the previous conversion from DATA OUT
Current (N) conversion cycle	The conversion cycle starts immediately after the current I/O cycle. The end of the current I/O cycle is the last clock falling edge in the I/O CLOCK sequence. The current conversion result is loaded into the output register when conversion is complete.
Current (N) conversion result	The current conversion result is serially shifted out on the next I/O cycle.
Previous (N – 1) conversion cycle	The conversion cycle just prior to the current I/O cycle
Next (N + 1) I/O cycle	The I/O period that follows the current conversion cycle

Example: In the 12-bit mode, the result of the current conversion cycle is a 12-bit serial-data stream clocked out during the next I/O cycle. The current I/O cycle must be exactly 12 bits long to maintain synchronization, even when this corrupts the output data from the previous conversion. The current conversion is begun immediately after the twelfth falling edge of the current I/O cycle.

data input

The data input is internally connected to an 8-bit serial-input address and control register. The register defines the operation of the converter and the output data length. The host provides the data word with the MSB first. Each data bit is clocked in on the rising edge of the I/O CLOCK sequence (see Table 1 for the data input-register format).

Table 1. Input-Register Format

FUNCTION SELECT	INPUT DATA BYTE							
	ADDRESS BITS				L1	L0	LSBF	BIP
	D7 (MSB)	D6	D5	D4	D3	D2	D1	D0 (LSB)
Select input channel								
AIN0	0	0	0	0				
AIN1	0	0	0	1				
AIN2	0	0	1	0				
AIN3	0	0	1	1				
AIN4	0	1	0	0				
AIN5	0	1	0	1				
AIN6	0	1	1	0				
AIN7	0	1	1	1				
AIN8	1	0	0	0				
AIN9	1	0	0	1				
AIN10	1	0	1	0				
Select test voltage								
$(V_{ref+} - V_{ref-})/2$	1	0	1	1				
V_{ref-}	1	1	0	0				
V_{ref+}	1	1	0	1				
Software power down	1	1	1	0				
Output data length								
8 bits					0	1		
12 bits					X[†]	0		
16 bits					1	1		
Output data format								
MSB first							0	
LSB first							1	
Unipolar (binary)								0
Bipolar (2s complement)								1

[†] X represents don't care condition.

data input address bits

The four MSBs (D7 – D4) of the data register address one of the 11 input channels, a reference-test voltage, or the power-down mode. The address bits affect the current conversion, which is the conversion that immediately follows the current I/O cycle. The reference voltage is nominally equal to $V_{ref+} - V_{ref-}$.

data output length

The next two bits (D3 and D2) of the data register select the output data length. The data-length selection is valid for the current I/O cycle (the cycle in which the data is read). The data-length selection, being valid for the current I/O cycle, allows device startup without losing I/O synchronization. A data length of 8, 12, or 16 bits can be selected. Since the converter has 12-bit resolution, a data length of 12 bits is suggested.

With D3 and D2 set to 00 or 10, the device is in the 12-bit data-length mode and the result of the current conversion is output as a 12-bit serial-data stream during the next I/O cycle. The current I/O cycle must be exactly 12 bits long for proper synchronization, even if this means corrupting the output data from a previous conversion. The current conversion is started immediately after the twelfth falling edge of the current I/O cycle.

With bits D3 and D2 set to 11, the 16-bit data-length mode is selected, which allows convenient communication with 16-bit serial interfaces. In the 16-bit mode, the result of the current conversion is output as a 16-bit serial-data stream during the next I/O cycle with the four LSBs always set to 0 (pad bits). The current I/O cycle must be exactly 16 bits long to maintain synchronization even if this means corrupting the output data from the previous conversion. The current conversion is started immediately after the sixteenth falling edge of the current I/O cycle.

data output length (continued)

With bits D3 and D2 set to 01, the 8-bit data-length mode is selected, which allows fast communication with 8-bit serial interfaces. In the 8-bit mode, the result of the current conversion is output as an 8-bit serial-data stream during the next I/O cycle. The current I/O cycle must be exactly eight bits long to maintain synchronization, even if this means corrupting the output data from the previous conversion. The four LSBs of the conversion result are truncated and discarded. The current conversion is started immediately after the eighth falling edge of the current I/O cycle.

Since D3 and D2 take effect on the current I/O cycle when the data length is programmed, there can be a conflict with the previous cycle when the data-word length is changed from one cycle to the next. This may occur when the data format is selected to be least significant bit first, since at the time the data length change becomes effective (six rising edges of I/O CLOCK), the previous conversion result has already started shifting out.

In actual operation, when different data lengths are required within an application and the data length is changed between two conversions, no more than one conversion result can be corrupted and only when it is shifted out in LSB-first format.

sampling period

During the sampling period, one of the analog inputs is internally connected to the capacitor array of the converter to store the analog input signal. The converter starts sampling the selected input immediately after the four address bits have been clocked into the input data register. Sampling starts on the fourth falling edge of I/O CLOCK. The converter remains in the sampling mode until the eighth, twelfth, or sixteenth falling edge of the I/O CLOCK depending on the data-length selection. After the EOC delay time from the last I/O CLOCK falling edge, the EOC output goes low indicating that the sampling period is over and the conversion period has begun. After EOC goes low, the analog input can be changed without affecting the conversion result. Since the delay from the falling edge of the last I/O CLOCK to EOC low is fixed, time-varying analog input signals can be digitized at a fixed rate without introducing systematic harmonic distortion or noise due to timing uncertainty.

After the 8-bit data stream has been clocked in, DATA INPUT should be held at a fixed digital level until EOC goes high (indicating the conversion is complete) to maximize the sampling accuracy and minimize the influence of external digital noise.

data register, LSB first

D1 in the input data register (LSB first) controls the direction of the output binary data transfer. When D1 is set to 0, the conversion result is shifted out MSB first. When set to 1, the data is shifted out LSB first. Selection of MSB first or LSB first always affects the next I/O cycle and not the current I/O cycle. When changing from one data direction to another, the current I/O cycle is never disrupted.

data register, bipolar format

D0 (BIP) in the input data register controls the binary data format used to represent the conversion result. When D0 is set to 0, the conversion result is represented as unipolar (unsigned binary) data. Nominally, the conversion result of an input voltage equal to V_{ref-} is a code of all zeros (000 . . . 0), the conversion result of an input voltage equal to V_{ref+} is a code of all ones (111 . . . 1), and the conversion result of $(V_{ref+} + V_{ref-})/2$ is a code of a one followed by zeros (100 . . . 0).

When D0 is set to 1, the conversion result is represented as bipolar (signed binary) data. Nominally, conversion of an input voltage equal to V_{ref-} is a code of a one followed by zeros (100 . . . 0), conversion of an input voltage equal to V_{ref+} is a code of a zero followed by all ones (011 . . . 1), and the conversion of $(V_{ref+} + V_{ref-})/2$ is a code of all zeros (000 . . . 0). The MSB is interpreted as the sign bit. The bipolar data format is related to the unipolar format in that the MSBs are always each other’s complement.

Selection of the unipolar or bipolar format always affects the current conversion cycle, and the result is output during the next I/O cycle. When changing between unipolar and bipolar formats, the data output during the current I/O cycle is not affected.

EOC output

The EOC signal indicates the beginning and the end of conversion. In the reset state, EOC is always high. During the sampling period (beginning after the fourth falling edge of the I/O CLOCK sequence), EOC remains high until the internal sampling switch of the converter is safely opened. The opening of the sampling switch occurs after the eighth, twelfth, or sixteenth I/O CLOCK falling edge, depending on the data-length selection in the input data register. After the EOC signal goes low, the analog input signal can be changed without affecting the conversion result.

The EOC signal goes high again after the conversion is completed and the conversion result is latched into the output data register. The rising edge of EOC returns the converter to a reset state and a new I/O cycle begins. On the rising edge of EOC, the first bit of the current conversion result is on DATA OUT when $\overline{\text{CS}}$ is low. When $\overline{\text{CS}}$ is negated between conversions, the first bit of the current conversion result occurs at DATA OUT on the falling edge of $\overline{\text{CS}}$.

data format and pad bits

D3 and D2 of the input data register determine the number of significant bits in the digital output that represent the conversion result. The LSB-first bit determines the direction of the data transfer while the BIP bit determines the arithmetic conversion. The numerical data is always justified toward the MSB in any output format.

The internal conversion result is always 12 bits long. When an 8-bit data transfer is selected, the four LSBs of the internal result are discarded to provide a faster one-byte transfer. When a 12-bit transfer is used, all bits are transferred. When a 16-bit transfer is used, four LSB pad bits are always appended to the internal conversion result. In the LSB-first mode, four leading zeros are output. In the MSB-first mode, the last four bits output are zeros.

When $\overline{\text{CS}}$ is held low continuously, the first data bit of the just completed conversion occurs on DATA OUT on the rising edge of EOC. When a new conversion is started after the last falling edge of I/O CLOCK, EOC goes low and the serial output is forced to a setting of 0 until EOC goes high again.

When $\overline{\text{CS}}$ is negated between conversions, the first data bit occurs on DATA OUT on the falling edge of $\overline{\text{CS}}$. On each subsequent falling edge of I/O CLOCK after the first data bit appears, the data is changed to the next bit in the serial conversion result until the required number of bits has been output.

chip-select input ($\overline{\text{CS}}$)

The chip-select input ($\overline{\text{CS}}$) enables and disables the device. During normal operation, $\overline{\text{CS}}$ should be low. Although the use of $\overline{\text{CS}}$ is not necessary to synchronize a data transfer, it can be brought high between conversions to coordinate the data transfer of several devices sharing the same bus.

When $\overline{\text{CS}}$ is brought high, the serial-data output is immediately brought to the high-impedance state, releasing its output data line to other devices that may share it. After an internally generated debounce time, I/O CLOCK is inhibited, thus preventing any further change in the internal state.

When $\overline{\text{CS}}$ is subsequently brought low again, the device is reset. $\overline{\text{CS}}$ must be held low for an internal debounce time before the reset operation takes effect. After $\overline{\text{CS}}$ is debounced low, I/O CLOCK must remain inactive (low) for a minimum time before a new I/O cycle can start.

$\overline{\text{CS}}$ can interrupt any ongoing data transfer or any ongoing conversion. When $\overline{\text{CS}}$ is debounced low long enough before the end of the current conversion cycle, the previous conversion result is saved in the internal output buffer and shifted out during the next I/O cycle.

power-down features

When a binary address of 1110 is clocked into the input data register during the first four I/O CLOCK cycles, the power-down mode is selected. Power down is activated on the falling edge of the fourth I/O CLOCK pulse.

During power down, all internal circuitry is put in a low-current standby mode. No conversions are performed, and the internal output buffer keeps the previous conversion cycle data results, provided that all digital inputs are held above V_{CC} – 0.5 V or below 0.5 V. The I/O logic remains active so the current I/O cycle must be completed even when the power-down mode is selected. Upon power-on reset and before the first I/O cycle, the converter normally begins in the power-down mode. The device remains in the power-down mode until a valid (other than 1110) input address is clocked in. Upon completion of that I/O cycle, a normal conversion is performed with the results being shifted out during the next I/O cycle.

analog input, test, and power-down mode

The 11 analog inputs, three internal voltages, and power-down mode are selected by the input multiplexer according to the input addresses shown in Tables 2, 3, and 4. The input multiplexer is a break-before-make type to reduce input-to-input noise rejection resulting from channel switching. Sampling of the analog input starts on the falling edge of the fourth I/O CLOCK and continues for the remaining I/O CLOCK pulses. The sample is held on the falling edge of the last I/O CLOCK pulse. The three internal test inputs are applied to the multiplexer, then sampled and converted in the same manner as the external analog inputs. The first conversion after the device has returned from the power-down state may not read accurately due to internal device settling.

Table 2. Analog-Channel-Select Address

ANALOG INPUT SELECTED	VALUE SHIFTED INTO DATA INPUT	
	BINARY	HEX
AIN0	0000	0
AIN1	0001	1
AIN2	0010	2
AIN3	0011	3
AIN4	0100	4
AIN5	0101	5
AIN6	0110	6
AIN7	0111	7
AIN8	1000	8
AIN9	1001	9
AIN10	1010	A

Table 3. Test-Mode-Select Address

INTERNAL SELF-TEST VOLTAGE SELECTED[†]	VALUE SHIFTED INTO DATA INPUT		UNIPOLAR OUTPUT RESULT (HEX)[‡]
	BINARY	HEX	
$\frac{V_{ref+} - V_{ref-}}{2}$	1011	B	200
V_{ref-}	1100	C	000
V_{ref+}	1101	D	3FF

[†] V_{ref+} is the voltage applied to REF+, and V_{ref-} is the voltage applied to REF–.
[‡] The output results shown are the ideal values and may vary with the reference stability and with internal offsets.

Table 4. Power-Down-Select Address

INPUT COMMAND	VALUE SHIFTED INTO DATA INPUT		RESULT
	BINARY	HEX	
Power down	1110	E	$I_{CC} \leq 25\ \mu A$

converter and analog input

The CMOS threshold detector in the successive-approximation conversion system determines each bit by examining the charge on a series of binary-weighted capacitors (see Figure 1). In the first phase of the conversion process, the analog input is sampled by closing the S_C switch and all S_T switches simultaneously. This action charges all the capacitors to the input voltage.

In the next phase of the conversion process, all S_T and S_C switches are opened and the threshold detector begins identifying bits by identifying the charge (voltage) on each capacitor relative to the reference (REF–) voltage. In the switching sequence, 12 capacitors are examined separately until all 12 bits are identified and the charge-convert sequence is repeated. In the first step of the conversion phase, the threshold detector looks at the first capacitor (weight = 4096). Node 4096 of this capacitor is switched to the REF+ voltage, and the equivalent nodes of all the other capacitors on the ladder are switched to REF–. When the voltage at the summing node is greater than the trip point of the threshold detector (approximately 1/2 V_{CC}), a bit 0 is placed in the output register and the 4096-weight capacitor is switched to REF–. When the voltage at the summing node is less than the trip point of the threshold detector, a bit 1 is placed in the register and this 4096-weight capacitor remains connected to REF+ through the remainder of the successive-approximation process. The process is repeated for the 2048-weight capacitor, the 1024-weight capacitor, and so forth down the line until all bits are determined. With each step of the successive-approximation process, the initial charge is redistributed among the capacitors. The conversion process relies on charge redistribution to determine the bits from MSB to LSB.

reference voltage inputs

There are two reference inputs used with the device, the voltages applied to the REF+ and REF– terminals. These voltage values establish the upper and lower limits of the analog input to produce a full-scale and zero-scale reading respectively. These voltages and the analog input should not exceed the positive supply or be lower than ground consistent with the specified absolute maximum ratings. The digital output is at full scale when the input signal is equal to or higher than REF+ terminal voltage and at zero when the input signal is equal to or lower than REF– terminal voltage.

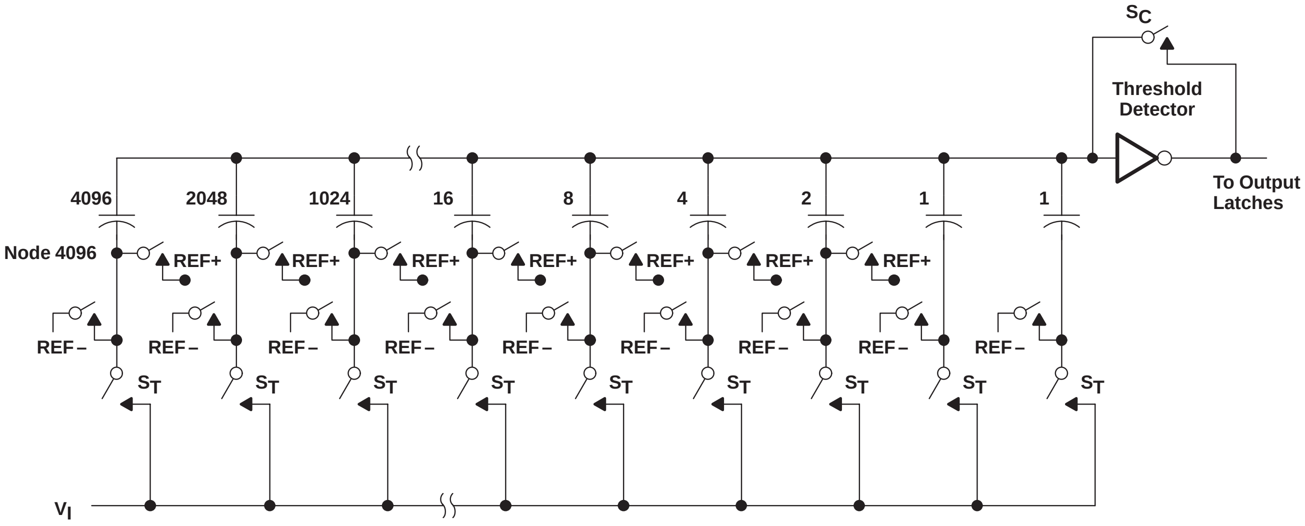


Figure 1. Simplified Model of the Successive-Approximation System

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC} (see Note 1) . . . . –0.5 V to 6.5 V
Input voltage range, V_I (any input) . . . . –0.3 V to V_{CC} + 0.3 V
Output voltage range, V_O . . . . –0.3 V to V_{CC} + 0.3 V
Positive reference voltage, V_{ref+} . . . . V_{CC} + 0.1 V
Negative reference voltage, V_{ref-} . . . . –0.1 V
Peak input current, I_I (any input) . . . . ±20 mA
Peak total input current, I_I (all inputs) . . . . ±30 mA
Operating free-air temperature range, T_A: TLC2543C . . . . 0°C to 70°C
TLC2543I . . . . –40°C to 85°C
Storage temperature range, T_{stg} . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from the case for 10 seconds . . . . 260°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to the GND terminal with REF– and GND wired together (unless otherwise noted).

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.5	5	5.5	V
Positive reference voltage, V_{ref+} (see Note 2)			V_{CC}		V
Negative reference voltage, V_{ref-} (see Note 2)			0		V
Differential reference voltage, $V_{ref+} - V_{ref-}$ (see Note 2)		2.5	V_{CC}	$V_{CC}+0.1$	V
Analog input voltage (see Note 2)		0		V_{CC}	V
High-level control input voltage, V_{IH}	V_{CC} = 4.5 V to 5.5 V	2			V
Low-level control input voltage, V_{IL}	V_{CC} = 4.5 V to 5.5 V			0.8	V
Clock frequency at I/O CLOCK		0		4.1	MHz
Setup time, address bits at DATA INPUT before I/O CLOCK↑, $t_{su(A)}$ (see Figure 5)		100			ns
Hold time, address bits after I/O CLOCK↑, $t_{h(A)}$ (see Figure 5)		0			ns
Hold time, $\overline{CS}$ low after last I/O CLOCK↓, $t_{h(CS)}$ (see Figure 6)		0			ns
Setup time, $\overline{CS}$ low before clocking in first address bit, $t_{su(CS)}$ (see Note 3 and Figure 6)		1.425			µs
Pulse duration, I/O CLOCK high, $t_{wH(I/O)}$		120			ns
Pulse duration, I/O CLOCK low, $t_{wL(I/O)}$		120			ns
Transition time, I/O CLOCK, $t_{t(I/O)}$ (see Note 4 and Figure 7)				1	µs
Transition time, DATA INPUT and $\overline{CS}$, $t_{t(CS)}$				10	µs
Operating free-air temperature, T_A	TLC2543C	0		70	°C
	TLC2543I	–40		85	

NOTES: 2. Analog input voltages greater than that applied to REF+ convert as all ones (111111111111), while input voltages less than that applied to REF– convert as all zeros (000000000000).

3. To minimize errors caused by noise at the $\overline{CS}$ input, the internal circuitry waits for a setup time after $\overline{CS}$↓ before responding to control input signals. No attempt should be made to clock in an address until the minimum $\overline{CS}$ setup time has elapsed.

4. This is the time required for the clock input signal to fall from V_{IH}min to V_{IL}max or to rise from V_{IL}max to V_{IH}min. In the vicinity of normal room temperature, the devices function with input clock transition time as slow as 1 µs for remote data acquisition applications where the sensor and the A/D converter are placed several feet away from the controlling microprocessor.

electrical characteristics over recommended operating free-air temperature range, $V_{CC} = V_{ref+}$ = 4.5 V to 5.5 V, I/O CLOCK frequency = 4.1 MHz (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage		V_{CC} = 4.5 V,	I_{OH} = –1.6 mA	2.4			V
			V_{CC} = 4.5 V to 5.5 V,	I_{OH} = –20 µA	$V_{CC}-0.1$			
V_{OL}	Low-level output voltage		V_{CC} = 4.5 V,	I_{OL} = 1.6 mA			0.4	V
			V_{CC} = 4.5 V to 5.5 V,	I_{OL} = 20 µA			0.1	
I_{OZ}	High-impedance off-state output current		$V_O = V_{CC}$,	$\overline{CS}$ at V_{CC}		1	2.5	µA
			V_O = 0,	$\overline{CS}$ at V_{CC}		1	–2.5	
I_{IH}	High-level input current		$V_I = V_{CC}$			1	2.5	µA
I_{IL}	Low-level input current		V_I = 0			1	–2.5	µA
I_{CC}	Operating supply current		$\overline{CS}$ at 0 V			1	2.5	mA
$I_{CC(PD)}$	Power-down current		For all digital inputs, $0 \le V_I \le 0.5$ V or $V_I \ge V_{CC} - 0.5$ V			4	25	µA
	Selected channel leakage current		Selected channel at V_{CC},	Unselected channel at 0 V			1	µA
			Selected channel at 0 V,	Unselected channel at V_{CC}			–1	
	Maximum static analog reference current into REF+		$V_{ref+} = V_{CC}$,	V_{ref-} = GND		1	2.5	µA
C_i	Input capacitance	Analog inputs				30	60	pF
		Control inputs				5	15	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

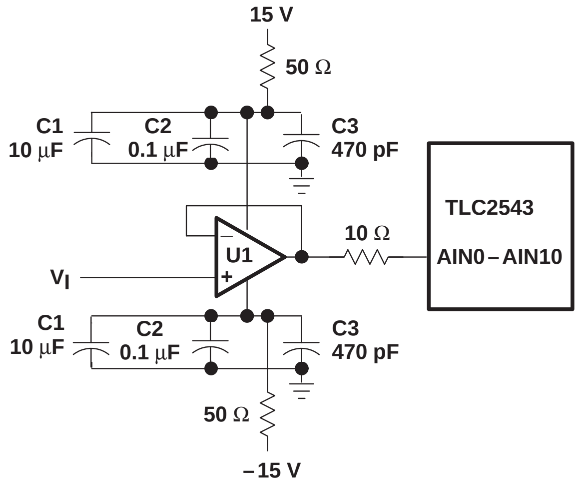
operating characteristics over recommended operating free-air temperature range, $V_{CC} = V_{ref+}$ = 4.5 V to 5.5 V, I/O CLOCK frequency = 4.1 MHz

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
E_L	Linearity error (see Note 5)	See Figure 2			±1	LSB
E_D	Differential linearity error	See Figure 2			±1	LSB
E_O	Offset error (see Note 6)	See Note 2 and Figure 2			±1.5	LSB
E_G	Gain error (see Note 6)	See Note 2 and Figure 2			±1	LSB
E_T	Total unadjusted error (see Note 7)				±1.75	LSB
	Self-test output code (see Table 3 and Note 8)	DATA INPUT = 1011		2048		
		DATA INPUT = 1100		0		
		DATA INPUT = 1101		4095		
t_{conv}	Conversion time	See Figures 10 – 15		8	10	µs
t_c	Total cycle time (access, sample, and conversion)	See Figures 10 – 15 and Note 9			10 + total I/O CLOCK periods + $t_{d(I/O-EOC)}$	µs
t_{acq}	Channel acquisition time (sample)	See Figures 10 – 15 and Note 9	4		12	I/O CLOCK periods
t_v	Valid time, DATA OUT remains valid after I/O CLOCK↓	See Figure 7	10			ns
$t_{d(I/O-DATA)}$	Delay time, I/O CLOCK↓ to DATA OUT valid	See Figure 7			150	ns
$t_{d(I/O-EOC)}$	Delay time, last I/O CLOCK↓ to EOC↓	See Figure 8		1.5	2.2	µs
$t_{d(EOC-DATA)}$	Delay time, EOC↑ to DATA OUT (MSB / LSB)	See Figure 9			100	ns
t_{PZH}, t_{PZL}	Enable time, $\overline{CS}$↓ to DATA OUT (MSB / LSB driven)	See Figure 4		0.7	1.3	µs
t_{PHZ}, t_{PLZ}	Disable time, $\overline{CS}$↑ to DATA OUT (high impedance)	See Figure 4		70	150	ns
$t_{r(EOC)}$	Rise time, EOC	See Figure 9		15	50	ns
$t_{f(EOC)}$	Fall time, EOC	See Figure 8		15	50	ns
$t_{r(bus)}$	Rise time, data bus	See Figure 7		15	50	ns
$t_{f(bus)}$	Fall time, data bus	See Figure 7		15	50	ns
$t_{d(I/O-CS)}$	Delay time, last I/O CLOCK↓ to $\overline{CS}$↓ to abort conversion (see Note 10)				5	µs

† All typical values are at T_A = 25°C.

NOTES:
2. Analog input voltages greater than that applied to REF + convert as all ones (111111111111), while input voltages less than that applied to REF – convert as all zeros (000000000000).
5. Linearity error is the maximum deviation from the best straight line through the A/D transfer characteristics.
6. Gain error is the difference between the actual midstep value and the nominal midstep value in the transfer diagram at the specified gain point after the offset error has been adjusted to zero. Offset error is the difference between the actual midstep value and the nominal midstep value at the offset point.
7. Total unadjusted error comprises linearity, zero-scale, and full-scale errors.
8. Both the input address and the output codes are expressed in positive logic.
9. I/O CLOCK period = 1 /(I/O CLOCK frequency) (see Figure 7).
10. Any transitions of $\overline{CS}$ are recognized as valid only when the level is maintained for a setup time. $\overline{CS}$ must be taken low at ≤ 5 µs of the tenth I/O CLOCK falling edge to ensure a conversion is aborted. Between 5 µs and 10 µs, the result is uncertain as to whether the conversion is aborted or the conversion results are valid.

PARAMETER MEASUREMENT INFORMATION



LOCATION	DESCRIPTION	PART NUMBER
U1	OP27	—
C1	10-µF 35-V tantalum capacitor	—
C2	0.1-µF ceramic NPO SMD capacitor	AVX 12105C104KA105 or equivalent
C3	470-pF porcelain Hi-Q SMD capacitor	Johanson 201S420471JG4L or equivalent

Figure 2. Analog Input Buffer to Analog Inputs AIN0 – AIN10

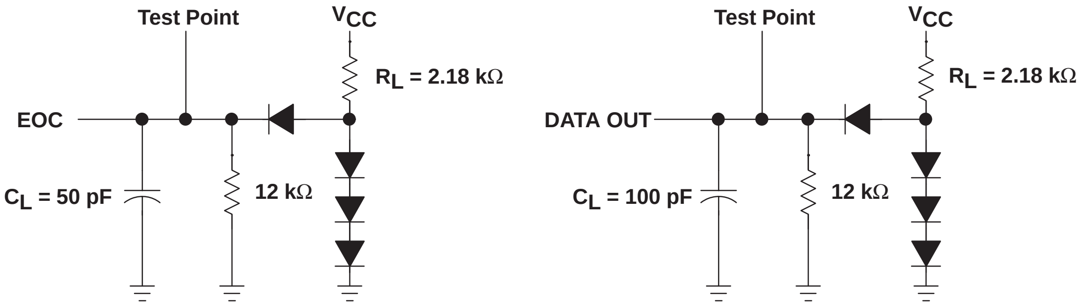


Figure 3. Load Circuits

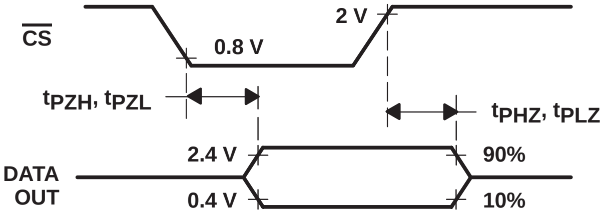


Figure 4. DATA OUT to Hi-Z Voltage Waveforms

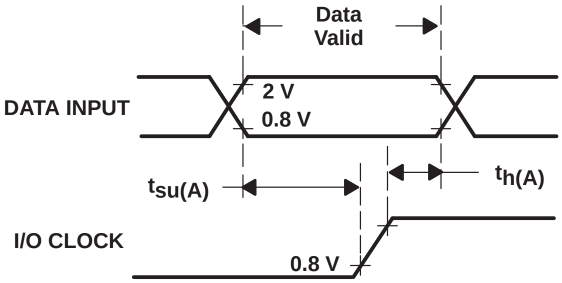


Figure 5. DATA INPUT and I/O CLOCK Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION

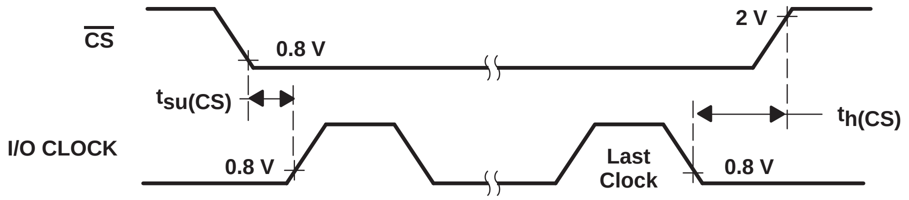


Figure 6. $\overline{CS}$ and I/O CLOCK Voltage Waveforms†

† To ensure full conversion accuracy, it is recommended that no input signal change occurs while a conversion is ongoing.

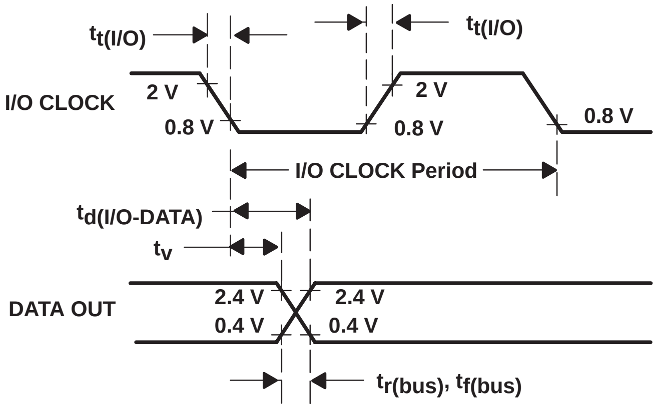


Figure 7. I/O CLOCK and DATA OUT Voltage Waveforms

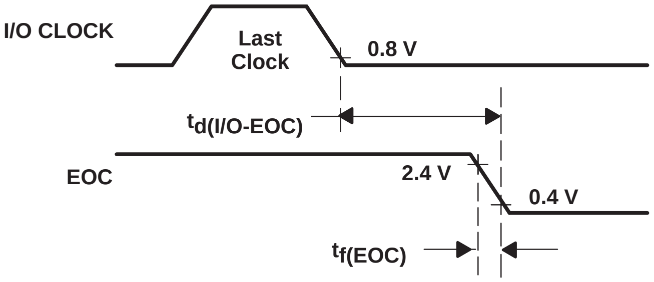


Figure 8. I/O CLOCK and EOC Voltage Waveforms

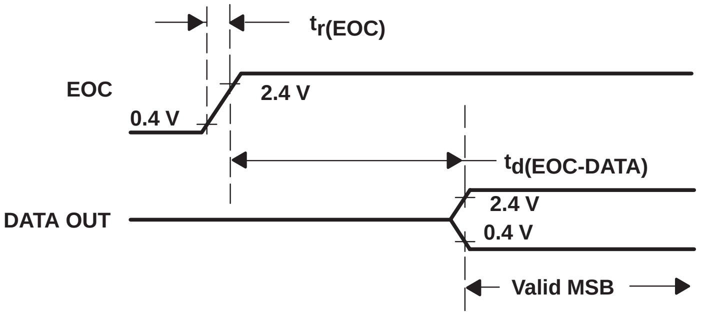


Figure 9. EOC and DATA OUT Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION

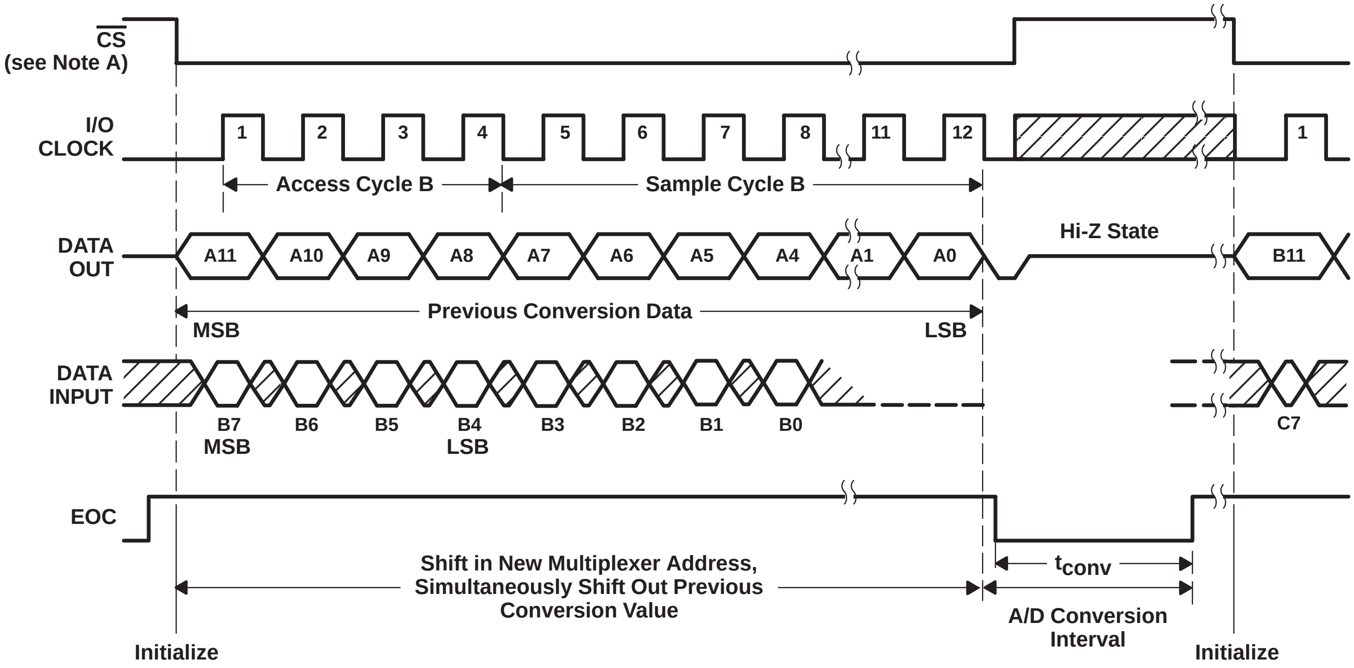


Figure 10. Timing for 12-Clock Transfer Using $\overline{\text{CS}}$ With MSB First

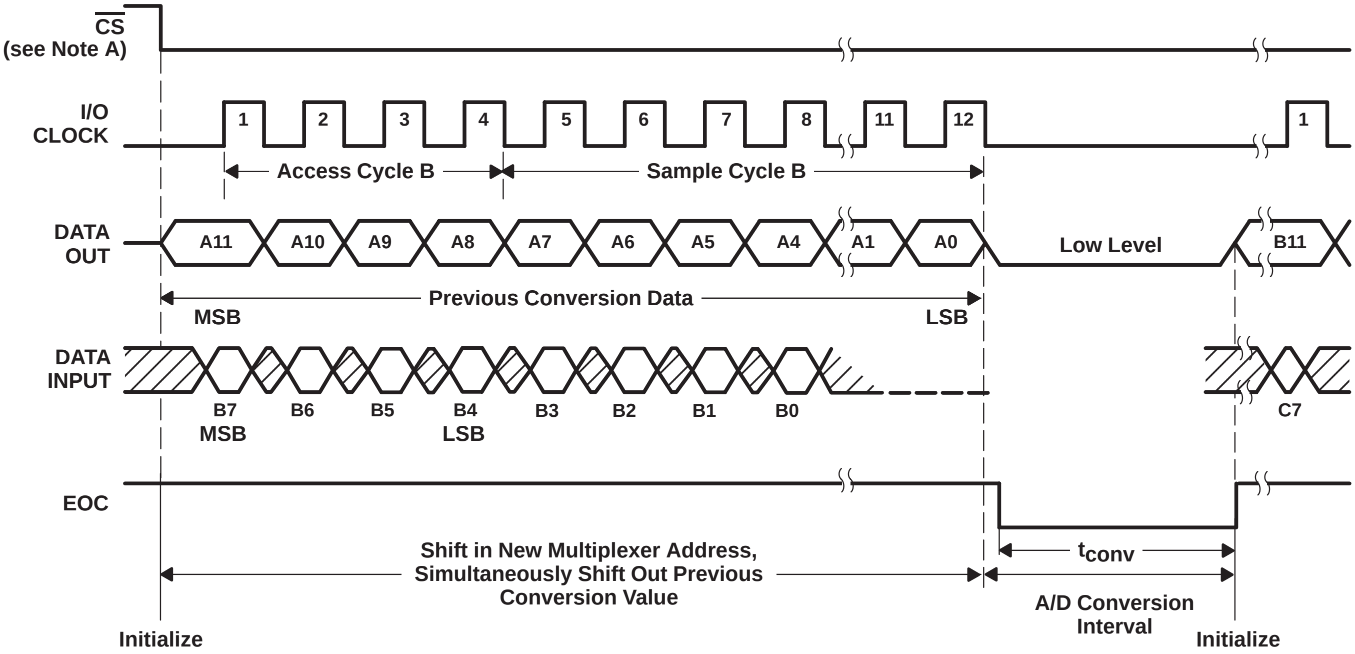


Figure 11. Timing for 12-Clock Transfer Not Using $\overline{\text{CS}}$ With MSB First

NOTE A: To minimize errors caused by noise at $\overline{\text{CS}}$, the internal circuitry waits for a setup time after $\overline{\text{CS}}$↓ before responding to control input signals. Therefore, no attempt should be made to clock in an address until the minimum $\overline{\text{CS}}$ setup time has elapsed.

PARAMETER MEASUREMENT INFORMATION

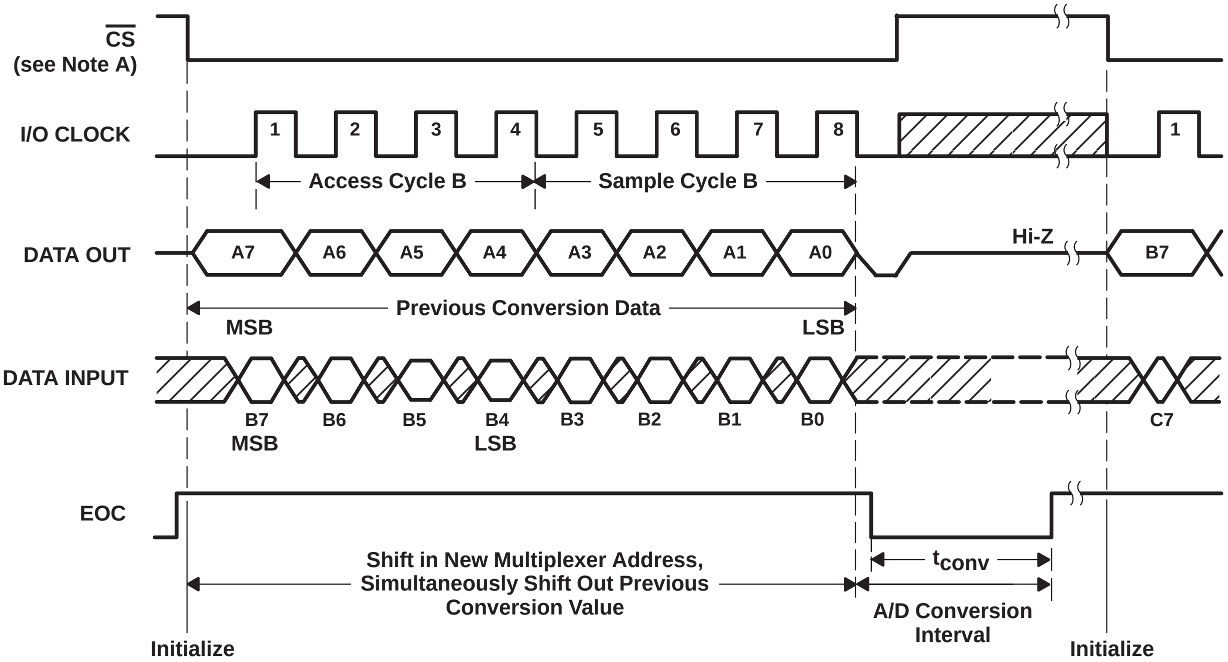


Figure 12. Timing for 8-Clock Transfer Using $\overline{CS}$ With MSB First

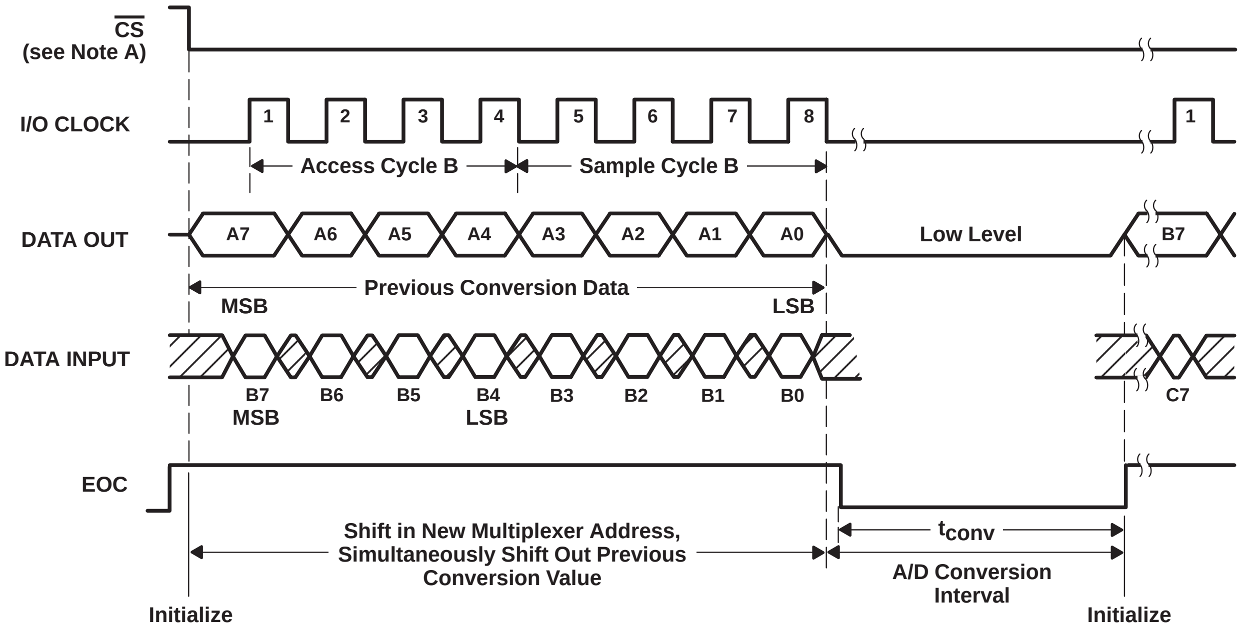


Figure 13. Timing for 8-Clock Transfer Not Using $\overline{CS}$ With MSB First

NOTE A: To minimize errors caused by noise at $\overline{CS}$, the internal circuitry waits for a setup time after $\overline{CS}$↓ before responding to control input signals. Therefore, no attempt should be made to clock in an address until the minimum $\overline{CS}$ setup time has elapsed.

PARAMETER MEASUREMENT INFORMATION

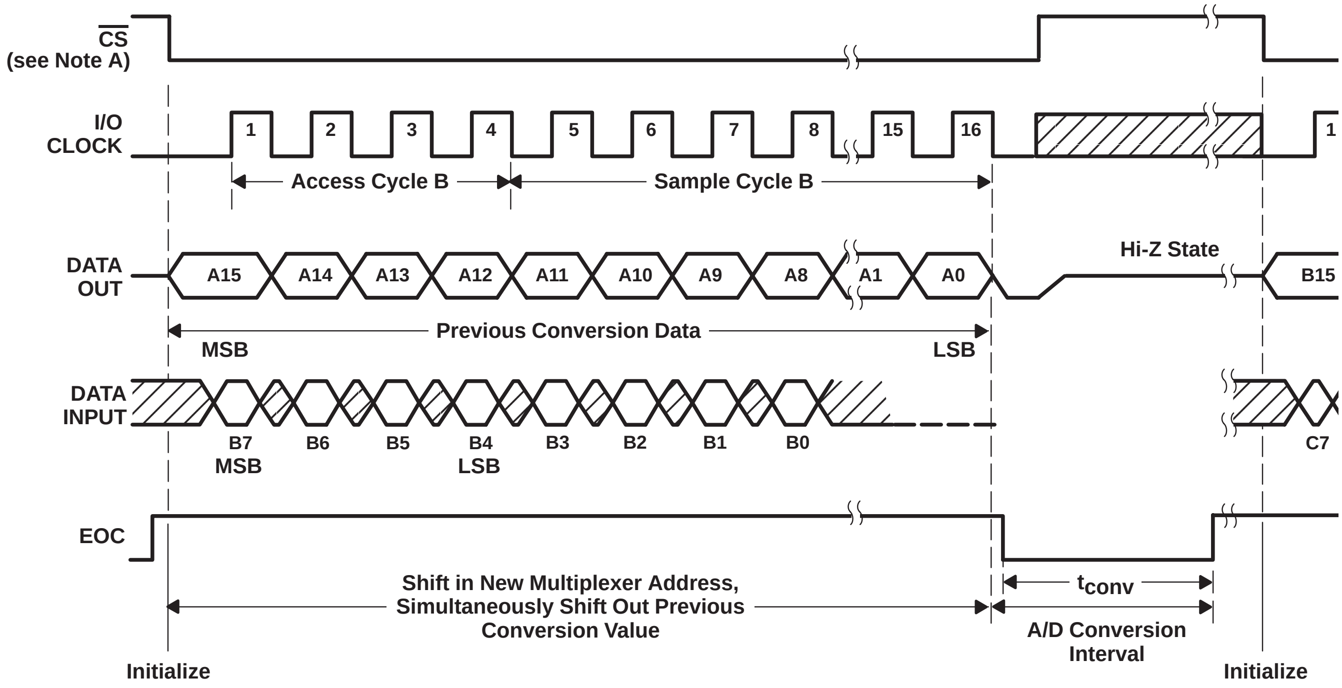


Figure 14. Timing for 16-Clock Transfer Using $\overline{\mathrm{CS}}$ With MSB First

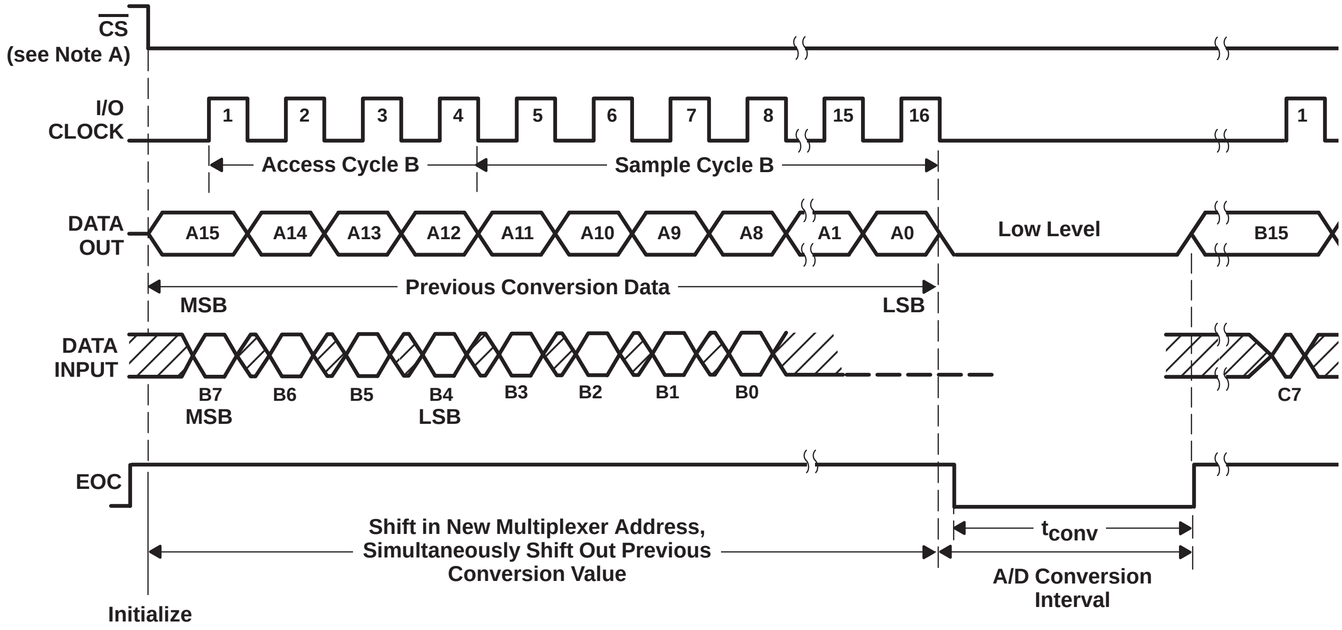
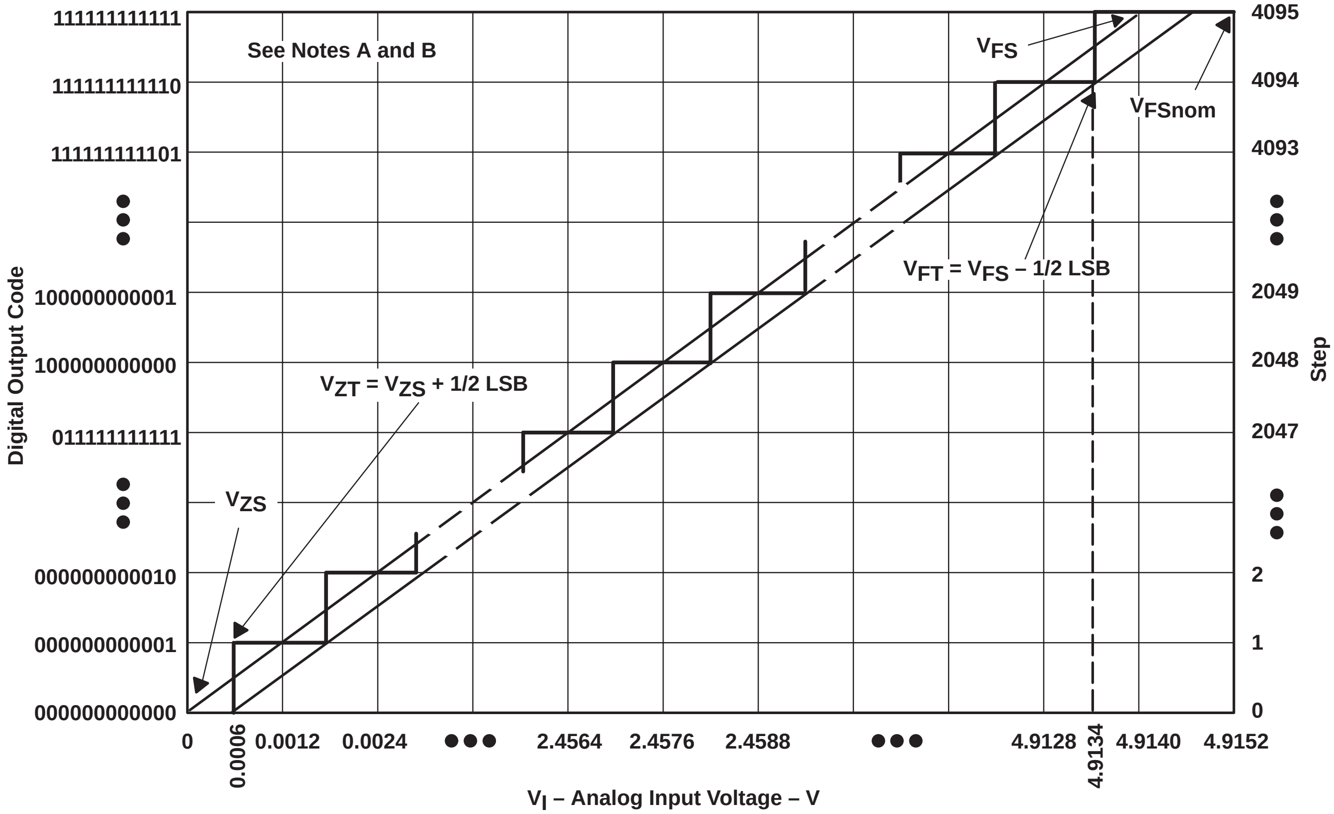


Figure 15. Timing for 16-Clock Transfer Not Using $\overline{\mathrm{CS}}$ With MSB First

NOTE A: To minimize errors caused by noise at $\overline{\mathrm{CS}}$, the internal circuitry waits for a setup time after $\overline{\mathrm{CS}}$↓ before responding to control input signals. Therefore, no attempt should be made to clock in an address until the minimum $\overline{\mathrm{CS}}$ setup time has elapsed.

APPLICATION INFORMATION



NOTES: A. This curve is based on the assumption that V_{ref+} and V_{ref-} have been adjusted so that the voltage at the transition from digital 0 to 1 (V_{ZT}) is 0.0006 V and the transition to full scale (V_{FT}) is 4.9134 V. 1 LSB = 1.2 mV.

B. The full-scale value (V_{FS}) is the step whose nominal midstep value has the highest absolute value. The zero-scale value (V_{ZS}) is the step whose nominal midstep value equals zero.

Figure 16. Ideal Conversion Characteristics

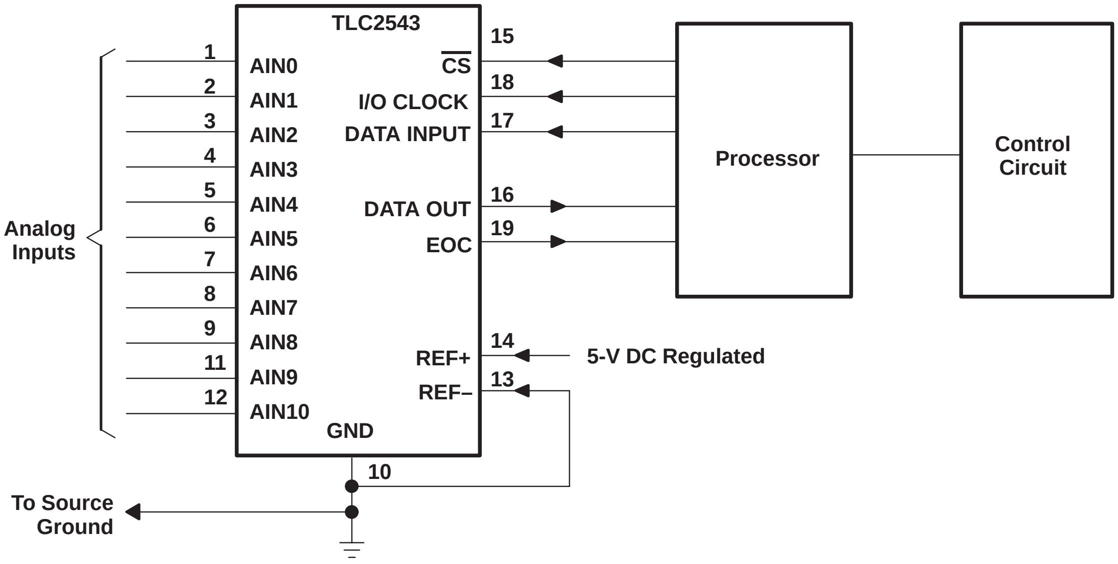


Figure 17. Serial Interface

APPLICATIONS INFORMATION

simplified analog input analysis

Using the equivalent circuit in Figure 18, the time required to charge the analog input capacitance from 0 to V_S within 1/2 LSB can be derived as follows:

The capacitance charging voltage is given by

$$V_C = V_S\left(1 - e^{-t_c / R_t C_i}\right) \tag{1}$$

where

$R_t = R_S + r_i$

The final voltage to 1/2 LSB is given by

$$V_C \text{ (1/2 LSB)} = V_S - (V_S/8192) \tag{2}$$

Equating equation 1 to equation 2 and solving for time t_c gives

$$V_S - \left(V_S/8192\right) = V_S\left(1 - e^{-t_c / R_t C_i}\right) \tag{3}$$

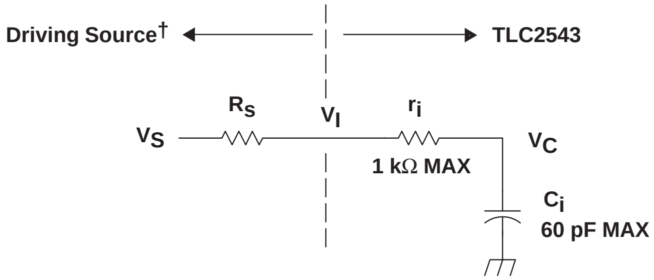
and

$$t_c \text{ (1/2 LSB)} = R_t \times C_i \times \ln(8192) \tag{4}$$

Therefore, with the values given, the time for the analog input signal to settle is

$$t_c \text{ (1/2 LSB)} = (R_S + 1\ \text{k}\Omega) \times 60\ \text{pF} \times \ln(8192) \tag{5}$$

This time must be less than the converter sample time shown in the timing diagrams.



V_I = Input Voltage at AIN
V_S = External Driving Source Voltage
R_S = Source Resistance
r_i = Input Resistance
C_i = Input Capacitance
V_C = Capacitance Charging Voltage

† Driving source requirements:
- Noise and distortion for the source must be equivalent to the resolution of the converter.
- R_S must be real at the input frequency.

Figure 18. Equivalent Input Circuit Including the Driving Source