SN65555, SN65556, SN75555, SN75556
ELECTROLUMINESCENT COLUMN DRIVERS

SLDS031A – APRIL 1985 – REVISED APRIL 1993

- **Each Device Drives 32 Electrodes**
- **90-V Output Voltage Swing Capability Using Ramped Supply**
- **15-mA Output Source and Sink Current Capability**
- **High-Speed Serially-Shifted Data Input**
- **Totem-Pole Outputs**
- **Latches on All Driver Outputs**

description

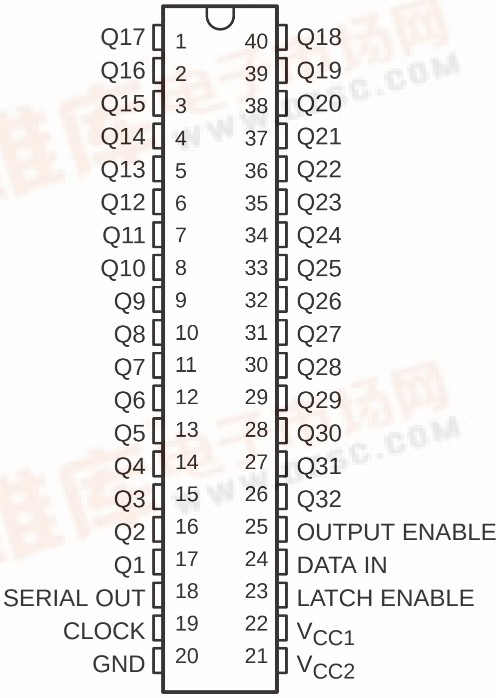
The SN65555, SN75555, SN65556, and SN75556 are monolithic BIDFET[†] integrated circuits designed to drive the column electrodes of an electroluminescent display. The SN65556 and SN75556 output sequence is reversed from the SN65555 and SN75555 for ease in printed-circuit-board layout.

The devices consist of a 32-bit shift register, 32 latches, and 32 output AND gates. Serial data is entered into the shift register on the low-to-high transition of CLOCK. When high, LATCH ENABLE transfers the shift register contents to the outputs of the 32 latches. When OUTPUT ENABLE is high, all Q outputs are enabled. Data must be loaded into the latches and OUTPUT ENABLE must be high before supply voltage V_{CC2} is ramped up.

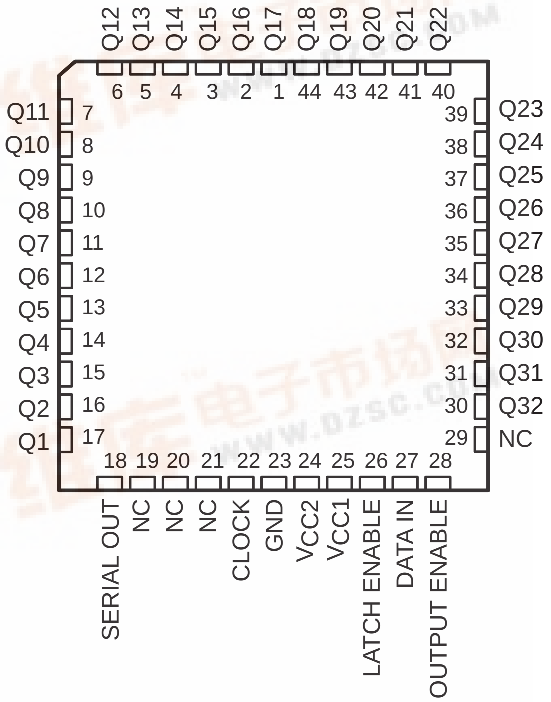
Serial data output from the shift register can be used to cascade shift registers. This output is not affected by LATCH ENABLE or OUTPUT ENABLE.

The SN65555 and SN65556 are characterized for operation from –40°C to 85°C. The SN75555 and SN75556 are characterized for operation from 0°C to 70°C.

SN75555 . . . N PACKAGE
(TOP VIEW)



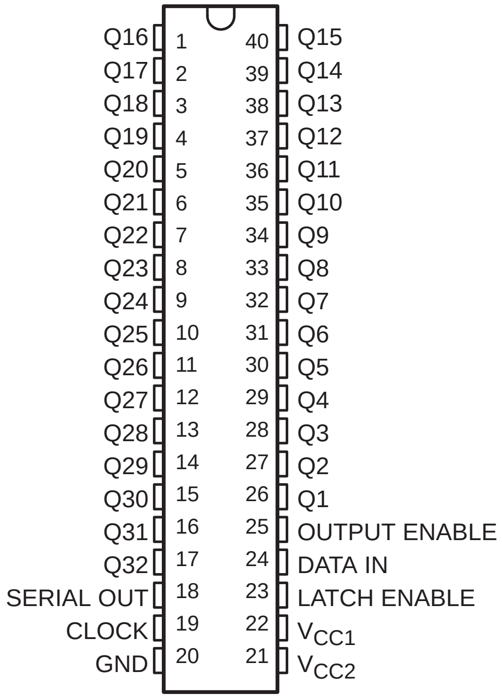
SN65555, SN75555 . . . FN PACKAGE
(TOP VIEW)



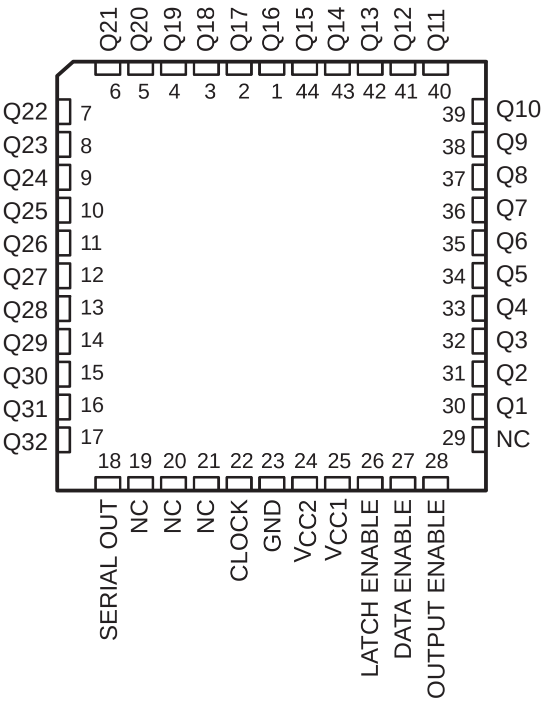
NC – No internal connection

[†] BIDFET – Bipolar, double-diffused, N-channel and P-channel MOS transistors on same chip. This is a patented process.

SN65556, SN75556
N PACKAGE
(TOP VIEW)



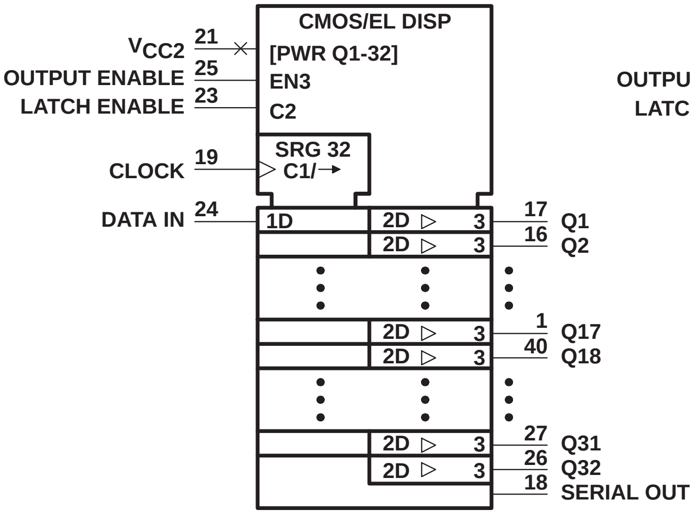
SN65556, SN75556
FN PACKAGE
(TOP VIEW)



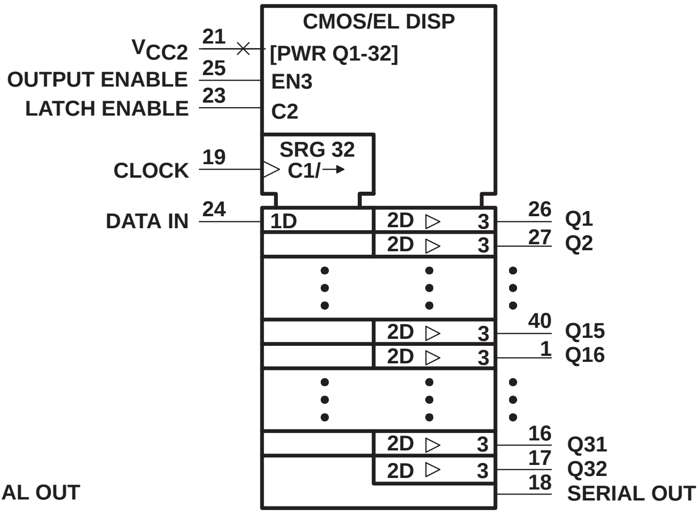
NC – No internal connection

logic symbols[†]

SN65555, SN75555

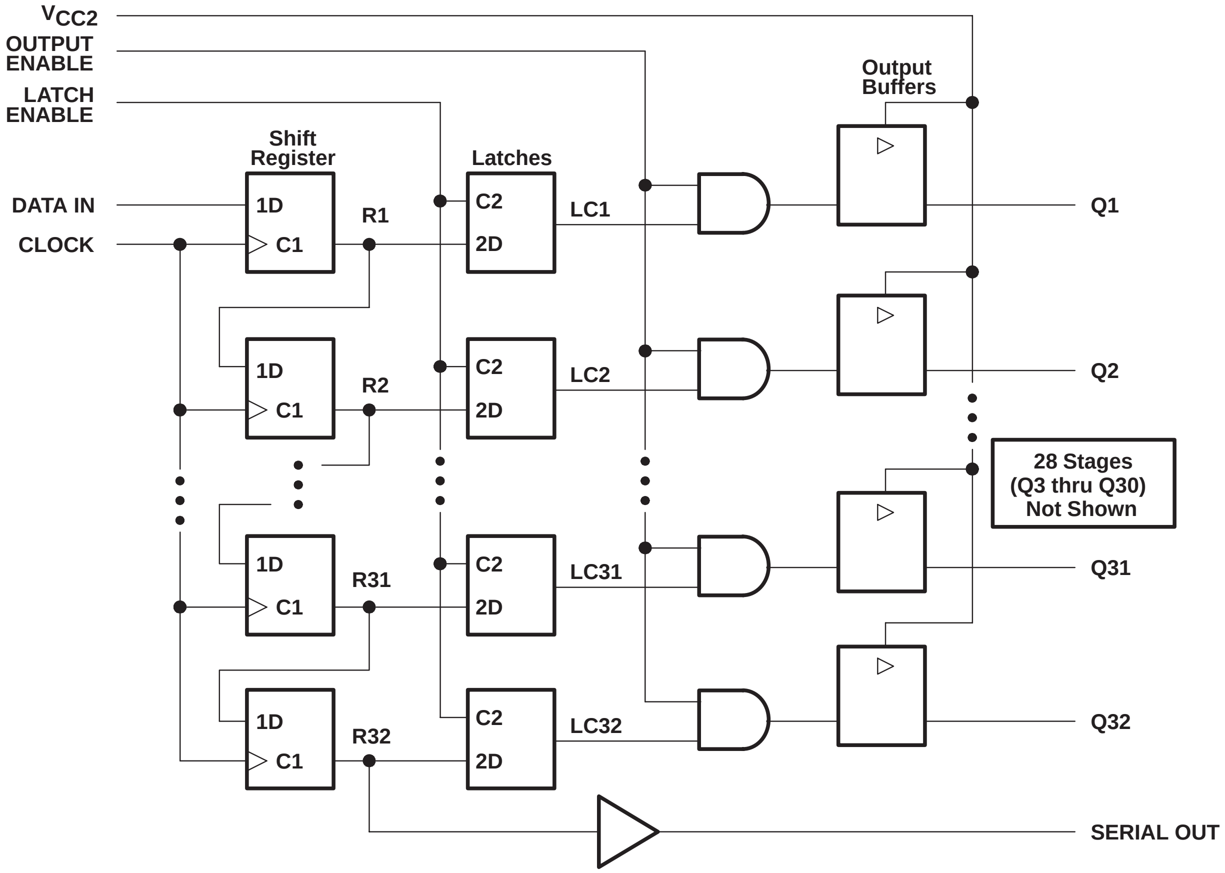


SN65556, SN75556



[†] These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for N packages.

logic diagram (positive logic)



FUNCTION TABLE

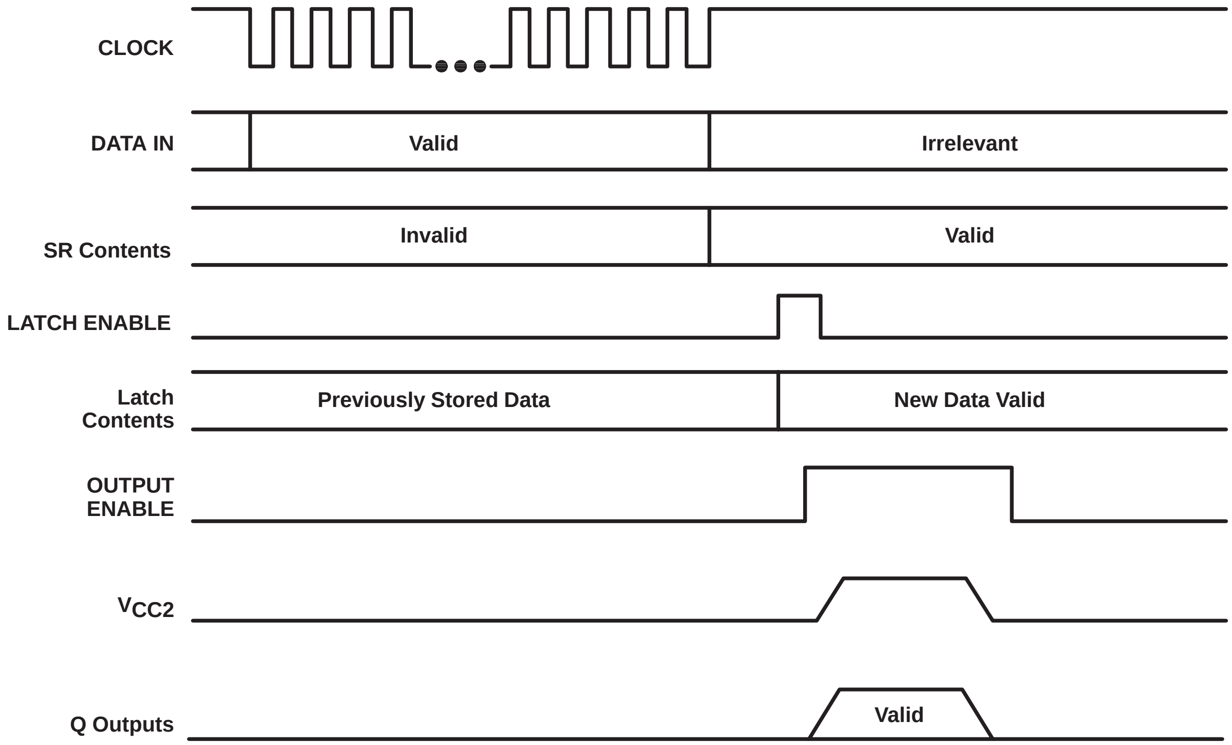
FUNCTION	CONTROL INPUTS			SHIFT REGISTER R1 THRU R32	LATCHES LC1 THRU LC32	OUTPUTS	
	CLOCK	LATCH ENABLE	OUTPUT ENABLE			SERIAL	Q1 THRU Q32
Load	↑ No↑	X X	X X	Load and shift† No change	Determined by LATCH ENABLE‡	R32 R32	Determined by OUTPUT ENABLE
Latch	X X	L H	X X	As determined above	Stored data New data	R32	Determined by OUTPUT ENABLE
Output Enable	X X	X X	L H	As determined above	Determined by LATCH ENABLE‡	R32 R32	All L LC1 thru LC21, respectively

H = high level, L = low level, X = irrelevant, ↑ = low-to-high-level transition.

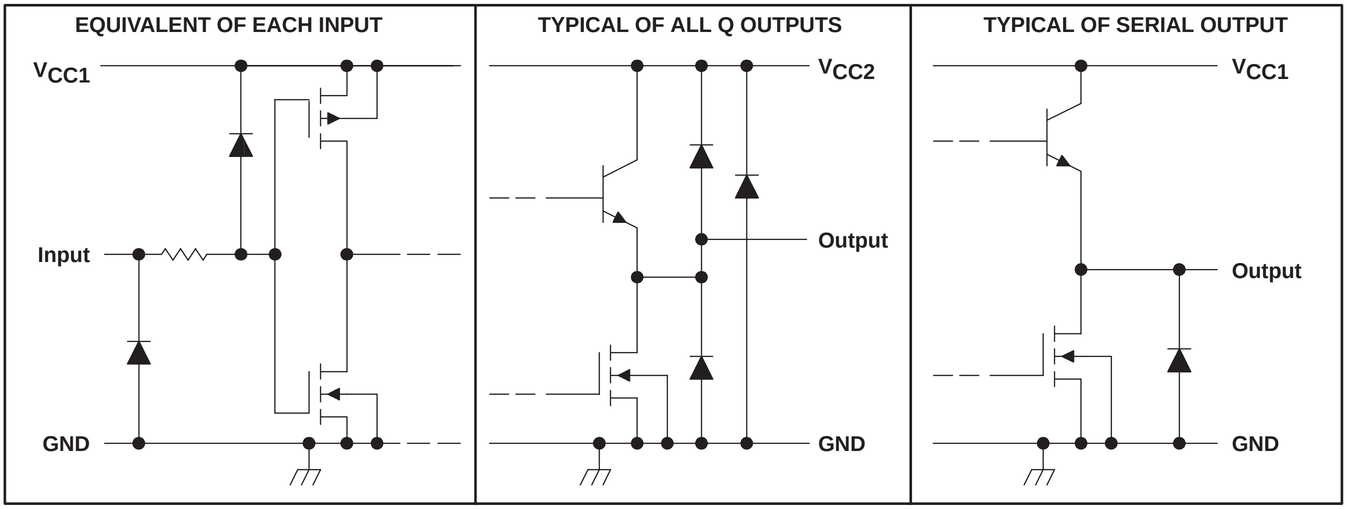
† R32 and the serial output take on the state of R31, R31 takes on the state of R30,. . .R2 takes on the state of R1, and R1 takes on the state of the data input.

‡ New data enter the latches while LATCH ENABLE is high. These data are stored while LATCH ENABLE is low.

typical operating sequence



schematic of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC1} (see Note 1)		18 V
Supply voltage, V_{CC2} (see Note 2)		90 V
Input voltage, V_I		V_{CC1} + 0.3 V
Ground current		700 mA
Continuous total power dissipation		See Dissipation Rating Table
Operating free-air temperature range, T_A:	SN65555, SN65556	– 40°C to 85°C
	SN75555, SN75556	0°C to 70°C
Storage temperature range, T_{stg}		–65°C to 150°C
Case temperature for 10 seconds: FN package		260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N package		260°C

NOTES: 1. Voltage values are with respect to network GND.
2. These devices have been designed to be used in applications in which the high-voltage supply, V_{CC2}, is switched to GND before changing the state of the outputs.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
FN	1700 mW	13.6 mW/°C	1088 mW	884 mW
N	1250 mW	10.0 mW/°C	800 mW	650 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC1}		10.8	12	15	V
Supply voltage, V_{CC2}		0		80	V
High-level input voltage, V_{IH} (see Figure 1)	V_{CC1} = 10.8 V	8.1		11.1	V
	V_{CC1} = 15 V	11.25		15.3	
Low-level input voltage, V_{IL} (see Figure 1)	V_{CC1} = 10.8 V	–0.3†		2.7	V
	V_{CC1} = 15 V	–0.3†		3.75	
High-level output current, I_{OH}				–15	mA
Low-level output current, I_{OL}				15	mA
Output clamp current, I_{OK}				20	mA
Clock frequency, f_{clock}		0		6.25	MHz
Pulse duration, CLOCK high or low, $t_{w(CLK)}$ (see Figure 2)		80			ns
Pulse duration, LATCH ENABLE, $t_{w(LE)}$		80			ns
Setup time, t_{su}	DATA IN before CLOCK ↑ (see Figure 2)	20			ns
	OUTPUT ENABLE before V_{CC2}↑ (see Figure 4)	500			
Hold time, t_h	DATA IN after CLOCK ↑ (see Figure 2)	80			ns
	OUTPUT ENABLE after V_{CC2}↑ (see Figure 4)	100			
Rate of rise for V_{CC2}, dv/dt				80	V/µs
Operating free-air temperature, T_A	SN65555, SN65556	–40		85	°C
	SN75555, SN75556	0		85	

† The algebraic convention, in which the least positive (most negative) value is designated as minimum, is used in this data sheet for logic voltage levels.

electrical characteristics over recommended operating free-air temperature range, V_{CC1} = 12 V, V_{CC2} = 80 V

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level output voltage	Q outputs	$I_O = -15$ mA	77		V
		SERIAL OUT	$I_O = -100$ µA	10.5		
V_{OL}	Low-level output voltage	Q outputs	I_{OL} = 15 mA		8	V
		SERIAL OUT	I_{OL} = 100 µA		1	
I_{IH}	High-level input current		V_I = 12 V		1	µA
I_{IL}	Low-level input current		V_I = 0		–1	µA
I_{CC1}	Supply current from V_{CC1}				2	mA
I_{CC2}	Supply current from V_{CC2}				5	mA

switching characteristics, V_{CC1} = 12 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{PHL}	Propagation delay time, high-to-low-level, SERIAL OUT from CLOCK	C_L = 20 pF to GND, V_{CC2} = 0, See Figure 3		140	ns
t_{PLH}	Propagation delay time, low-to-high level, SERIAL OUT from CLOCK			140	ns
t_d	Delay time, V_{CC2} to Q outputs	dv/dt = 80 V/µs, See Figure 4		100	ns

RECOMMENDED OPERATING CONDITIONS

INPUT VOLTAGE LOGIC-LEVEL LIMITS
vs
SUPPLY VOLTAGE V_{CC1}

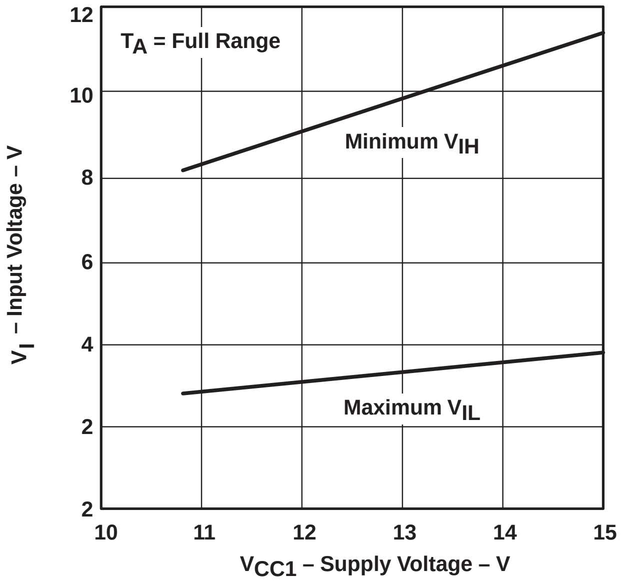


Figure 1

PARAMETER MEASUREMENT INFORMATION

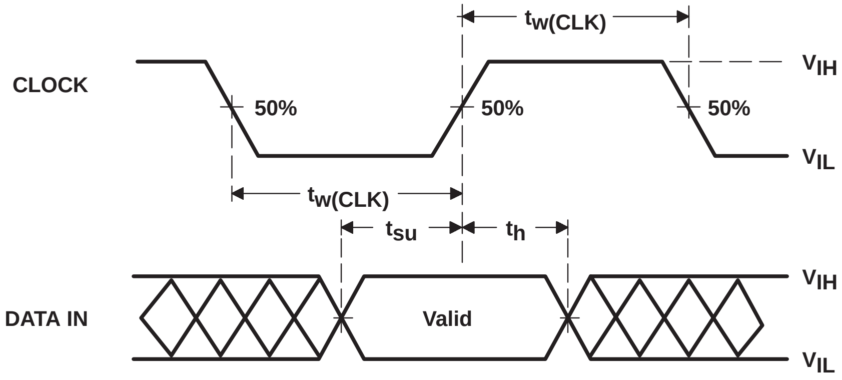


Figure 2. Input Timing Voltage Waveforms

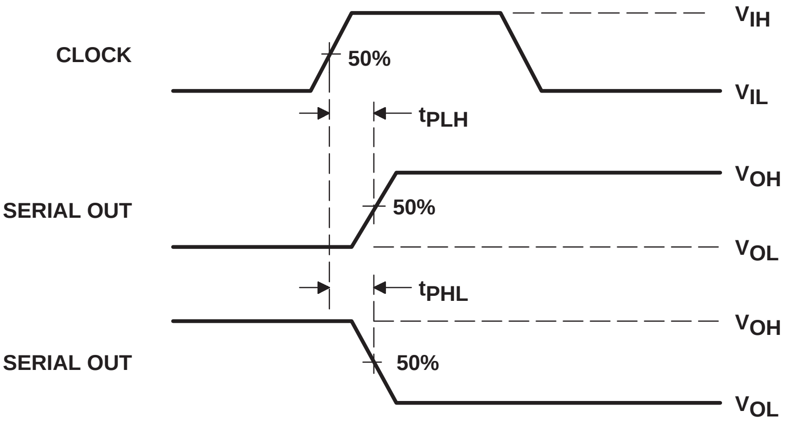


Figure 3. Voltage Waveforms for Propagation Delay Time, CLOCK to SERIAL OUT

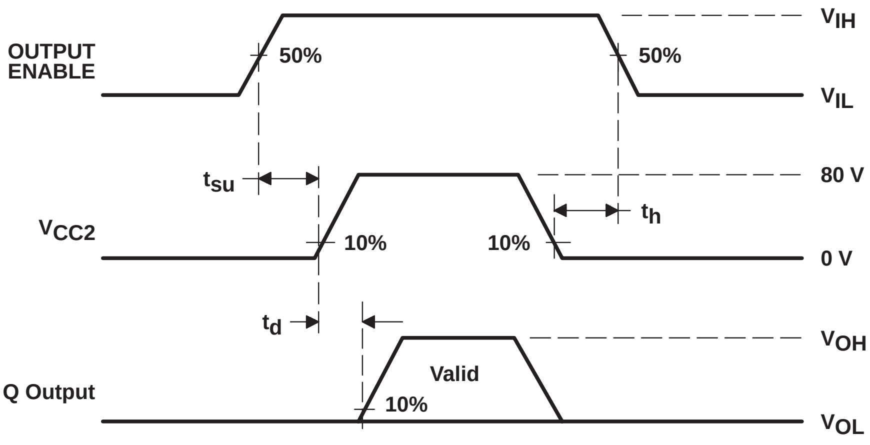


Figure 4. Voltage Waveforms for Delay Times, V_{CC2} to Q Outputs

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