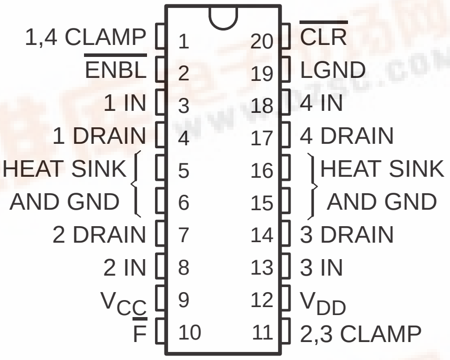
# TPIC2406
# INTELLIGENT-POWER QUAD MOSFET LATCH

SLIS012 – D3378, FEBRUARY 1990

- **Output Voltage up to 60 V**
- **Four Output Channels of 700-mA Nominal Current Per Channel**
- **Pulsed Current . . . 3 A Per Channel**
- **Low $r_{DS(on)}$ . . . 0.5 Ω Typ**
- **Avalanche Energy . . . 50 mJ**
- **Thermal Shutdown Protection With Fault (Overtemperature) Output**
- **NE Package Designed for Heat Sinking**
- **Integral Output Clamp Diodes**
- **Input Transparent Latches for Data Storage**
- **Asynchronous Clear to Turn off All Outputs**
- **Output Parallel Capability for Increased Current Drive up to 12-A Total Pulsed Load Current**

**NE PACKAGE**
**(TOP VIEW)**



**FUNCTION TABLE**
**(each channel)**

| FUNCTION | INPUTS | | | OUTPUT | FAULT |
|---|---|---|---|---|---|
| | $\overline{\text{ENBL}}$ | $\overline{\text{CLR}}$ | IN | Y | $\overline{\text{F}}$ |
| Normal Operation | X | L | X | H | H |
| | L | H | L | H | H |
| | L | H | H | L | H |
| | H | H | X | $Q_0$ | H |
| Thermal Shutdown | X | X | X | H | L |

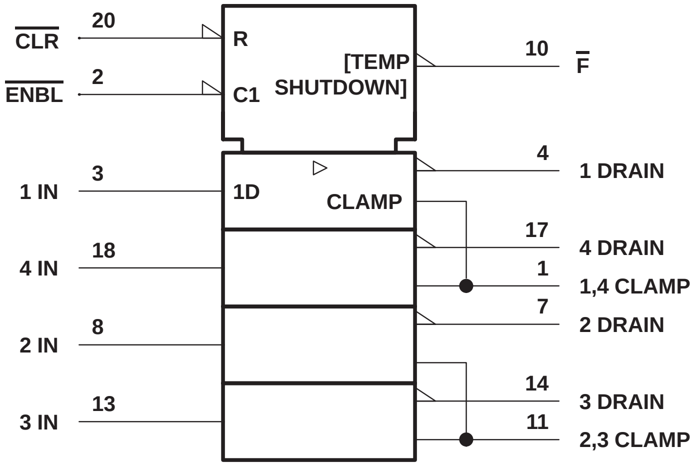
H = high-level, L = low-level, X = irrelevant

## description

The TPIC2406 is a monolithic, high-voltage, high-current, quadruple power driver designed for use in systems that require high load power. The device contains built-in high-speed output clamp diodes for inductive transient protection. Power driver applications include lamps, relays, solenoids, and dc stepping motors.

The device features four inverting open-drain outputs, each controlled by an input storage latch with common clear and enable controls. All inputs accept standard TTL- and CMOS-logic levels. The $\overline{\text{CLR}}$ function is asynchronous and turns all four outputs off regardless of data inputs. Taking $\overline{\text{ENBL}}$ low puts the input latch into a transparent mode, allowing the data inputs to affect the output. In this state, all four outputs are held off while $\overline{\text{CLR}}$ is low, but return to the stages on the data inputs when $\overline{\text{CLR}}$ goes high. When $\overline{\text{ENBL}}$ is taken high, the latch is put into a storage mode and the last state of the data inputs is held in the latches. If $\overline{\text{CLR}}$ is taken low, the data in the latches is cleared and all outputs are turned off. If $\overline{\text{CLR}}$ is taken high again, $\overline{\text{ENBL}}$ must be cycled low to read new data into the latch.

## logic symbol†



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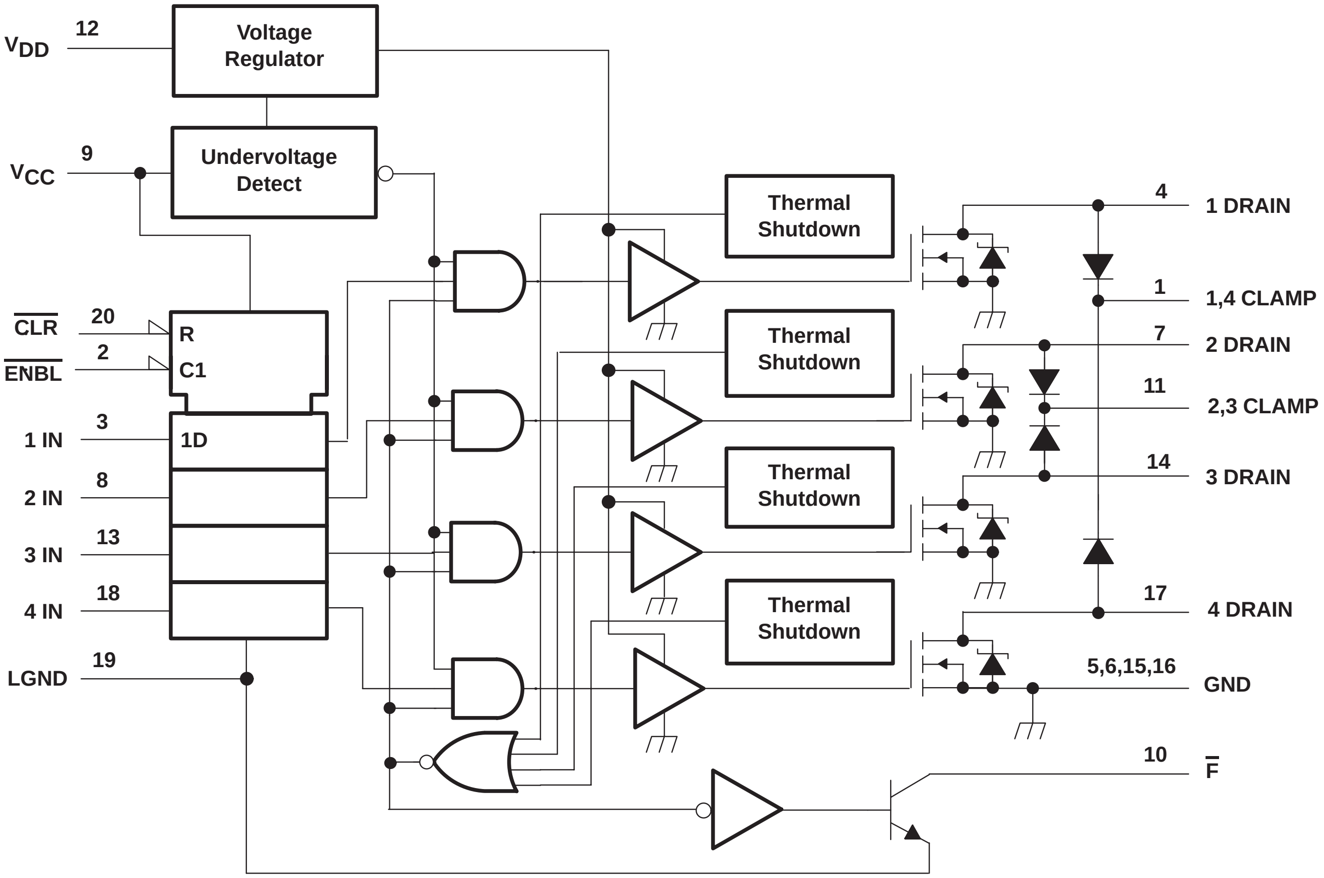
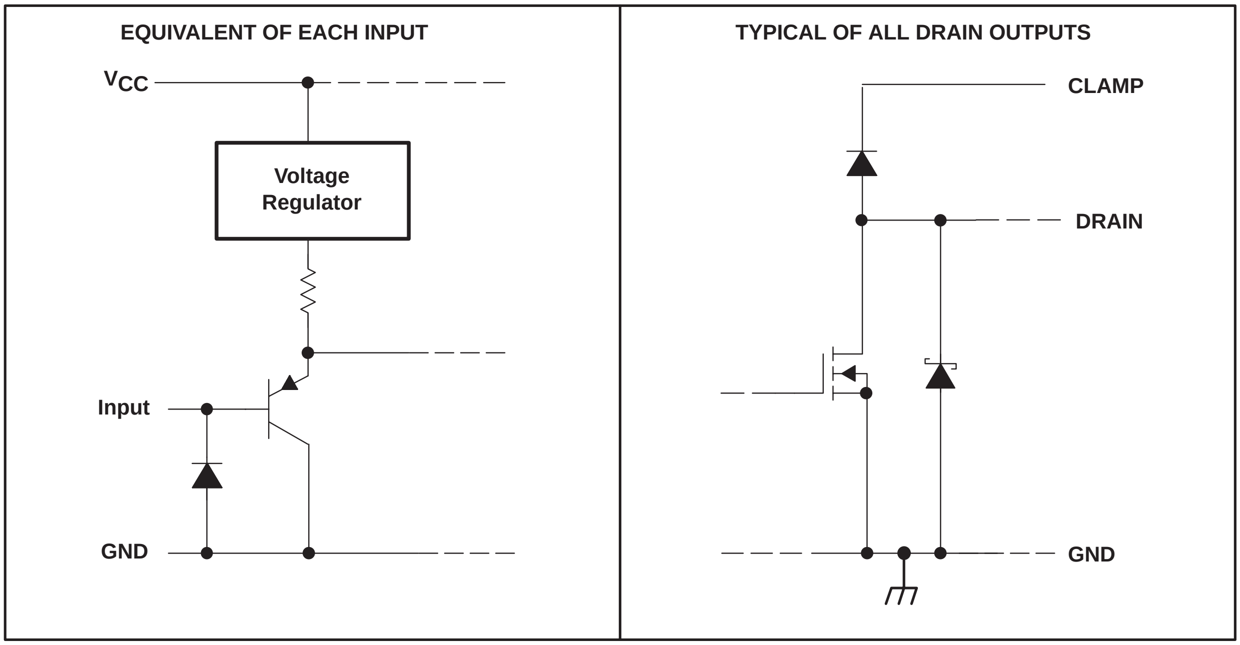
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)



## schematics of inputs and outputs



## absolute maximum ratings over –40°C to 125°C case temperature range (unless otherwise noted)

| | |
|---|---|
| Logic supply voltage, $V_{CC}$ (see Note 1) | 7 V |
| Power MOSFET driver supply voltage, $V_{DD}$ | 60 V |
| Logic input voltage, $V_I$ | 7 V |
| Power MOSFET drain-source voltage, $V_{DS}$ | 60 V |
| Output voltage at $\overline{F}$, $V_O$ | 7 V |
| Clamp-diode voltage | 60 V |
| Continuous source-drain diode anode current | 1.25 A |
| Pulsed source-drain diode anode current | 6 A |
| Pulsed drain current, each output, all outputs on, $I_{D1} = I_{D2} = I_{D3} = I_{D4}$, $T_A = 25°C$ (see Note 2 and Figures 5 through 8) | 3 A |
| Continuous drain current, each output, all outputs on, $I_{D1} = I_{D2} = I_{D3} = I_{D4}$, $T_A = 25°C$ | 770 mA |
| Peak drain current, single output, $I_{DM}$, $T_A = 25°C$ (see Note 3) | 12.5 A |
| Single-pulse avalanche energy, $E_{AS}$ | 50 mJ |
| Continuous total dissipation at or below 25°C free-air temperature (see Note 4) | 2.5 W |
| Continuous total dissipation at or below 100°C case temperature (see Note 4) | 6 W |
| Operating junction temperature range, $T_J$ | –40°C to 150°C |
| Storage temperature range | –40°C to 150°C |
| Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds | 260°C |

NOTES: 1. All voltage values are with respect to the five ground (GND and LGND) terminals connected together.
2. Pulse duration = 10 ms, duty cycle = 6%.
3. Pulse duration ≤ 100 µs, duty cycle ≤ 2%.
4. For operation above 25°C free-air temperature, derate linearly at the rate of 20 mW/°C. For operation above 100°C case temperature, derate linearly at the rate of 120 mW/°C. To avoid exceeding the design maximum junction temperature, these ratings should not be exceeded. Due to variations in individual devices, electrical characteristics, and thermal resistance, the built-in thermal overload protection can be activated at power levels slightly above or below the rated dissipation.

## recommended operating conditions

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Logic supply voltage, $V_{CC}$ | | 4.5 | | 5.5 | V |
| Output supply voltage, $V_{DD}$ | | 10 | | 35 | V |
| High-level input voltage, $V_{IH}$ | | 2 | | | V |
| Low-level input voltage, $V_{IL}$ | | | | 0.6 | V |
| Setup time, data before $\overline{\text{ENBL}}$ ↑, $t_{su}$ (see Figure 1) | | 100 | | | ns |
| Hold time, data after $\overline{\text{ENBL}}$ ↑, $t_h$ (see Figure 1) | | 100 | | | ns |
| Pulse duration, $t_w$ (see Figure 1) | $\overline{\text{ENBL}}$ low | 300 | | | ns |
| | $\overline{\text{CLR}}$ low | | | | |
| Operating case temperature, $T_C$ | | –40 | | 125 | °C |

## electrical characteristics, $V_{CC}$ = 5 V, $V_{DD}$ = 14 V, $T_C$ = 25°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS† | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{(BR)DSX}$ | Drain-source breakdown voltage | $I_D$ = 1 mA | 60 | | | V |
| $V_{F(K)}$ | Clamp-diode forward voltage | $I_F$ = 1.25 A, See Notes 5 and 6 | | | 1.6 | V |
| $V_{SD}$ | Source-drain diode forward voltage | $I_S$ = 1.25 A, See Notes 5 and 6 | | | 1.5 | V |
| $V_{IK}$ | Input clamp voltage | $V_{CC}$ = MIN, $I_I$ = ~ 12 mA | | | –1.5 | V |
| $V_{OL}$ | Low-level output voltage at $\overline{\text{F}}$ | $I_{OL}$ = 4 mA | | 0.4 | | V |
| $I_{IH}$ | High-level input current | $V_{CC}$ = 5.5 V, $V_I$ = 2.7 V | | | 20 | µA |
| $I_{IL}$ | Low-level input current | $V_{CC}$ = 5.5 V, $V_I$ = 0.4 V | | | 0.1 | mA |
| $I_{CC}$ | Logic supply current | $I_O$ = 0, All outputs off | | | 10 | mA |
| $I_N$ | Nominal current | $V_{DS(on)}$ = 0.5 V, $I_N$ = $I_D$, $T_C$ = 85°C, See Notes 5, 6, and 7 | | 700 | | mA |
| $I_{DD}$ | Output supply current | $I_O$ = 0, All outputs off | | | 6 | mA |
| $I_{R(K)}$ | Clamp-diode reverse current | $V_{DS}$ = 55 V, $V_O$ = 0 | | | 1 | µA |
| | | $V_{DS}$ = 55 V, $V_O$ = 0, $T_C$ = 125°C | | | 10 | |
| $I_{DSX}$ | Off-state drain current | $V_R$ = 55 V | | | 1 | µA |
| | | $V_R$ = 55 V, $T_C$ = 125°C | | | 10 | |
| $I_{O(F)}$ | High-level fault leakage current | $V_{OH}$ = 5.5 V | | | 1 | µA |
| $r_{DS(on)}$ | Static drain-source on-state resistance | $I_D$ = 1.25 A, See Notes 5 and 6 | | 0.5 | 0.6 | Ω |
| | | $I_D$ = 1.25 A, $T_C$ = 125°C | | 0.8 | 1 | |
| | | $I_D$ = 3 A | | 0.55 | 0.65 | |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

NOTES: 5. Technique should limit $T_J$ – $T_C$ to 10°C maximum.

6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

7. Nominal current is defined for a consistent comparison between devices from different sources. It is the current that produces a voltage drop of 0.5 V at 85°C case temperature.

## switching characteristics, $V_{CC}$ = 5 V, $V_{DD}$ = 24 V, $T_C$ = 25°C

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation delay time, low-to-high-level drain output from clock | $C_L$ = 30 pF, | See Figure 1 | | 450 | | ns |
| $t_{PHL}$ | Propagation delay time, high-to-low-level drain output from clock | | | | 550 | | ns |
| $t_{TLH}$ | Transition time, low-to-high-level of source-drain output | | | | 35 | | ns |
| $t_{THL}$ | Transition time, high-to-low-level of source-drain output | | | | 30 | | ns |
| $t_{PLH}$ | Propagation delay time, low-to-high-level drain output from input | $C_L$ = 30 pF,<br>$I_D = I_N$ = 700 mA | See Figure 2, | | 380 | | ns |
| $t_{PHL}$ | Propagation delay time, high-to-low-level drain output from input | | | | 380 | | ns |
| $t_r$ | Rise time, low-to-high-level of source-drain output | | | | 35 | | ns |
| $t_f$ | Fall time, high-to-low-level of source-drain output | | | | 70 | | ns |
| $t_a$ | Reverse-recovery-current rise time | $I_F$ = 3 A,<br>See Notes 5 and 6, | di/dt = 100 A/μs,<br>See Figure 3 | | 45 | | ns |

NOTES: 5. Technique should limit $T_J - T_C$ to 10°C maximum.

6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

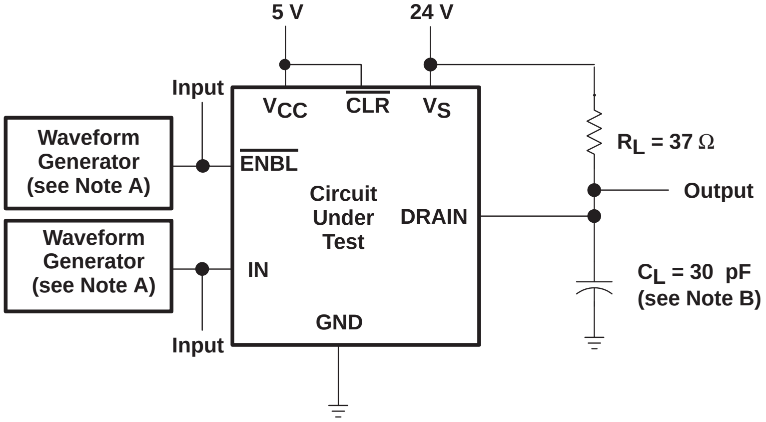
## thermal resistance

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $R_{\theta JC}$ | Junction-to-case thermal resistance | All four outputs with equal power | | | 8.33 | °C/W |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | | | | 50 | |

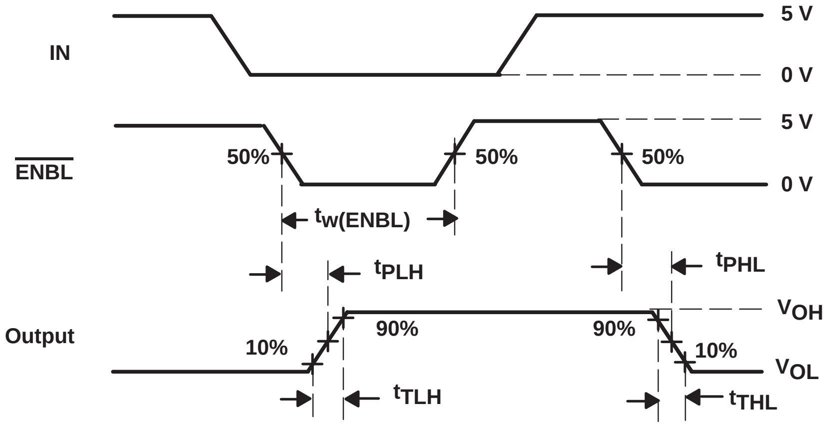
## operating characteristics over –40°C to 125°C case temperature range

| PARAMETER | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|
| Undervoltage shutdown | 3 | | 4.5 | V |
| Thermal shutdown temperature | | 155 | | °C |
| Thermal shutdown hysteresis | | 15 | | °C |

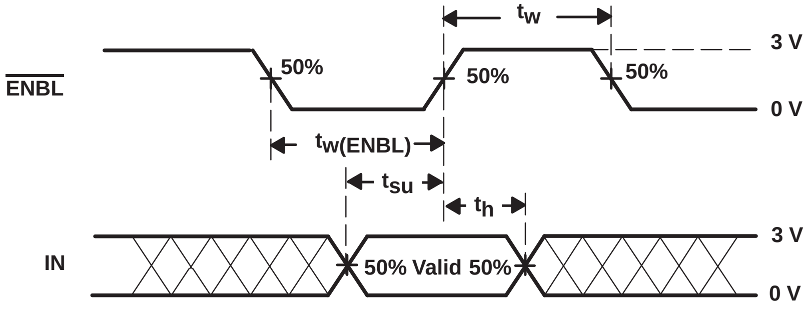
## PARAMETER MEASUREMENT INFORMATION



(a) TEST CIRCUIT



(b) SWITCHING TIMES FROM ENABLE INPUT

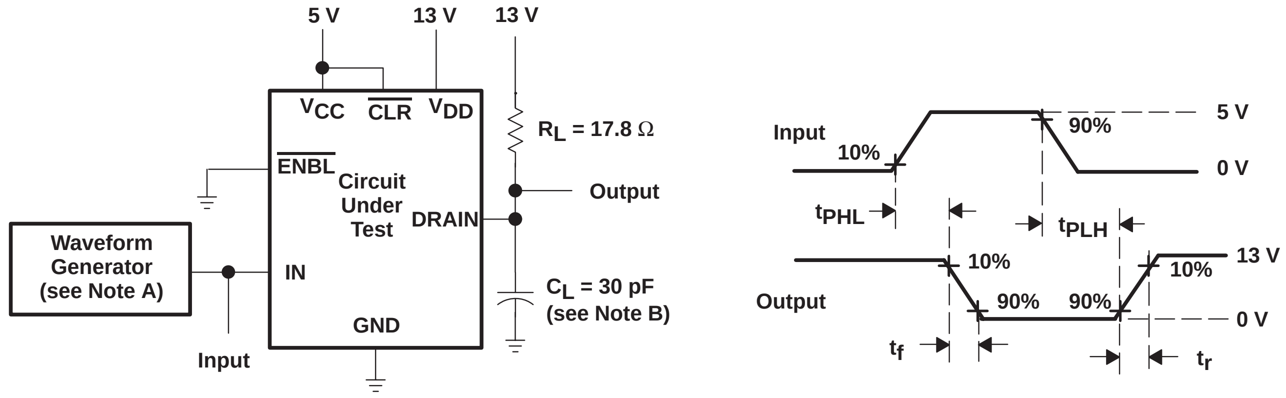


(c) INPUT SETUP AND HOLD WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, $t_W = 300$ ns, PRR = 5 kHz, $Z_O = 50\ \Omega$.
B. $C_L$ includes probe and jig capacitance.

Figure 1. Test Circuit and Voltage Waveforms

## PARAMETER MEASUREMENT INFORMATION

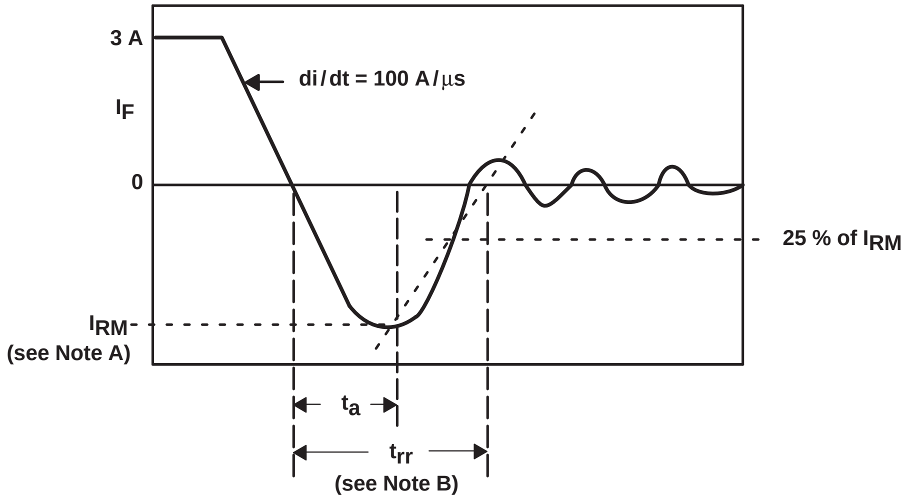


(a) TEST CIRCUIT

(b) VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: $t_r \le 10$ ns, $t_f \le 10$ ns, $t_w = 5$ ms, PRR = 5 kHz, $Z_O = 50\ \Omega$.
B. $C_L$ includes probe and jig capacitance.

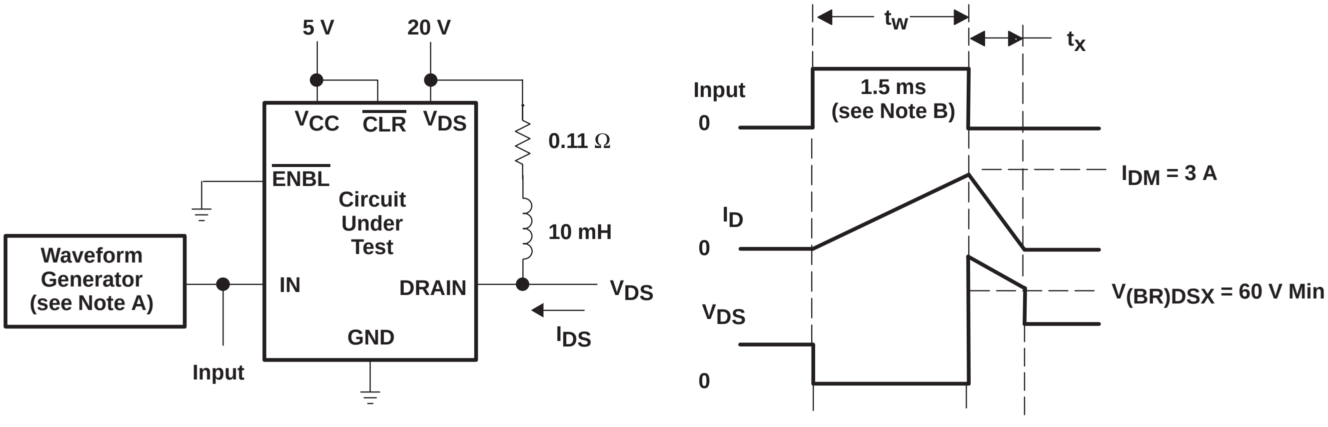
Figure 2. Test Circuit and Voltage Waveforms



NOTES: A. $I_{RM}$ = maximum recovery current.
B. $t_{rr}$ = reverse recovery time.

Figure 3. Reverse-Recovery-Current Waveforms of Source-Drain Diode

## PARAMETER MEASUREMENT INFORMATION



(a) TEST CIRCUIT

(b) VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, $t_w = 1$ ms, PRR = 5 kHz, $Z_O = 50\ \Omega$.

B. Input pulse duration ($t_w$) is increased until peak current $I_{DM} = 3$ A.

Energy test level is defined as $E_{AS} = \dfrac{I_{DM} \times V_{(BR)DSX} \times t_x}{2} = 50\ \text{mJ min.}$

Figure 4. Single-Pulse Avalanche Energy Test Circuit and Waveforms

## MAXIMUM RATINGS

MAXIMUM DRAIN CURRENT
vs
DUTY CYCLE

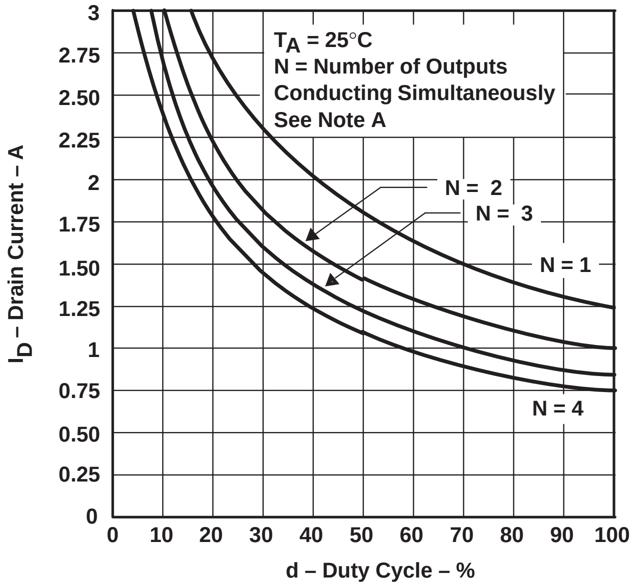


Figure 5

MAXIMUM DRAIN CURRENT
vs
DUTY CYCLE

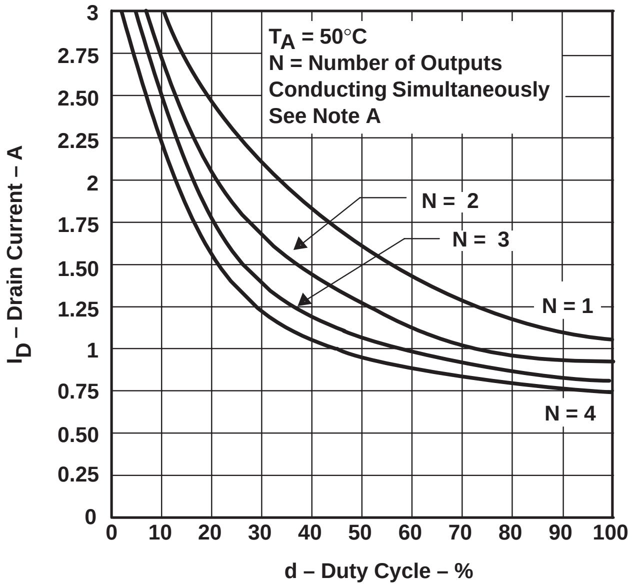


Figure 6

MAXIMUM DRAIN CURRENT
vs
DUTY CYCLE

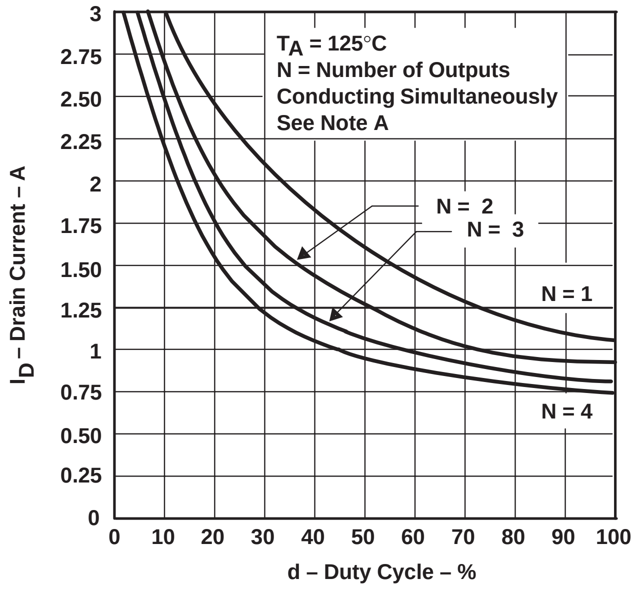


Figure 7

MAXIMUM DRAIN CURRENT
vs
PULSE DURATION

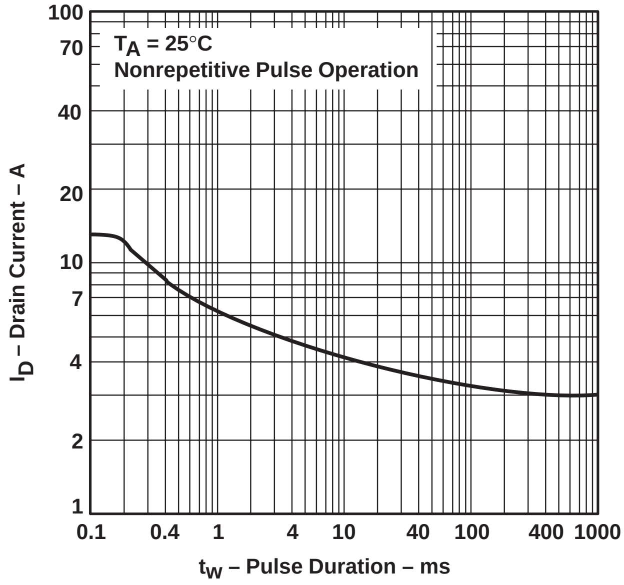
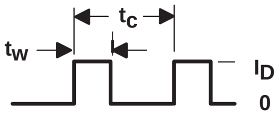


Figure 8

NOTE A: For Figures 5, 6, and 7, d = $\frac{t_W}{t_C} = \frac{10\ \text{ms}}{t_C}$, where $t_W$ and $t_C$ are defined by the following:



## MAXIMUM RATINGS

### MAXIMUM CONTINUOUS DRAIN CURRENT vs FREE-AIR TEMPERATURE

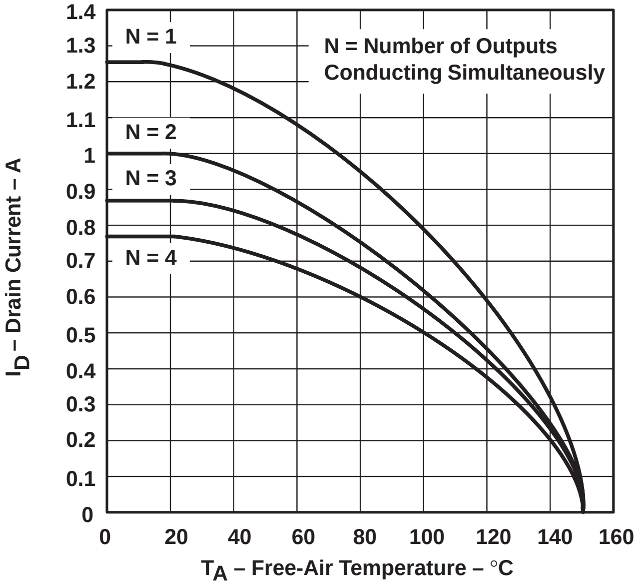
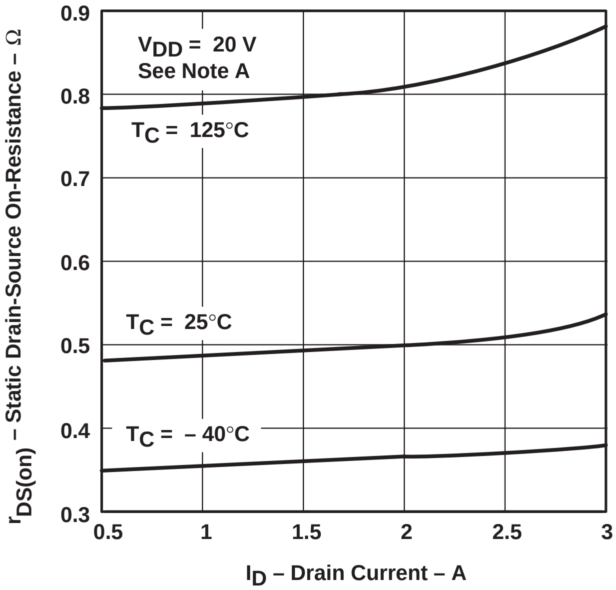


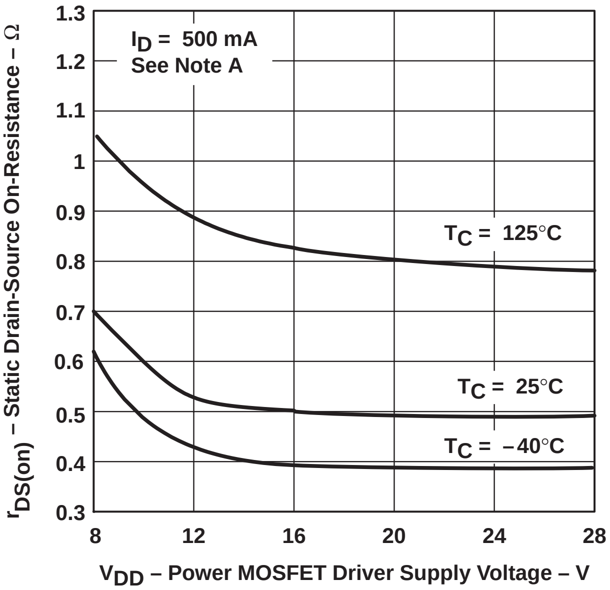
**Figure 9**

## TYPICAL CHARACTERISTICS

### STATIC DRAIN-SOURCE ON-RESISTANCE vs DRAIN CURRENT



### STATIC DRAIN-SOURCE ON-RESISTANCE vs POWER MOSFET DRIVER SUPPLY VOLTAGE



NOTE A: Technique should limit $T_J – T_C$ to 10°C maximum.

**Figure 10**

**Figure 11**

## THERMAL INFORMATION

**FREE-AIR TEMPERATURE**
**DISSIPATION DERATING CURVE**

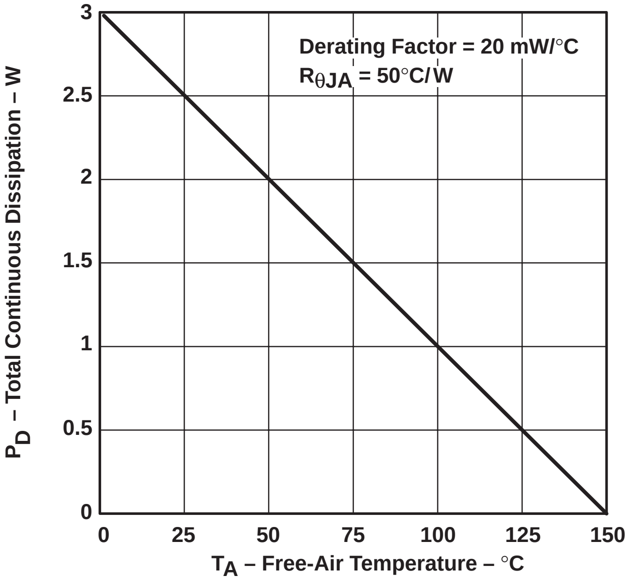


Figure 12

**TRANSIENT THERMAL IMPEDANCE**
**vs**
**ON TIME**

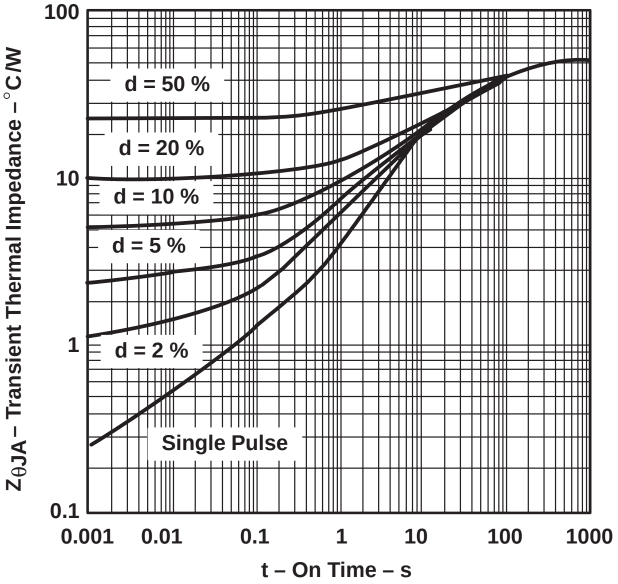


Figure 13

The single-pulse curve in Figure 11 represents measured data. The curves for various pulse durations are based on the following equation:

$$Z_{\theta JA} = \left|\frac{t_w}{t_c}\right| R_{\theta JA} + \left|1 - \frac{t_w}{t_c}\right| Z_{\theta(t_w + t_c)} + Z_{\theta(t_w)} - Z_{\theta(t_c)}$$

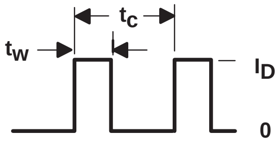
Where:

$Z_{\theta(t_w)}$ = the single-pulse thermal impedance for t = $t_W$ seconds

$Z_{\theta(t_c)}$ = the single-pulse thermal impedance for t = $t_C$ seconds

$Z_{\theta(t_w + t_c)}$ = the single-pulse thermal impedance for t = $t_W + t_C$ seconds

$$d = t_W/t_C$$



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