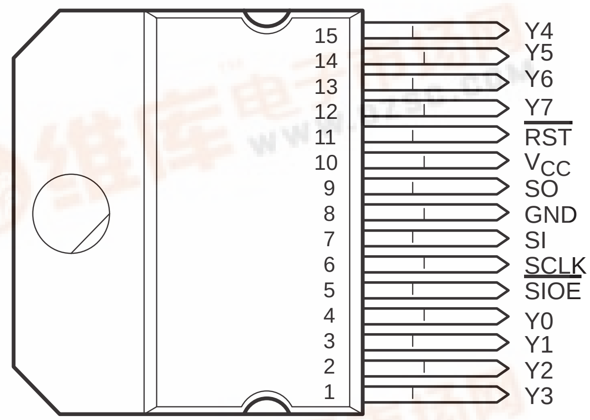
TPIC2802
OCTAL INTELLIGENT-POWER SWITCH WITH SERIAL INPUT

SLIS013 – APRIL 1992

- **8-Bit Serial-In Parallel-Out Driver**
- **1-A Output Current Capability Per Channel or 8-A Total Current**
- **Overcurrent Limiting and Out-of-Saturation Voltage Protection on Driver Outputs**
- **Contains Eight Open-Collector Saturating Sink Outputs With Low On-State Voltage**
- **High-Impedance Inputs With Hysteresis Are Compatible With TTL or CMOS Levels**
- **Exceptionally Low On-State Supply Current 50 mA**
- **Very Low Standby Power 20 mW Typical**
- **Status of Output Drivers May Be Monitored at Serial Output**
- **3-State Serial Output Permits Serial Cascading or Wire-AND Device Connections**
- **45-V Transient Clamping With Inductive Switching on Outputs, 20-mJ Rating Per Driver Output**

KV PACKAGE
(TOP VIEW)



The tab is electrically connected to GND.

description

The TPIC2802 octal intelligent-power switch is a monolithic BIDFET† integrated circuit designed to sink currents up to 1 A at 45 V simultaneously at each of eight driver outputs under serial input data control. Furthermore, use of a Darlington output structure enables an 80% reduction in the on-state supply current compared with earlier designs. Status of the individual driver outputs is available in serial data format. The driver outputs have overcurrent limiting and out-of-saturation voltage protection features. Applications include driving solenoids, relays, dc motors, lamps, and other medium-current or high-voltage loads.

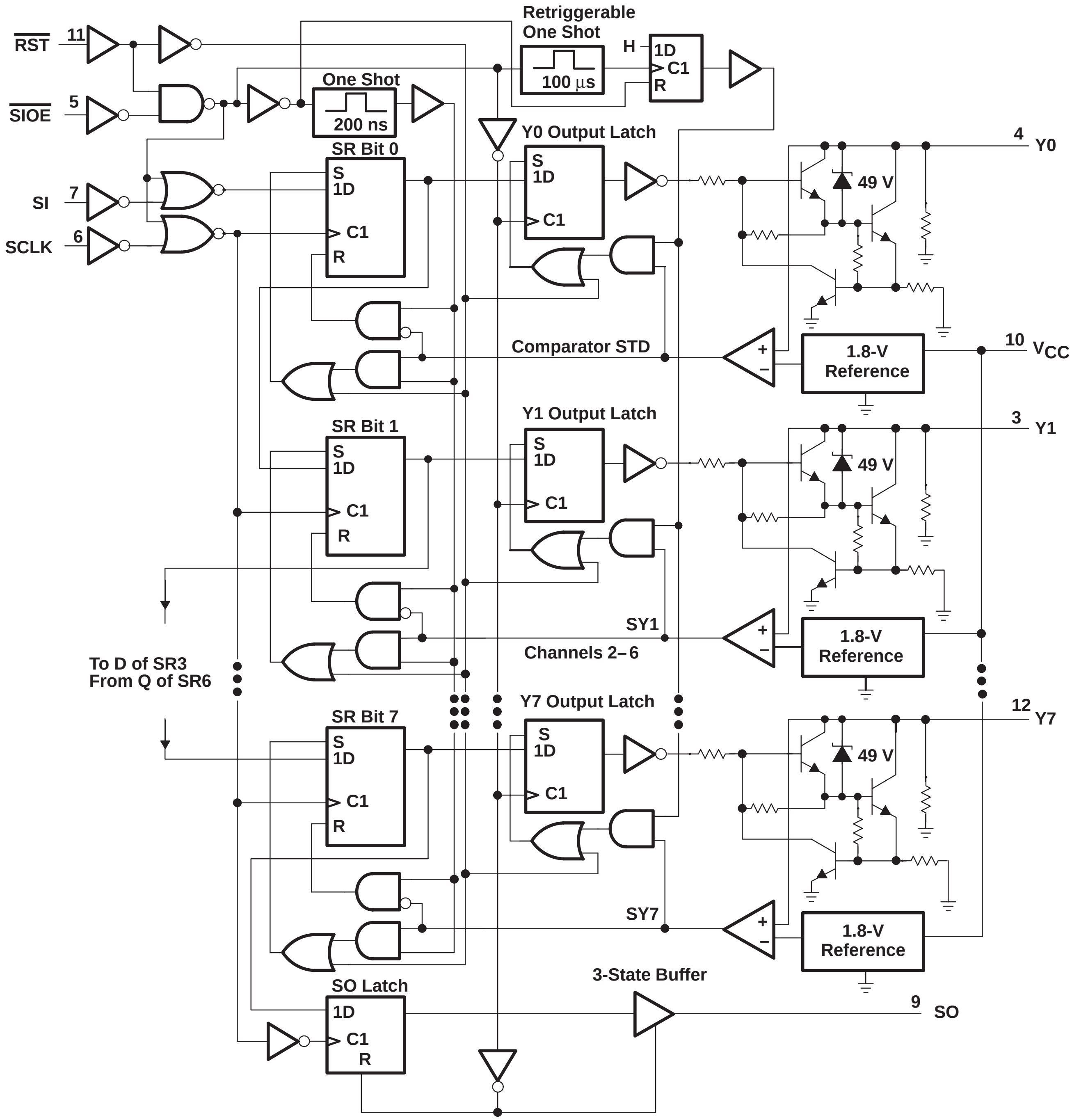
The device contains an 8-bit serial-in, parallel-out shift register that feeds an 8-bit parallel latch, which independently controls each of the eight Y-output drivers.

Data is entered into the device serially via the serial input (SI) and goes directly into the lowest bit (0) of the shift register. Using proper timing signals, the input data is passed to the corresponding output latch and output driver. A logic-high SI bit n turns the corresponding output driver (Y_n)off. A logic-low bit at SI turns the corresponding output driver on. Serial data is transferred into SI on the high-to-low transition of the serial clock (SCLK) input in 8-bit bytes with data for the Y7 output (most significant bit) first and data for Y0 output (least significant bit) last. Both SI and SCLK are active when the serial input-output enable ($\overline{SIOE}$) input is low and are disabled when $\overline{SIOE}$ is high.

Each driver output is monitored by a voltage comparator that compares the Y-output voltage level with an internal out-of-saturation threshold voltage reference level. The logic state of the comparator output is dependent upon whether the Y output is greater or smaller than the reference voltage level. While $\overline{SIOE}$ is held high, an activated driver output is unlatched and turned off when the output voltage exceeds the out-of-saturation threshold voltage level except when the internal unlatch enable is low and disabled. The high-to-low transition of $\overline{SIOE}$ transfers the logic state of the comparator output to the shift register.

† BIDFET – Bipolar, double-diffused, N-channel and P-channel MOS transistors on same chip. This is a patented process.

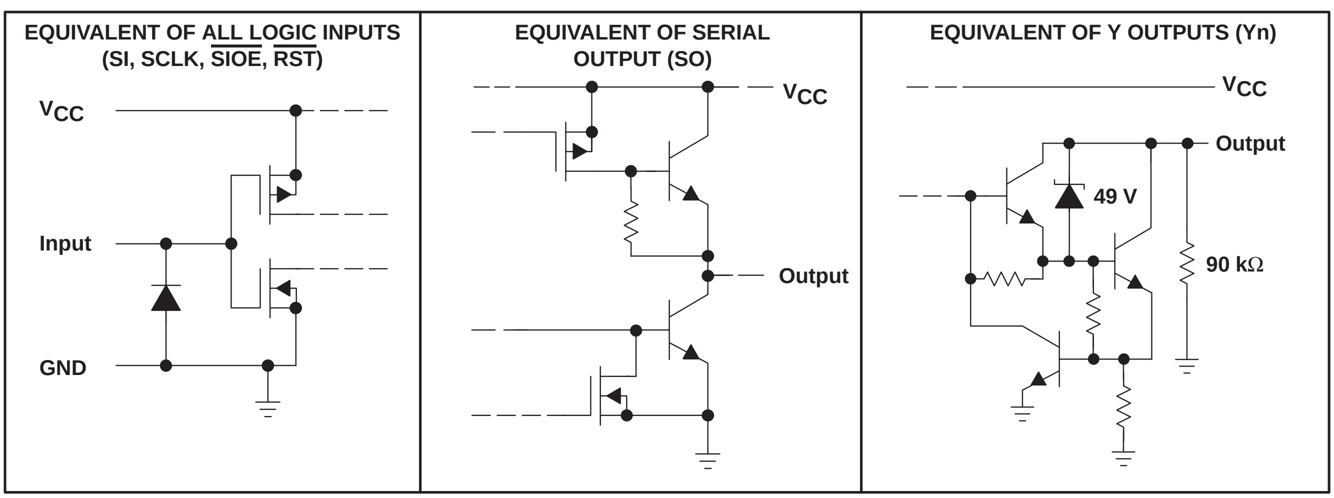
functional block diagram



Terminal Functions

PIN NAME	PIN NO.	I/O	DESCRIPTION
GND	8		Ground. Common return for entire chip. The output current from this terminal is potentially as high as 8 A if all outputs are on. GND is used for both logic and power circuits.
$\overline{RST}$	11	I	Reset. An asynchronous reset is provided for the shift register and the parallel latches. This terminal is active when low and has no internal pullup. When active, it causes the power outputs to turn off. A power-on clear can be implemented using an RC network to V_{CC}.
SCLK	6	I	Serial clock. This terminal clocks the shift register. The serial output (SO) changes state on the rising edge of SCLK and serial input (SI) data is accepted on the falling edge.
SI	7	I	Serial Input. A high on this terminal programs a particular output to be off, and a low turns it on.
$\overline{SIOE}$	5	I	Serial input-output enable. Data is transferred from the shift registers to the power outputs on the rising edge of this signal. The falling edge of this signal parallel loads the output voltage sense bits from the power output stages into the shift register. The output driver SO is enabled when this terminal is low, provided $\overline{RST}$ is high.
SO	9	O	Serial output. This terminal is the serial 3-state output from the shift register and is in a high-impedance state when $\overline{SIOE}$ is high or $\overline{RST}$ is low. A high for a data bit on this terminal indicates that the corresponding power output (Y_n) is high. This means that the output was programmed to be off the last time a byte was input to the device or that the output faulted and was latched off by the output voltage-sense indicator. A low on this output indicates that the corresponding power output (Y_n) is low (on output stage or open-circuit condition).
V_{CC}	10		5-V supply voltage
Y0 Y1 Y2 Y3 Y4 Y5 Y6 Y7	4 3 2 1 15 14 13 12	O	Power outputs. These outputs are provided with current limiting and voltage sense for fault indication and protection. The nominal load current for these outputs is 500 mA, and the current limiting is set to a minimum of 1 A. The active-low outputs also have voltage clamps set at about 45 V for recirculation of inductive load current. Internal 90-kΩ pulldown resistors are provided at each output. These resistors hold the output low during an open-circuit condition.

schematic of inputs and outputs



All resistor and voltage values shown are nominal.

absolute maximum ratings over operating temperature range (unless otherwise noted)

Supply voltage range, V_{CC} (see Note 1) . . . . – 0.3 V to 7 V
Input voltage, V_I . . . . 7 V
Output voltage range, SO . . . . – 0.3 V to 7 V
Input current, I_I . . . . –15 mA
Peak output sink current at Y, I_O repetitive, t_w = 10 ms, duty cycle = 50%,
(see Notes 2 and 3) . . . . internally limited
Continuous output current at Y, I_O (see Note 3) . . . . 1 A
Peak current through GND terminal: Nonrepetitive t_w = 0.2 ms . . . . – 8 A
Repetitive t_w = 10 ms, duty cycle = 50% . . . . – 6 A
Continuous current through GND terminal . . . . – 4.5 A
Single-pulse avalanche energy rating, E_{AS} (see Note 4) . . . . 20 mJ
Avalanche current, $I_{AS(max)}$ (see Note 5) . . . . 1 A
Continuous dissipation at (or below) T_A = 25°C (see Note 6) . . . . 3.575 W
Continuous dissipation at (or below) T_C = 75°C (see Note 6) . . . . 25 W
Operating case or virtual-junction temperature range . . . . – 55°C to 150°C
Storage temperature range, T_{stg} . . . . – 65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . 260°C

NOTES:
1. All voltage values are with respect to network GND.
2. Each Y output is individually current limited with a typical overcurrent limit of about 1.8 A.
3. Multiple Y outputs of this device can conduct rated current simultaneously; however, power dissipation (average) over a short time interval must fall within the continuous dissipation range and the GND terminal current range.
4. V_{CC} = 20 V, starting T_J = 25°C, L = 310 mH, I_{AS} = 0.28 A.
5. V_{CC} = 10 V, starting T_J = 25°C, L = 8 mH, I_{AS} = 1 A (see Figure 6).
6. For operation above 25°C free-air temperature, derate linearly at the rate of 28.6 mW/°C. For operation above 75°C case temperature, derate linearly at the rate of 333 mW/°C. To avoid exceeding the maximum virtual-junction temperature, these ratings must not be exceeded.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level input voltage, V_{IH}	0.75 V_{CC}		5.25	V
Low-level input voltage, V_{IL}	–0.3		0.2 V_{CC}	V
Output voltage, $V_{O(off)}$			45	V
Continuous output current, $I_{O(on)}$			1	A
Operating case temperature, T_C	–40	25	105	°C

electrical characteristics over recommended operating virtual junction temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC}	Supply current	All outputs on, I_O = 0.5 A at all outputs			50	mA
		All outputs off, T_J = 25°C		4	10	

electrical characteristics over recommended operating virtual junction temperature range (unless otherwise noted) (continued)

driver array outputs (Y0 to Y7)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OK}	Output clamp voltage	I_O = 0.5 A,	Output programmed off and current shunted to ground	45	49		V
$V_{O(on)}$	On-state output voltage	With one output programmed on and conducting	I_{OL} = 0.175 A			1	V
			I_{OL} = 0.5 A		1	1.3	V
			I_{OL} = 0.75 A		1.2	1.5	V
			I_{OL} = 1 A, During unlatch disable		1.4	1.6	V
V_{TOS}	Out-of-saturation threshold voltage	With output programmed on and an overcurrent fault condition		1.6	1.8	2.1	V
$I_{O(off)}$	Off-state output current	V_O = 24 V with output programmed off				600	µA
$I_{O(cl)}$	Output current limit	V_O = 3 V with output programmed on		1	1.8		A
	Internal output pulldown resistor			40	90		kΩ

shift register (Inputs SI, $\overline{SCLK}$, SCLK, and $\overline{RST}$)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V_{IT+}	Positive-going threshold voltage			0.75 V_{CC}	V
V_{IT-}	Negative-going threshold voltage		0.1 V_{CC}		V
V_{hys}	Hysteresis voltage ($V_{IT+} - V_{IT-}$)		0.85	2.5	V
I_I	Input current	V_I = 0 to V_{CC}		±10	µA
C_i	Input capacitance	V_I = 0 to V_{CC}		20	pF

shift register (output SO)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OL}	Low-level output voltage	I_O = 1.6 mA			0.2	0.4	V
V_{OH}	High-level output voltage	I_O = – 0.8 mA		V_{CC} –1.3			V
I_O	Output current	V_O = 0 to V_{CC},	$\overline{SIOE}$ input high			±20	µA
C_o	Output capacitance	V_O = 0 to V_{CC},	$\overline{SIOE}$ input high			20	pF

† All typical values are at V_{CC} = 5 V, T_J = 25°C.

timing requirements over recommended ranges of supply voltage and operating case temperature (see Figure 1)

			MIN	MAX	UNIT
f_{clock}	Clock frequency, SCLK	See Note 7	0	1	MHz
$t_{w(SCLKH)}$	Pulse duration, SCLK high		410		ns
$t_{w(SCLKL)}$	Pulse duration, SCLK low		410		ns
$t_{w(RST)}$	Pulse duration, $\overline{RST}$ low		1200		ns
t_{su1}	Setup time, $\overline{SIOE}$↓ before SCLK↑		1		µs
t_{su2}	Setup time, SCLK↓ before $\overline{SIOE}$↑		1		µs
t_{su3}	Setup time, SI high before SCLK↓		150		ns
t_{h1}	Hold time, SI low after SCLK↓		150		ns
t_r	Rise time, SCLK, SI, $\overline{SIOE}$			90	ns
t_f	Fall time, SCLK, SI, $\overline{SIOE}$			90	ns

NOTE 7: For cascaded operation, the clock pulse durations ($t_{w(SCLKL)}$ and $t_{w(SCLKH)}$) must be a minimum of 700 ns (giving a maximum clock frequency of 632 kHz).

thermal characteristics

PARAMETER		MIN	MAX	UNIT
$R_{\theta JC}$	Thermal resistance, junction-to-case temperature		3	°C/W
$R_{\theta JA}$	Thermal resistance, junction-to-ambient temperature		35	°C/W

switching characteristics over recommended ranges of supply voltage and operating case temperature

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	MAX	UNIT
t_{en}	Enable time	$\overline{SIOE}$↓	SO	C_L = 20 pF, R_L = 1 kΩ, See Figure 2		1000	ns
t_{dis}	Disable time	$\overline{SIOE}$↑	SO	C_L = 20 pF, R_L = 1 kΩ, See Figure 2		1000	ns
t_{d1}	Delay time, valid data	SCLK↑	SO	C_L = 200 pF, See Figure 3		550	ns
t_{d2}	Delay time, unlatch disable	$\overline{SIOE}$↑	Y_n	C_L = 20 pF, R_L = 5 Ω, See Figure 4	75	450	µs
$t_{r(SO)}$	Rise time		SO	C_L = 200 pF, See Figure 3		150	ns
$t_{f(SO)}$	Fall time		SO	C_L = 200 pF, See Figure 3		150	ns
$t_{d(on)}$	Delay time, turn on	$\overline{SIOE}$↑	Y_n	C_L = 20 pF, R_L = 28 Ω, I_{OL} = 500 mA, See Figure 5		10	µs
$t_{d(off)}$	Delay time, turn off	$\overline{SIOE}$↑	Y_n	C_L = 20 pF, R_L = 28 Ω, I_{OL} = 500 mA, See Figure 5		10	µs
t_v	Valid time, SO output data remains valid after SCLK high	SCLK↑	SO	C_L = 200 pF, See Figure 3	0		ns

PARAMETER MEASUREMENT INFORMATION

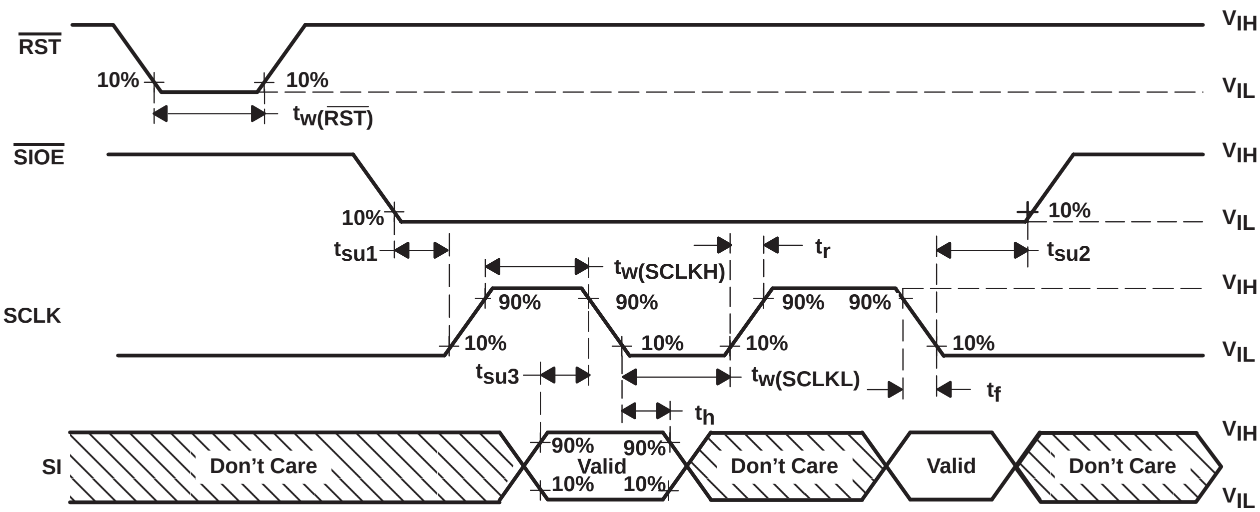
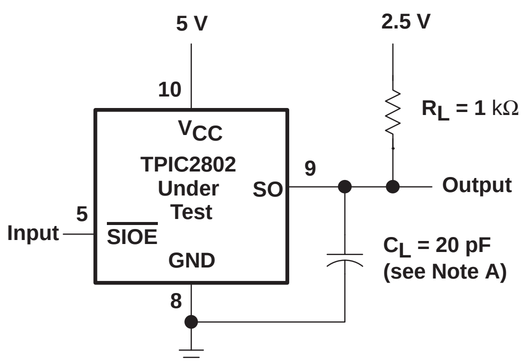
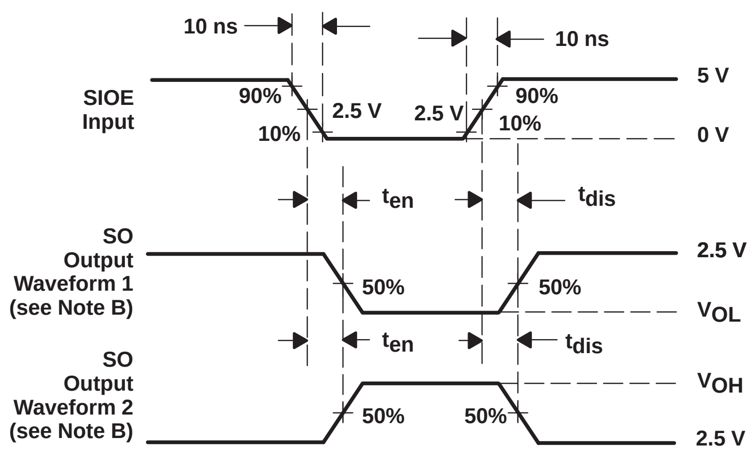


Figure 1. Input Timing Waveforms



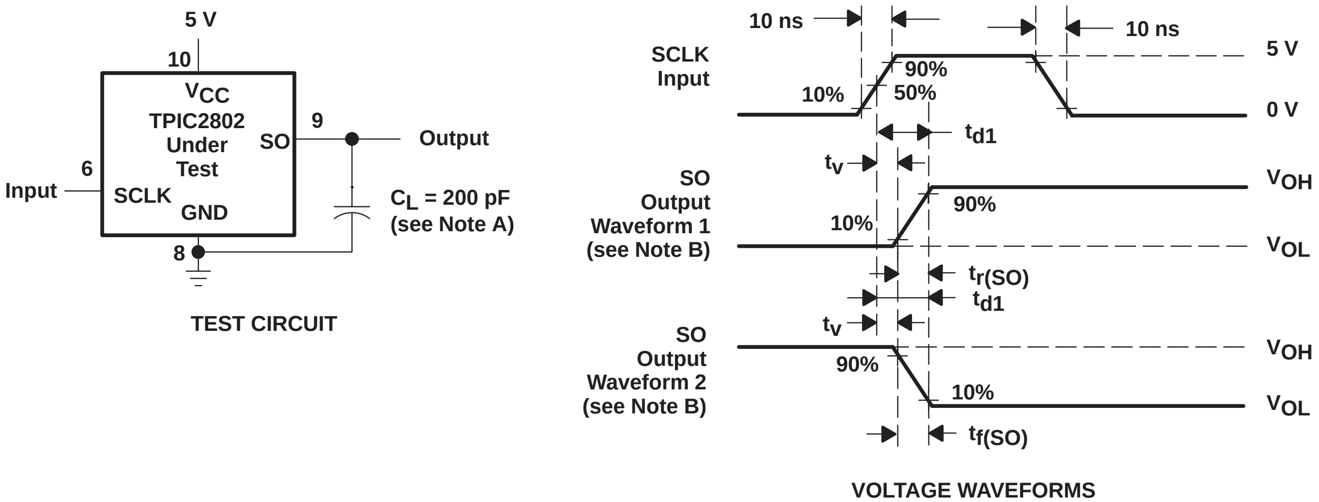


NOTES: A. C_L includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control when $\overline{SIOE}$ is high. Waveform 2 is for an output with internal conditions such that the low-to-high transition of $\overline{SIOE}$ causes the output to switch from off to on.

Figure 2. Test Circuit and Voltage Waveforms for Enable and Disable Times

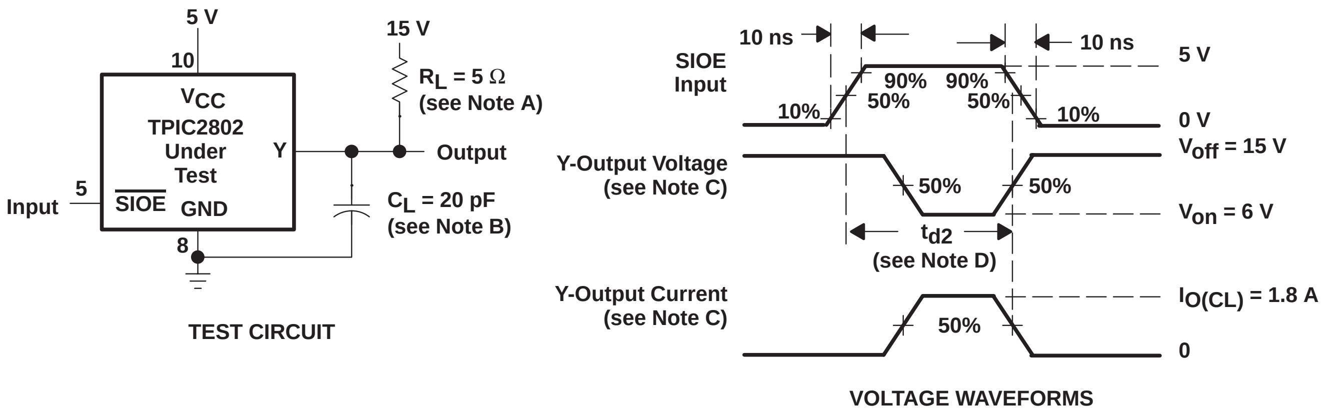
PARAMETER MEASUREMENT INFORMATION



NOTES: C. C_L includes probe and jig capacitance.

D. Waveform 1 is for an output with internal conditions such that the low-to-high transition of SCLK causes the SO output to switch from high to low. Waveform 2 is for an output with internal conditions such that the low-to-high transition of $\overline{SIOE}$ causes the output to switch from off to on.

Figure 3. Test Circuit and Voltage Waveforms for Delay Times



NOTES: A. Load voltage V_S and load resistance R_L are selected such that on-state voltage at the Y output under test, V_{on} is greater than the maximum out-of-saturation hold voltage, V_{TOS}. Thus $V_{OL} = V_{on} > V_{TOS(max)} = 2.1$ V.

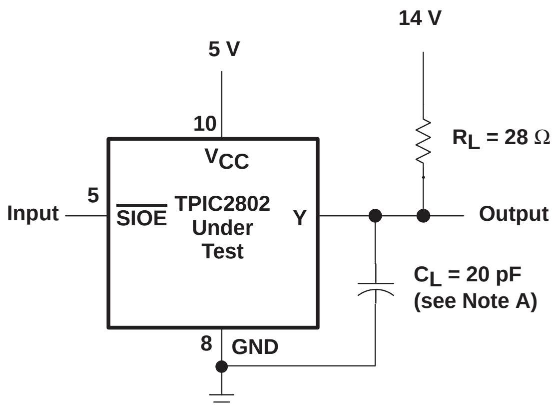
B. C_L includes probe and jig capacitance.

C. Output voltage and current waveforms are for an output with internal conditions such that the low-to-high transition of $\overline{SIOE}$ causes the output to switch from off to on.

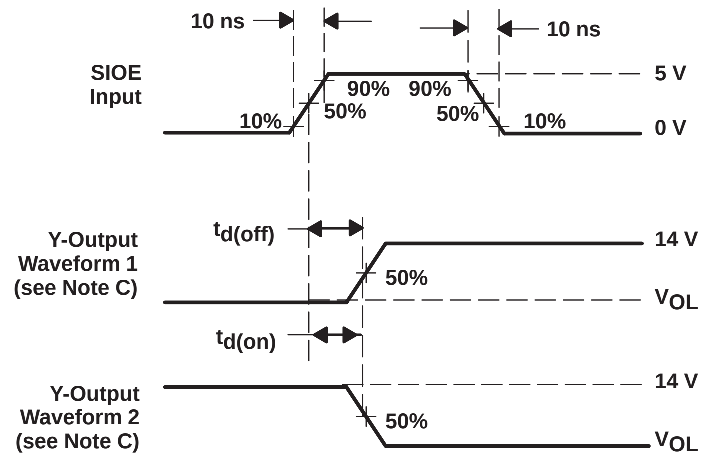
D. t_{d2} = delay until Y-output current goes off under fault condition.

Figure 4. Test Circuit and Voltage Waveforms for Unlatch Disable Delay

PARAMETER MEASUREMENT INFORMATION



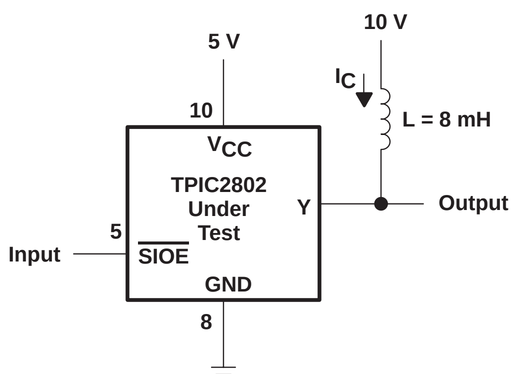
TEST CIRCUIT FOR TURN-OFF $t_{d(off)}$ AND TURN-ON $t_{d(on)}$ DELAY TIMES (see Note B)



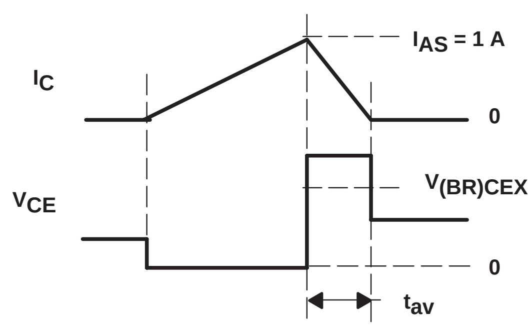
VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. $t_{d(off)} = t_{PLH}$, $t_{d(on)} = t_{PHL}$
C. Waveform 1 is for an output with internal conditions such that the low-to-high transition of $\overline{\text{SIOE}}$ causes the output to switch from on to off. Waveform 2 is for an output with internal conditions such that the low-to-high transition of $\overline{\text{SIOE}}$ causes the output to switch from off to on.

Figure 5. Test Current and Voltage and Current Waveforms for Turn-Off and Turn-On Delay Times



(a) TEST CIRCUIT



(b) VOLTAGE AND CURRENT WAVEFORMS

Figure 6. Single-Pulse Avalanche Energy Test Circuit and Waveforms

TYPICAL CHARACTERISTICS

PEAK AVALANCHE CURRENT vs TIME DURATION OF AVALANCHE

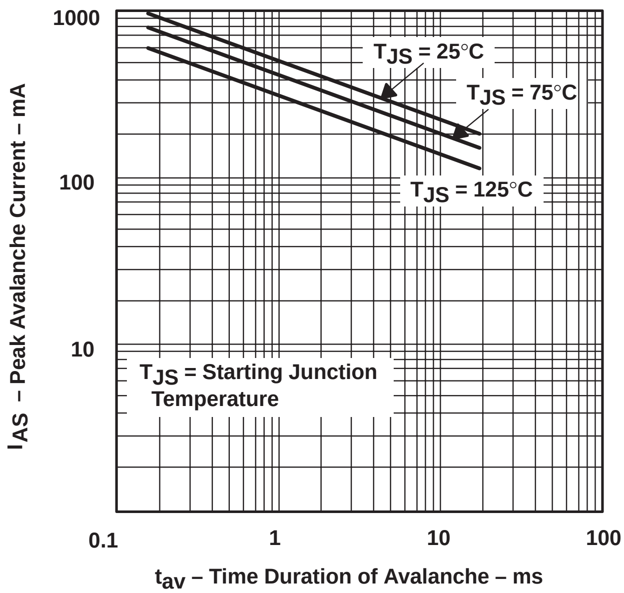


Figure 7

PEAK AVALANCHE CURRENT vs JUNCTION TEMPERATURE

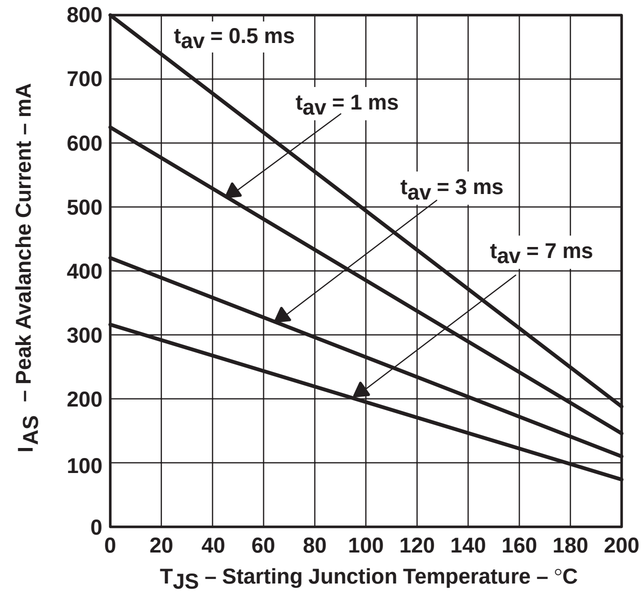


Figure 8

APPLICATION INFORMATION

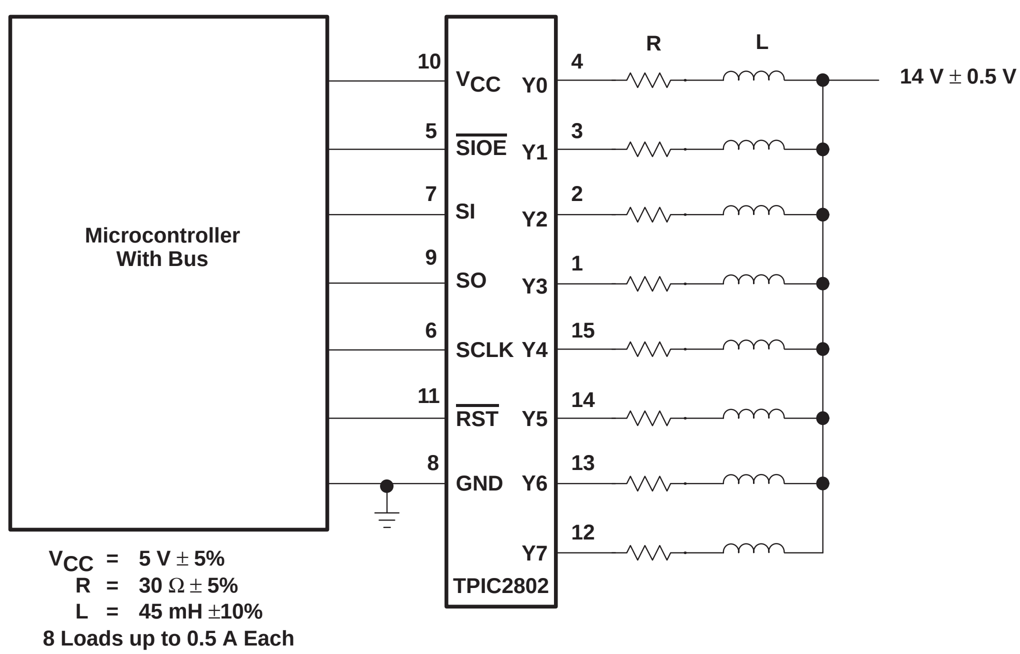


Figure 9. Microcontroller Driving Eight Loads Using a TPIC2802 for Load Interface

PRINCIPLES OF OPERATION

timing data transfer

Figure 10 shows the overall 8-bit data-byte transfer to and from the TPIC2802 interface bus. The logic state of the eight output drivers, Y0 through Y7, is latched into the shift register at time t_0 on the high-to-low transition of $\overline{SIOE}$. Therefore, the SO output data (DY0, DY1 . . .) represent the conditions at the Y-driver outputs at time t_0. The data at the SO output is updated on the low-to-high transition of SCLK.

Input data present at the SI input is clocked into the shift register on the high-to-low transition of SCLK. As shown in Figure 10 on the SI input, input data DI7 is clocked at time t_1, DI6 is clocked at time t_2, etc. Eight SCLK pulses are used to serially load the eight bits of new data into the device. After all the new data is serially loaded, the low-to-high transition of SIOE parallel loads the new data to the eight driver output latches, which in turn directly control the eight Y-driver outputs.

An unlimited amount of data can be shifted through the shift register (into the SI and out the SO), and this allows other devices to be cascaded in a daisy chain with the TPIC2802. Once the last data bit has been shifted into the TPIC2802, the $\overline{SIOE}$ input is pulled high. The clock (SCLK) input is low at both transitions of the $\overline{SIOE}$ input to avoid any false clicking of the shift register. The SCLK input is gated by the $\overline{SIOE}$ input, so the SCLK input is ignored whenever $\overline{SIOE}$ is high. At the rising edge of $\overline{SIOE}$, the shift register data is latched into the parallel latch and the output stages are actuated by the new data. An internal 100-µs delay timer is also started on this rising edge. During the time delay, the outputs are protected only by the analog current-limiting circuits, since the resetting of the parallel latches by fault conditions are inhibited during this time period. This allows the device to overcome any high switching currents that can flow during turn-on. Once the delay ends, the output voltages are sensed by the comparators and any output voltages higher than nominally 1.8 V are latched off.

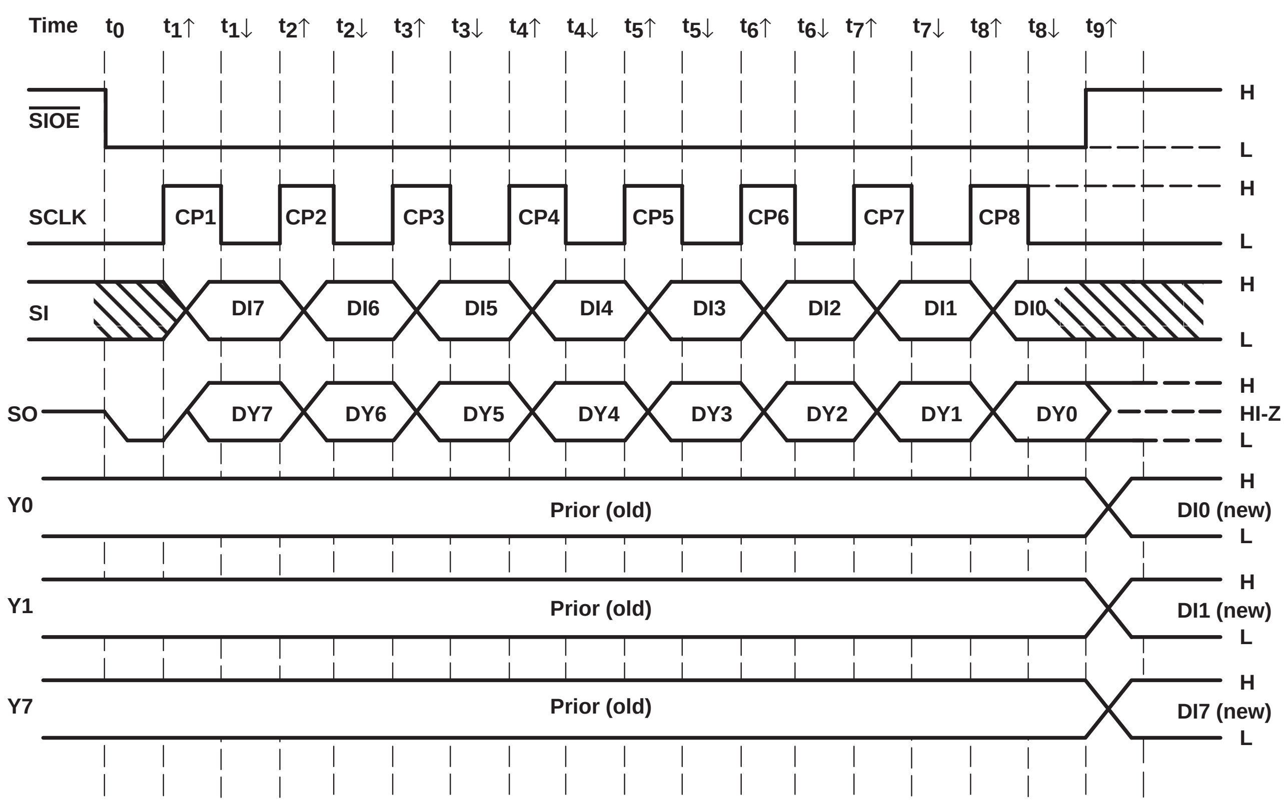


Figure 10. Data-Byte Transfer Timing

fault-conditions check

Open-circuit conditions on any output can be monitored or checked by programming that output off. After a short delay (microseconds), another control byte can be clocked into the device. If the diagnostic bit for that output comes back low, it indicates that the output is low and open circuited. A current overload condition can be detected by programming an output on. After waiting an appropriate length of time, another byte is clocked into the TPIC2802. The diagnostic bit clocked back from the TPIC2802 in the subsequent data transfer indicates a low output. If a high returns, a current overload is indicated. A quick overall check can be done by clocking in a test control byte and after a sufficient time delay, clock in another control byte. The diagnostic data is exclusive ORed with the original control byte. If a fault condition exists, a high results from the subsequent exclusive OR.

IMPORTANT NOTICE