

3-CHANNEL INDEPENDENT GATE-PROTECTED POWER DMOS ARRAY

SLIS039A – SEPTEMBER 1994 – REVISED SEPTEMBER 1995

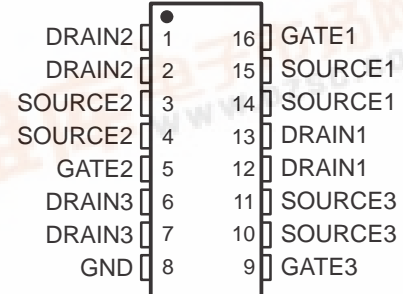
- Low $r_{DS(on)}$. . . 0.4 Ω Typ
- High Voltage Output . . . 60 V
- Extended ESD Capability . . . 4000 V
- Pulsed Current . . . 5 A Per Channel
- Fast Commutation Speed

description

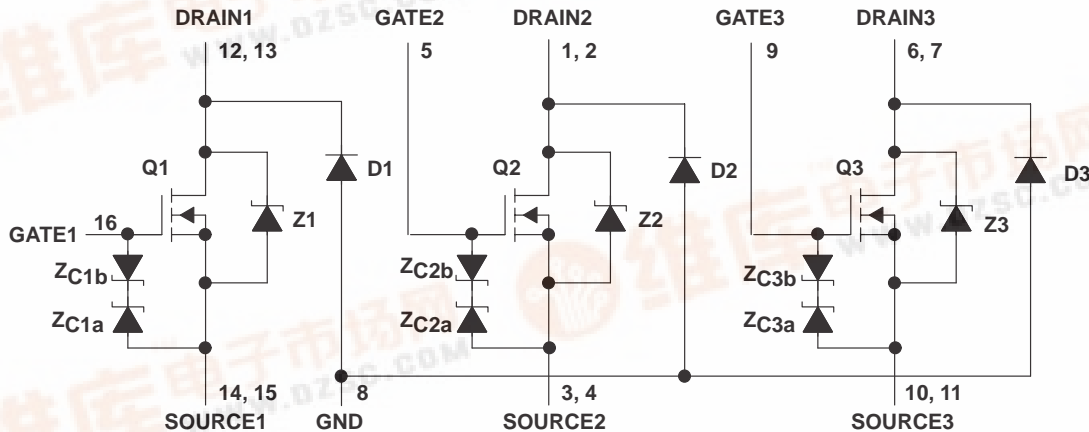
The TPIC5303 is a monolithic gate-protected power DMOS array that consists of three independent electrically isolated N-channel enhancement-mode DMOS transistors. Each transistor features integrated high-current zener diodes (Z_{CXa} and Z_{CXb}) to prevent gate damage in the event that an overstress condition occurs. These zener diodes also provide up to 4000 V of ESD protection when tested using the human-body model of a 100-pF capacitor in series with a 1.5-k Ω resistor.

The TPIC5303 is offered in a standard 16-pin small-outline surface-mount (D) package and is characterized for operation over the case temperature range of -40°C to 125°C .

D PACKAGE
(TOP VIEW)



schematic



NOTE A: For correct operation, no terminal pin may be taken below GND.

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absolute maximum ratings over operating case temperature range (unless otherwise noted)[†]

Drain-to-source voltage, V_{DS}	60 V
Source-to-GND voltage (Q1, Q2, and Q3)	100 V
Drain-to-GND voltage (Q1, Q2, and Q3)	100 V
Gate-to-source voltage range, V_{GS}	–9 V to 18 V
Continuous drain current, each output, $T_C = 25^\circ\text{C}$	1.4 A
Continuous source-to-drain diode current, $T_C = 25^\circ\text{C}$	1.4 A
Pulsed drain current, each output, I_{max} , $T_C = 25^\circ\text{C}$ (see Note 1 and Figure 15)	5 A
Continuous gate-to-source zener-diode current, $T_C = 25^\circ\text{C}$	± 50 mA
Pulsed gate-to-source zener-diode current, $T_C = 25^\circ\text{C}$	± 500 mA
Single-pulse avalanche energy, E_{AS} , $T_C = 25^\circ\text{C}$ (see Figures 4, 15, and 16)	10.2 mJ
Continuous total power dissipation, $T_C = 25^\circ\text{C}$ (see Figure 15)	1.08 W
Operating virtual junction temperature range, T_J	–40°C to 150°C
Operating case temperature range, T_C	–40°C to 125°C
Storage temperature range, T_{stg}	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Pulse duration = 10 ms, duty cycle = 2%

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electrical characteristics, $T_C = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(BR)DSX}$ Drain-to-source breakdown voltage	$I_D = 250\ \mu\text{A}$, $V_{GS} = 0$	60			V
$V_{GS(th)}$ Gate-to-source threshold voltage	$I_D = 1\ \text{mA}$, See Figure 5 $V_{DS} = V_{GS}$	1.5	1.8	2.2	V
$V_{(BR)GS}$ Gate-to-source breakdown voltage	$I_{GS} = 250\ \mu\text{A}$	18			V
$V_{(BR)SG}$ Source-to-gate breakdown voltage	$I_{SG} = 250\ \mu\text{A}$	9			V
$V_{(BR)}$ Reverse drain-to-GND breakdown voltage (across D1, D2, D3)	Drain-to-GND current = $250\ \mu\text{A}$	100			V
$V_{DS(on)}$ Drain-to-source on-state voltage	$I_D = 1.4\ \text{A}$, $V_{GS} = 10\ \text{V}$, See Notes 2 and 3		0.56	0.64	V
$V_{F(SD)}$ Forward on-state voltage, source-to-drain	$I_S = 1.4\ \text{A}$, $V_{GS} = 0$ (Z1, Z2, Z3), See Notes 2 and 3 and Figure 12		0.9	1.1	V
V_F Forward on-state voltage, GND-to-drain	$I_D = 1.4\ \text{A}$ (D1, D2, D3), See Notes 2 and 3		5		V
I_{DSS} Zero-gate-voltage drain current	$V_{DS} = 48\ \text{V}$, $V_{GS} = 0$	$T_C = 25^\circ\text{C}$	0.05	1	μA
		$T_C = 125^\circ\text{C}$	0.5	10	
I_{GSSF} Forward-gate current, drain short circuited to source	$V_{GS} = 15\ \text{V}$, $V_{DS} = 0$		20	200	nA
I_{GSSR} Reverse-gate current, drain short circuited to source	$V_{SG} = 5\ \text{V}$, $V_{DS} = 0$		10	100	nA
I_{lkg} Leakage current, drain-to-GND	$V_{DGND} = 48\ \text{V}$	$T_C = 25^\circ\text{C}$	0.05	1	μA
		$T_C = 125^\circ\text{C}$	0.5	10	
$r_{DS(on)}$ Static drain-to-source on-state resistance	$V_{GS} = 10\ \text{V}$, $I_D = 1.4\ \text{A}$, See Notes 2 and 3 and Figures 6 and 7	$T_C = 25^\circ\text{C}$	0.4	0.46	Ω
		$T_C = 125^\circ\text{C}$	0.62	0.66	
g_{fs} Forward transconductance	$V_{DS} = 15\ \text{V}$, $I_D = 0.7\ \text{A}$, See Notes 2 and 3 and Figure 9	1	1.19		S
C_{iss} Short-circuit input capacitance, common source	$V_{DS} = 25\ \text{V}$, $f = 1\ \text{MHz}$, $V_{GS} = 0$, See Figure 11		107	137	pF
C_{oss} Short-circuit output capacitance, common source			71	89	
C_{rss} Short-circuit reverse transfer capacitance, common source			22	28	

NOTES: 2. Technique should limit $T_J - T_C$ to 10°C maximum.
3. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

source-to-drain and GND-to-drain diode characteristics, $T_C = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t _{rr}	Reverse-recovery time	I _S = 0.7 A, V _{GS} = 0, See Figures 1 and 14	V _{DS} = 48 V, di/dt = 100 A/μs,	Z1, Z2, and Z3	92		ns
				D1, D2, and D3	244		
Q _{RR}	Total diode charge			Z1, Z2, and Z3	0.1		μC
				D1, D2, and D3	1.3		

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resistive-load switching characteristics, $T_C = 25^\circ\text{C}$

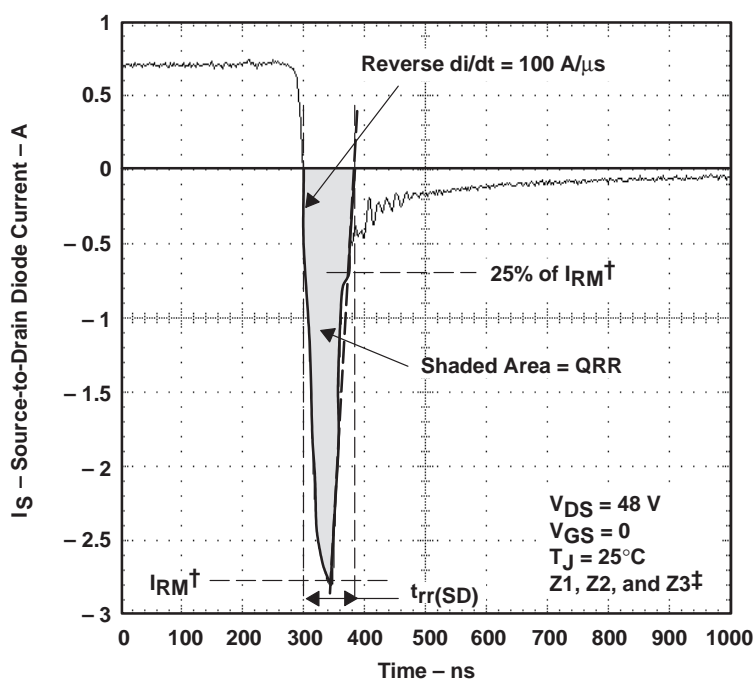
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(on)}$ Turn-on delay time	$V_{DD} = 25\text{ V}$, $t_{f1} = 10\text{ ns}$, $R_L = 36\ \Omega$, See Figure 2		25	40	ns
$t_{d(off)}$ Turn-off delay time			27	40	
t_{r2} Rise time			15	25	
t_{f2} Fall time			7	14	
Q_g Total gate charge	$V_{DS} = 48\text{ V}$, See Figure 3 $I_D = 0.7\text{ A}$, $V_{GS} = 10\text{ V}$		2.1	2.6	nC
$Q_{gs(th)}$ Threshold gate-to-source charge			0.3	0.38	
Q_{gd} Gate-to-drain charge			1.2	1.5	
L_D Internal drain inductance			5		nH
L_S Internal source inductance			5		
R_g Internal gate resistance			0.25		Ω

thermal resistance

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{\theta JA}$ Junction-to-ambient thermal resistance	See Notes 4 and 7		115		$^\circ\text{C/W}$
$R_{\theta JB}$ Junction-to-board thermal resistance	See Notes 5 and 7		64		
$R_{\theta JP}$ Junction-to-pin thermal resistance	See Notes 6 and 7		33		

- NOTES:
- Package mounted on an FR4 printed-circuit board with no heatsink.
 - Package mounted on a 24 inch², 4-layer FR4 printed-circuit board.
 - Package mounted in intimate contact with infinite heatsink.
 - All outputs with equal power

PARAMETER MEASUREMENT INFORMATION



† I_{RM} = maximum recovery current

‡ The above waveform is representative of D1, D2, and D3 in shape only.

Figure 1. Reverse-Recovery-Current Waveform of Source-to-Drain Diode

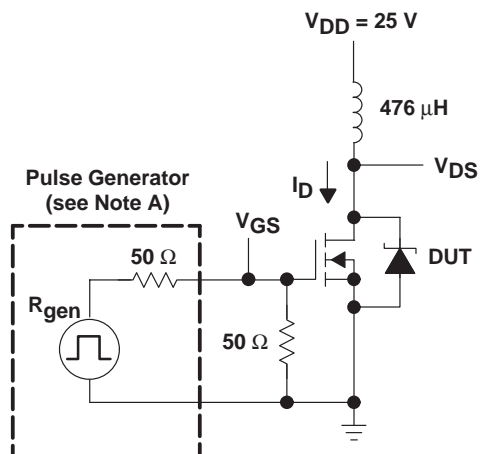
VOLTAGE WAVEFORM

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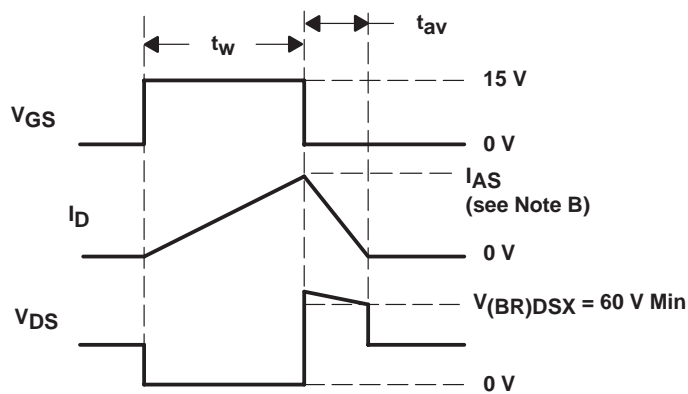
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PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE AND CURRENT WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, $Z_O = 50 \Omega$.

B. Input pulse duration (t_w) is increased until peak current $I_{AS} = 5$ A.

Energy test level is defined as $E_{AS} = \frac{I_{AS} \times V_{(BR)DSX} \times t_{av}}{2} = 10.2$ mJ, where t_{av} = avalanche time.

Figure 4. Single-Pulse Avalanche Energy Test Circuit and Waveforms

TYPICAL CHARACTERISTICS

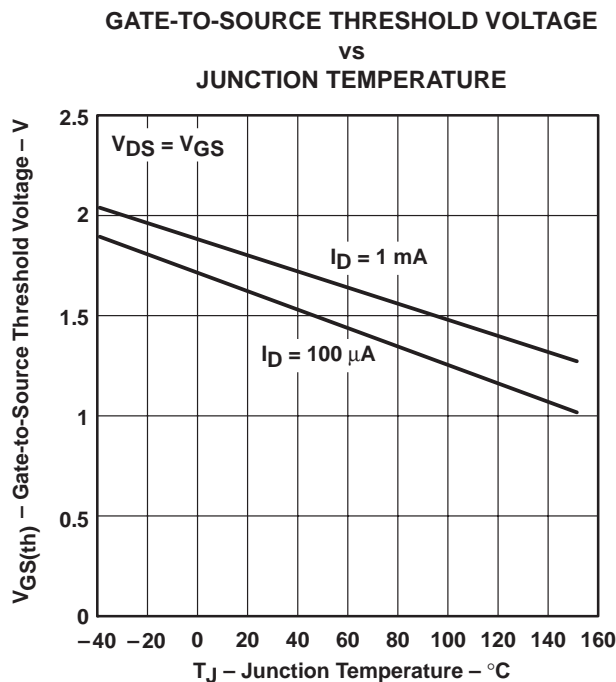


Figure 5

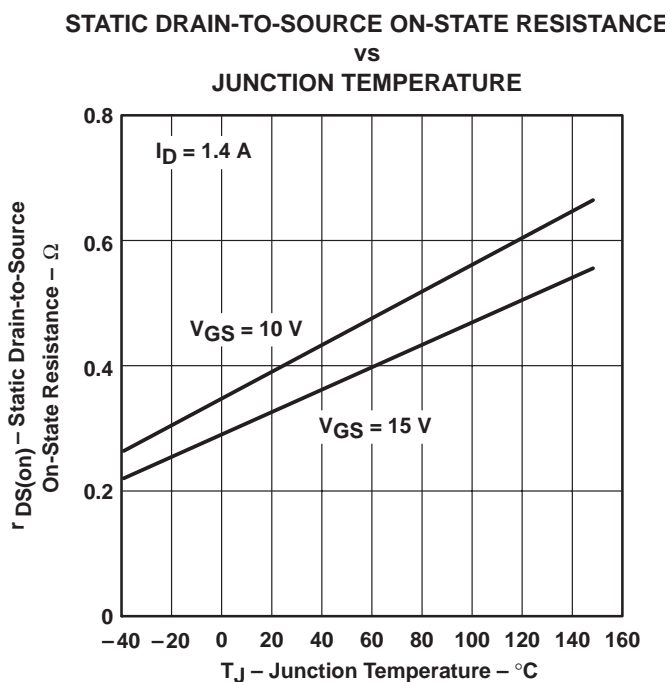


Figure 6

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TYPICAL CHARACTERISTICS

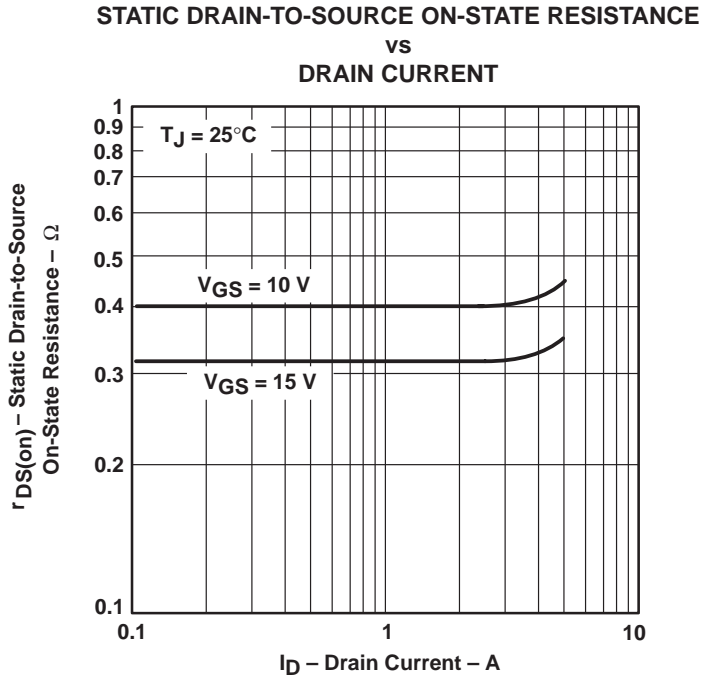


Figure 7

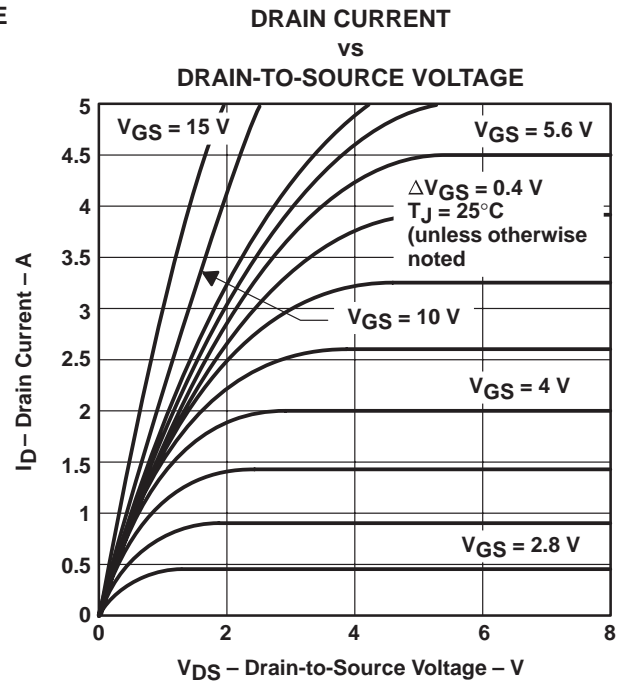


Figure 8

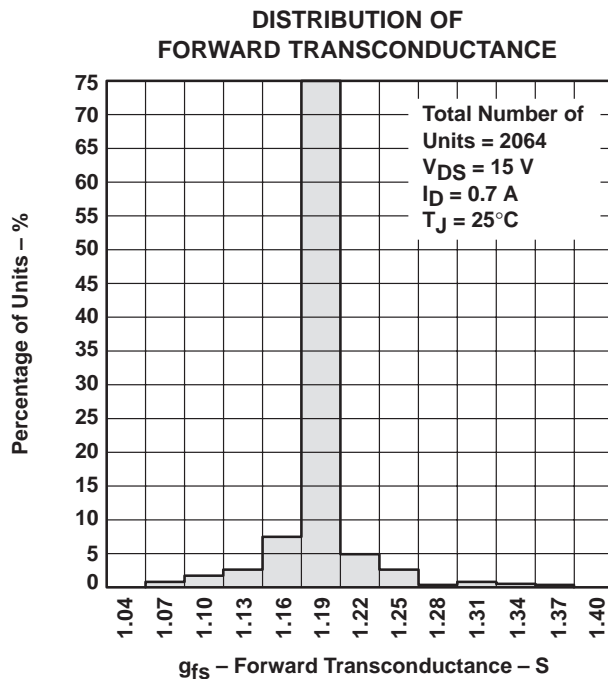


Figure 9

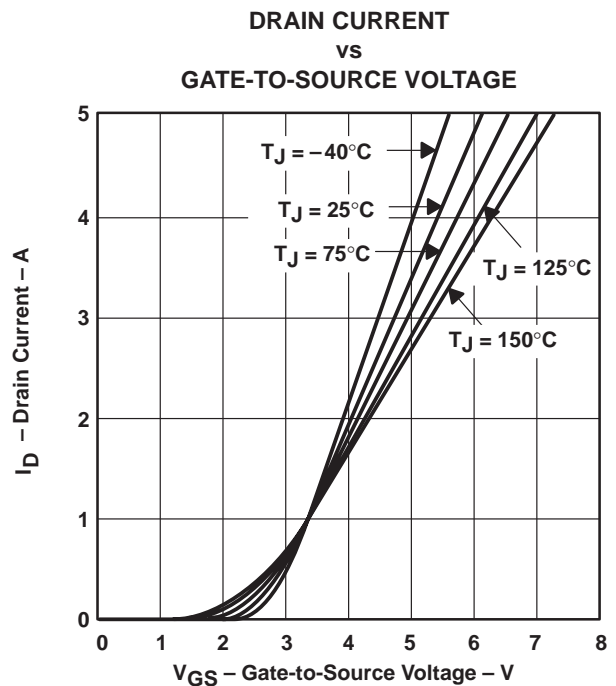


Figure 10

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TYPICAL CHARACTERISTICS

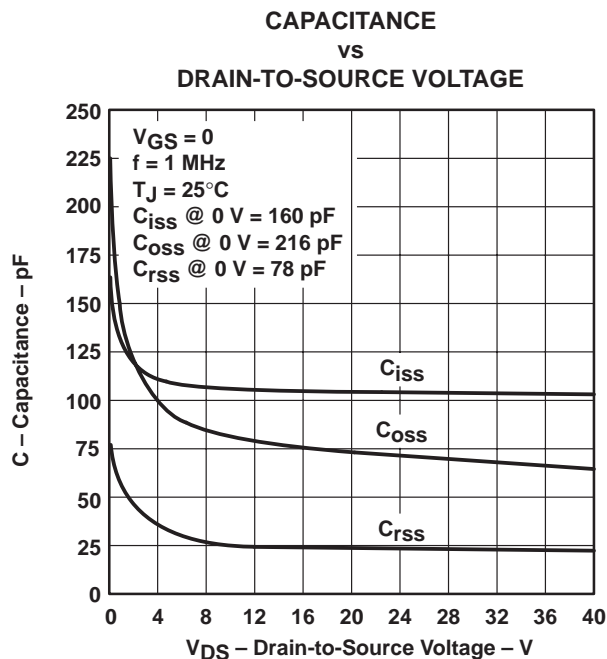


Figure 11

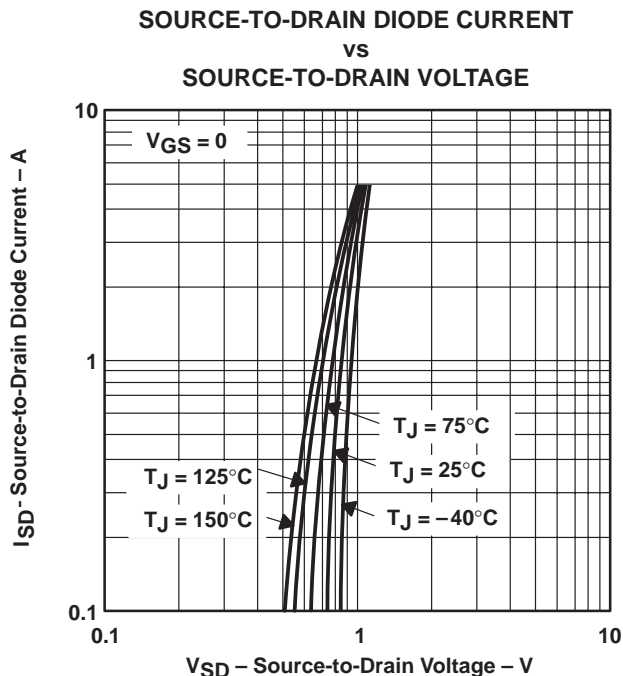


Figure 12

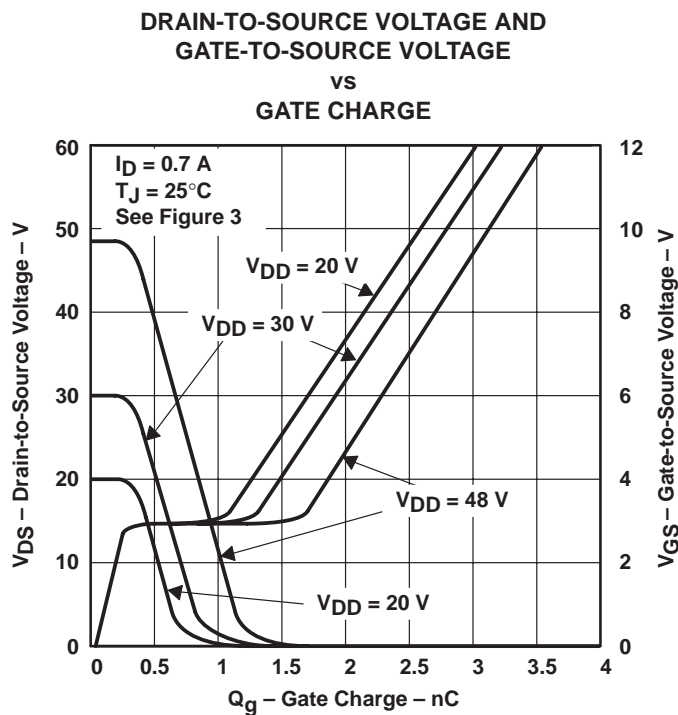


Figure 13

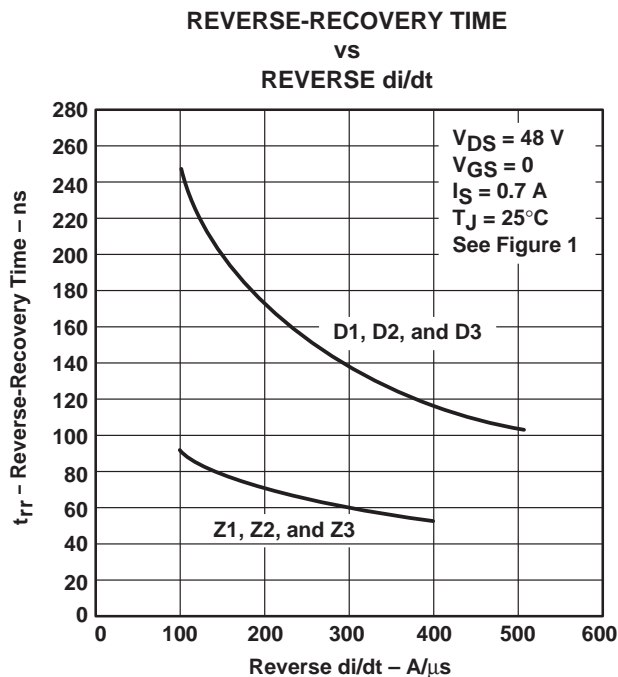
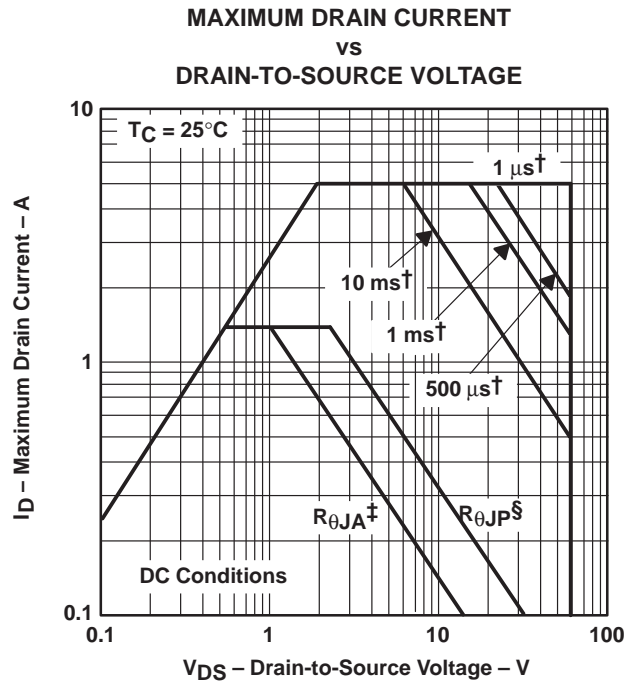


Figure 14

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THERMAL INFORMATION



† Less than 2% duty cycle

‡ Device mounted on FR4 printed-circuit board with no heatsink.

§ Device mounted in intimate contact with infinite heatsink.

Figure 15

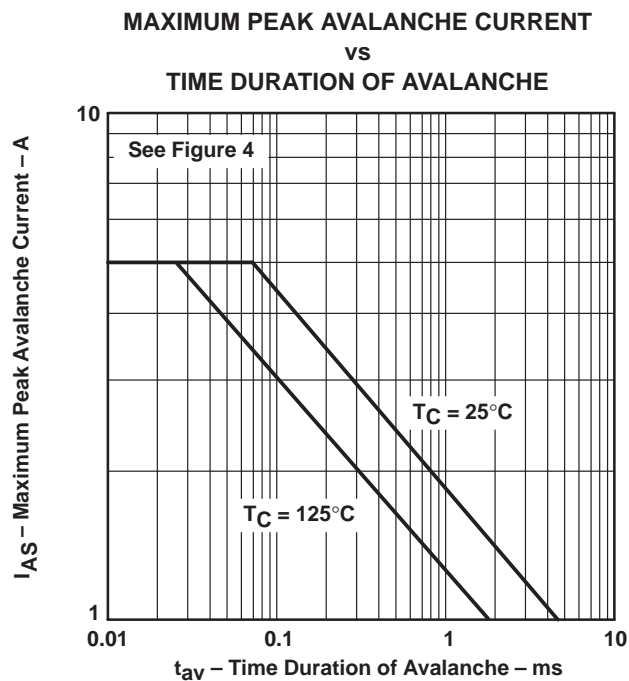


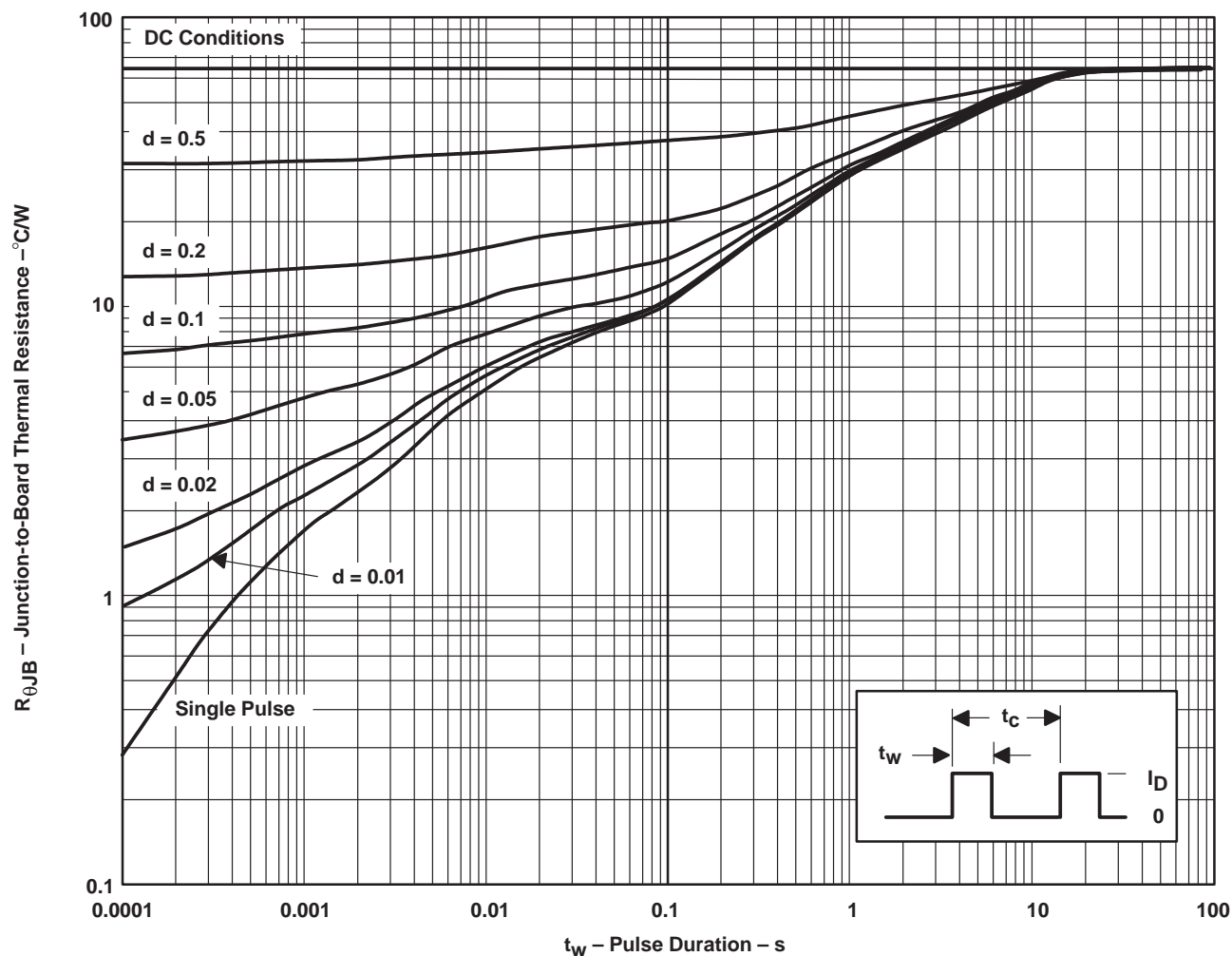
Figure 16

TPIC5303
3-CHANNEL INDEPENDENT GATE-PROTECTED
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THERMAL INFORMATION

D PACKAGE†
JUNCTION-TO-BOARD THERMAL RESISTANCE
VS
PULSE DURATION



† Device mounted on 24 in², 4-layer FR4 printed-circuit board with no heatsink

NOTE A: $Z_{\theta JB}(t) = r(t) R_{\theta JB}$

t_w = pulse duration

t_c = cycle time

d = duty cycle = t_w/t_c

Figure 17

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