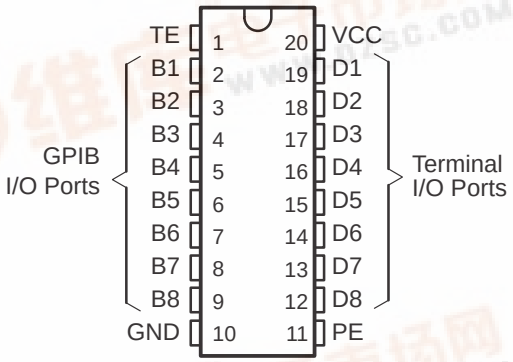
SN75160B
OCTAL GENERAL-PURPOSE INTERFACE BUS TRANSCEIVER

SLLS004B – OCTOBER 1985 – REVISED MAY 1995

- Meets IEEE Standard 488-1978 (GPIB)
- 8-Channel Bidirectional Transceiver
- Power-Up/Power-Down Protection (Glitch Free)
- High-Speed, Low-Power Schottky Circuitry
- Low Power Dissipation . . . 72 mW Max Per Channel
- Fast Propagation Times . . . 22 ns Max
- High-Impedance pnp Inputs
- Receiver Hysteresis . . . 650 mV Typ
- Open-Collector Driver Output Option
- No Loading of Bus When Device Is Powered Down (V_{CC} = 0)

DW OR N PACKAGE
(TOP VIEW)



description

The SN75160B 8-channel general-purpose interface bus (GPIB) transceiver is a monolithic, high-speed, low-power Schottky device designed for two-way data communications over single-ended transmission lines. It is designed to meet the requirements of IEEE Standard 488-1978. The transceiver features driver outputs that can be operated in either the passive-pullup or 3-state mode. If talk enable (TE) is high, these ports have the characteristics of passive-pullup outputs when pullup enable (PE) is low and of 3-state outputs when PE is high. Taking TE low places these ports in the high-impedance state. The driver outputs are designed to handle loads up to 48 mA of sink current.

Output glitches during power up and power down are eliminated by an internal circuit that disables both the bus and receiver outputs. The outputs do not load the bus when V_{CC} = 0. When combined with the SN75161B or SN75162B management bus transceivers, the pair provides the complete 16-wire interface for the IEEE-488 bus.

The SN75160B is characterized for operation from 0°C to 70°C.

Function Tables

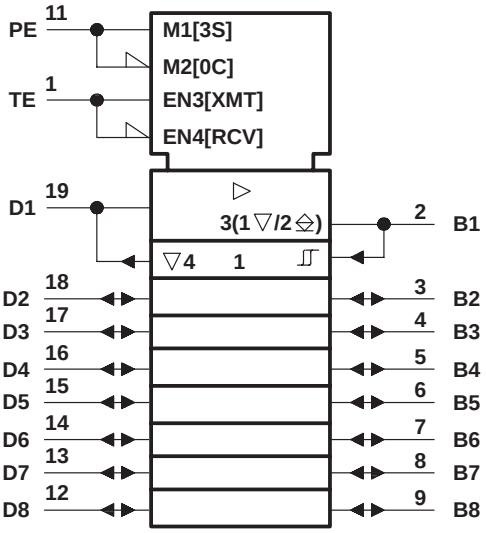
EACH DRIVER			
INPUTS			OUTPUT
D	TE	PE	B
H	H	H	H
L	H	X	L
H	X	L	Z†
X	L	X	Z†

EACH RECEIVER			
INPUTS			OUTPUT
B	TE	PE	D
L	L	X	L
H	L	X	H
X	H	X	Z

H = high level, L = low level, X = irrelevant, Z = high impedance

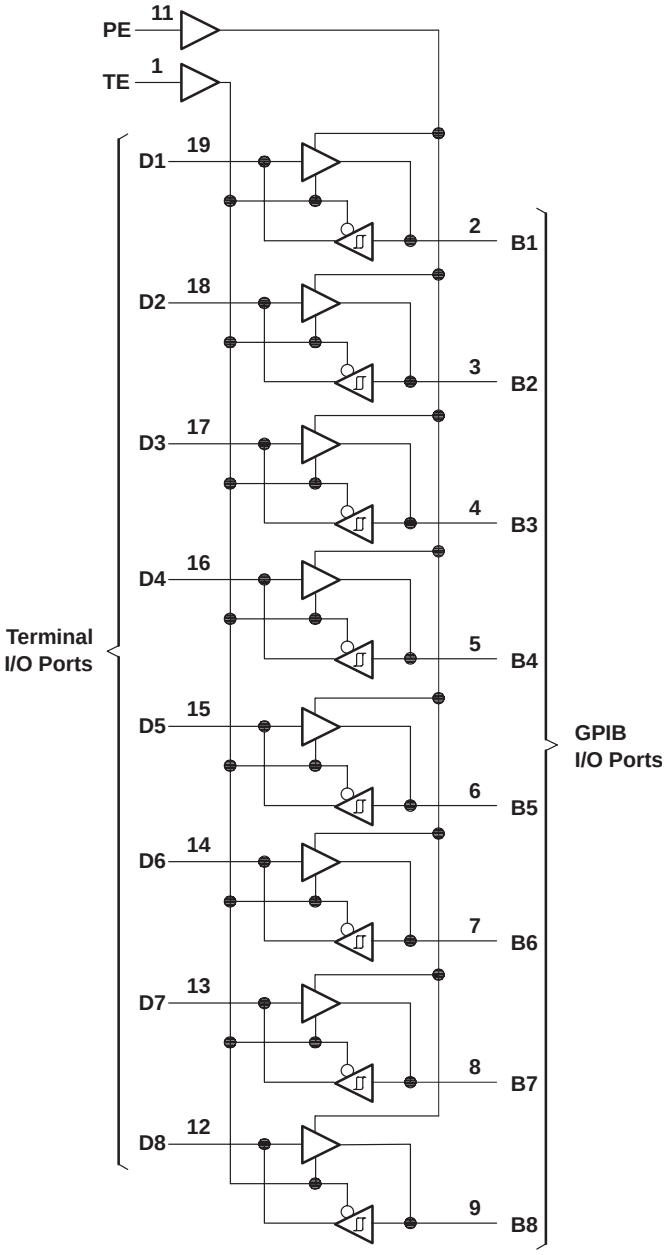
† This is the high-impedance state of a normal 3-state output modified by the internal resistors to V_{CC} and GND.

logic symbol†



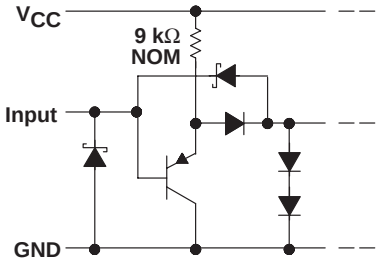
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
▽ Designates 3-state outputs
⏢ Designates passive-pullup outputs

logic diagram (positive logic)

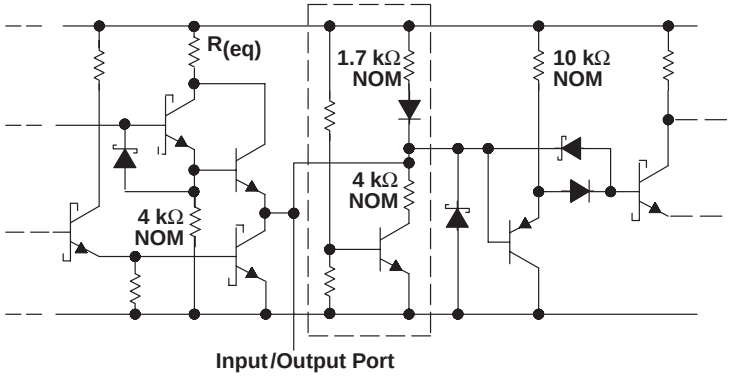


schematics of inputs and outputs

EQUIVALENT OF ALL CONTROL INPUTS



EQUIVALENT OF ALL INPUT/OUTPUT PORTS



Driver output $R_{(eq)}$ = 30 Ω NOM
Receiver output $R_{(eq)}$ = 110 Ω NOM
Circuit inside dashed lines is on the driver outputs only.
$R_{(eq)}$ = equivalent resistor

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage, V_I . . . . . 5.5 V
Low-level driver output current, I_{OL} . . . . . 100 mA
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
DW	1125 mW	9.0 mW/°C	720 mW
N	1150 mW	9.2 mW/°C	736 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level input voltage, V_{IH}		2			V
Low-level input voltage, V_{IL}				0.8	V
High-level output current, I_{OH}	Bus ports with pullups active			–5.2	mA
	Terminal ports			–800	µA
Low-level output current, I_{OL}	Bus ports			48	mA
	Terminal ports			16	
Operating free-air temperature, T_A		0		70	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

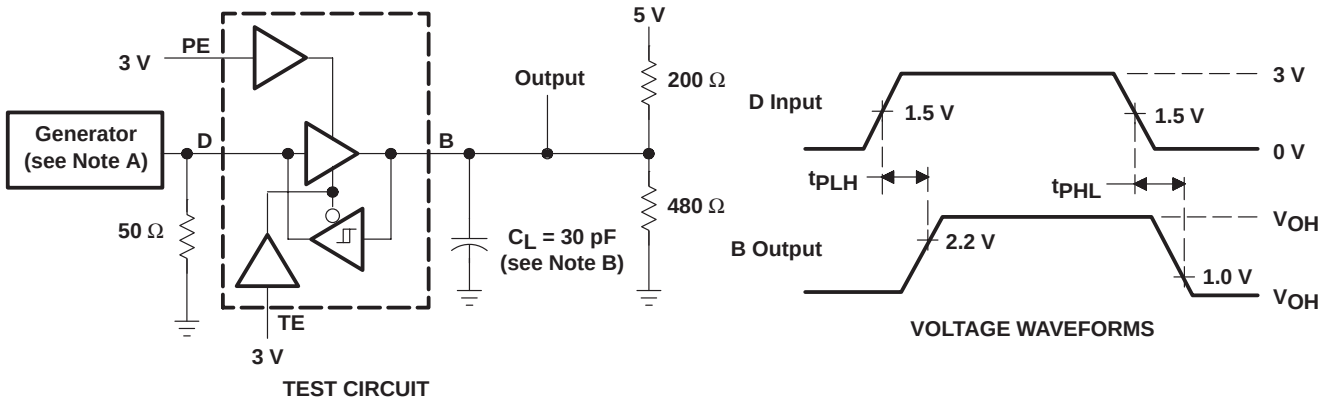
PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage		I_I = –18 mA			–0.8	–1.5	V
V_{hys}	Hysteresis voltage ($V_{IT+} - V_{IT-}$)	Bus	See Figure 8		0.4	0.65		V
V_{OH}	High-level output voltage	Terminal	I_{OH} = –800 µA,	TE at 0.8 V	2.7	3.5		V
		Bus	I_{OH} = –5.2 mA,	PE and TE at 2 V	2.5	3.3		
V_{OL}	Low-level output voltage	Terminal	I_{OL} = 16 mA,	TE at 0.8 V		0.3	0.5	V
		Bus	I_{OL} = 48 mA,	TE at 2 V		0.35	0.5	
I_I	Input current at maximum input voltage	Terminal	V_I = 5.5 V			0.2	100	µA
I_{IH}	High-level input current	Terminal	V_I = 2.7 V			0.1	20	µA
I_{IL}	Low-level input current	Terminal	V_I = 0.5 V			–10	–100	µA
$V_{I/O(bus)}$	Voltage at bus port		Driver disabled	$I_{I(bus)}$ = 0	2.5	3.0	3.7	V
				$I_{I(bus)}$ = –12 mA			–1.5	
$I_{I/O(bus)}$	Current into bus port	Power on	Driver disabled	$V_{I(bus)}$ = –1.5 V to 0.4 V	–1.3			mA
				$V_{I(bus)}$ = 0.4 V to 2.5 V	0		–3.2	
				$V_{I(bus)}$ = 2.5 V to 3.7 V			2.5 –3.2	
				$V_{I(bus)}$ = 3.7 V to 5 V	0		2.5	
				$V_{I(bus)}$ = 5 V to 5.5 V	0.7		2.5	
		Power off	V_{CC} = 0,	$V_{I(bus)}$ = 0 to 2.5 V			–40	
I_{OS}	Short-circuit output current	Terminal			–15	–35	–75	mA
		Bus			–25	–50	–125	
I_{CC}	Supply current		No load	Receivers low and enabled		70	90	mA
				Drivers low and enabled		85	110	
$C_{I/O(bus)}$	Bus-port capacitance		V_{CC} = 0 to 5 V, f = 1 MHz	$V_{I/O}$ = 0 to 2 V,		16		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, C_L = 15 pF, T_A = 25°C (unless otherwise noted)

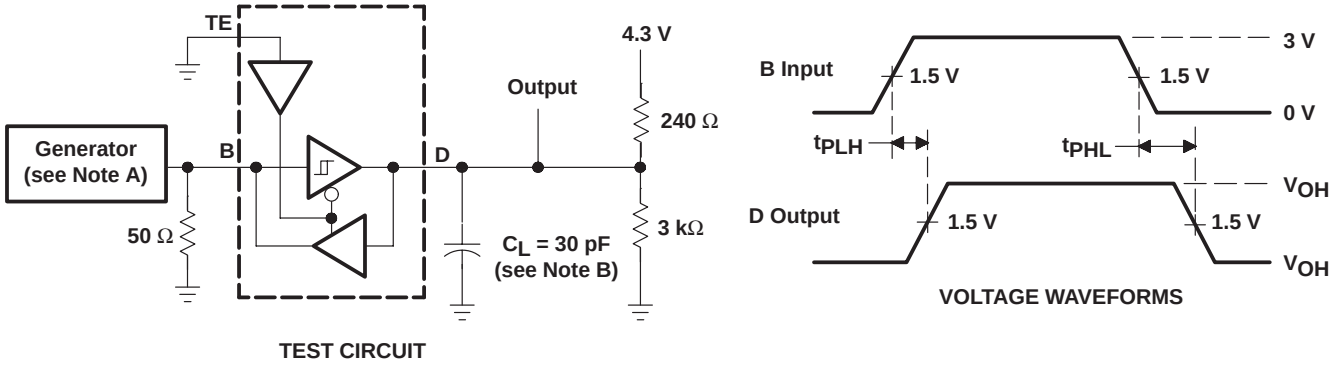
PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propation delay time, low- to high-level output	Terminal	Bus	C_L = 30 pF, See Figure 1		14	20	ns
t_{PHL}	Propagation delay time, high- to low-level output					14	20	
t_{PLH}	Propagation delay time, low- to high-level output	Bus	Terminal	C_L = 30 pF, See Figure 2		10	20	ns
t_{PHL}	Propagation delay time, high- to low-level output					15	22	
t_{PZH}	Output enable time to high level	TE	BUS	See Figure 3		25	35	ns
t_{PHZ}	Output disable time from high level					13	22	
t_{PZL}	Output enable time to low level					22	35	
t_{PLZ}	Output disable time from low level					22	32	
t_{PZH}	Output enable time to high level	TE	Terminal	See Figure 4		20	30	ns
t_{PHZ}	Output disable time from high level					12	20	
t_{PZL}	Output enable time to low level					23	32	
t_{PLZ}	Output disable time from low level					19	30	
t_{en}	Output pullup enable time	PE	Bus	See Figure 5		15	22	ns
t_{dis}	Output pullup disable time					13	20	

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

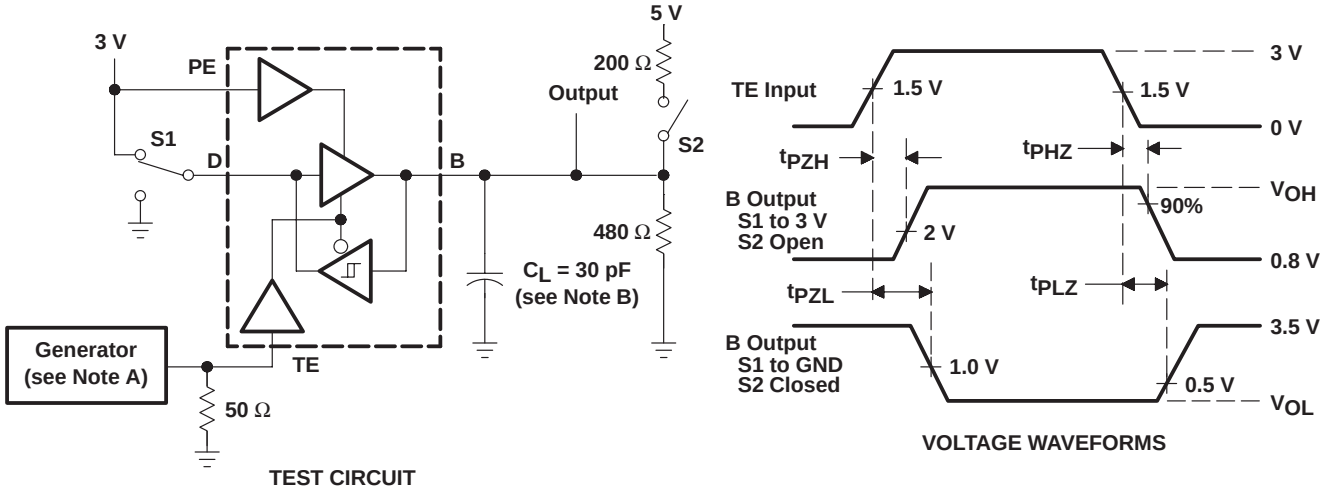
Figure 1. Terminal-to-Bus Test Circuit and Voltage Waveforms



NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

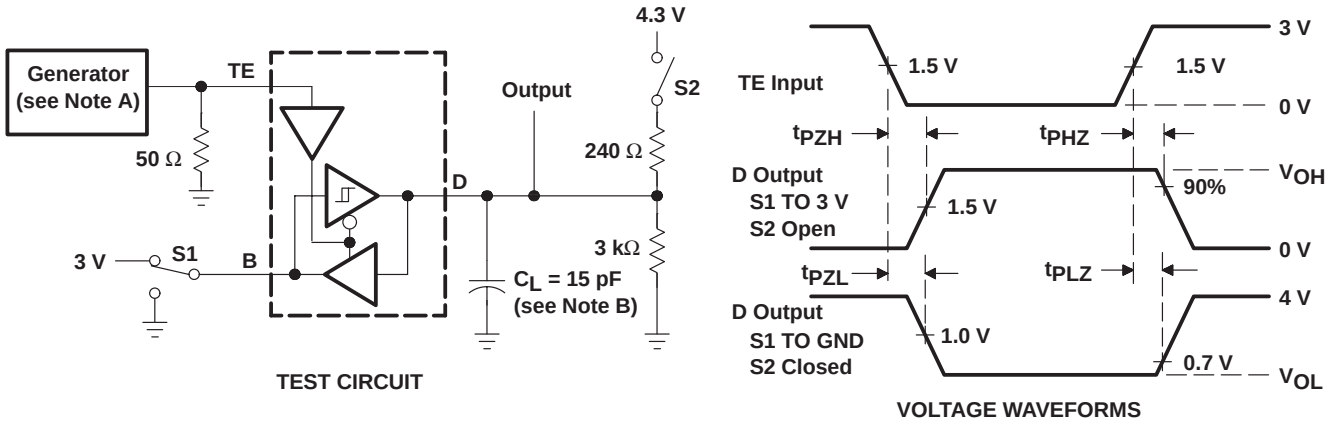
Figure 2. Bus-to-Terminal Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

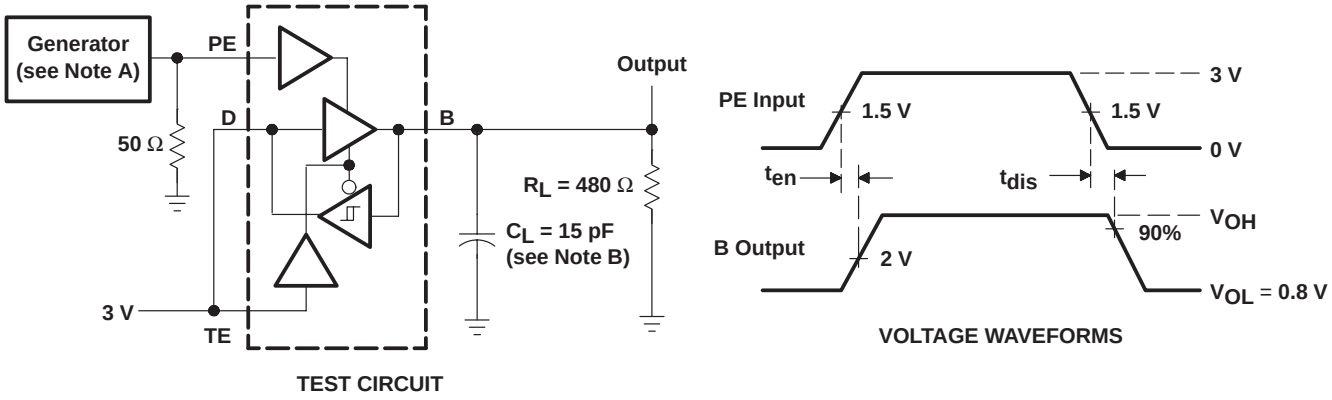
Figure 3. TE-to-Bus Test Circuit and Voltage Waveforms



NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

Figure 4. TE-to-Terminal Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

Figure 5. PE-to-Bus Pullup Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

TERMINAL I/O PORTS
HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

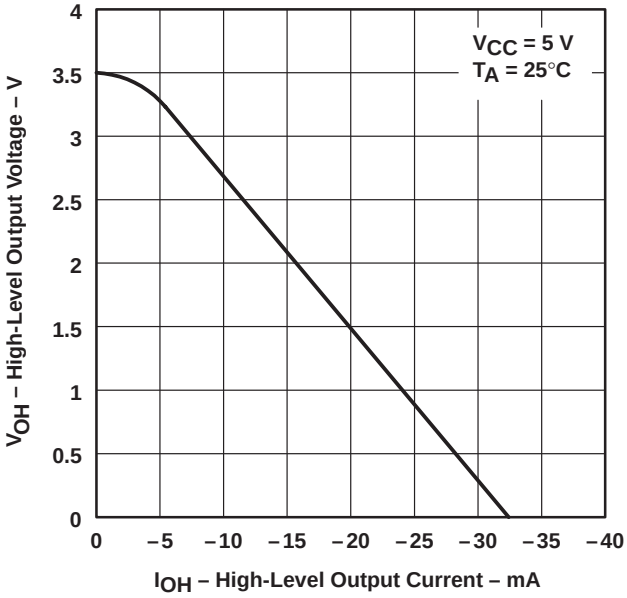


Figure 6

TERMINAL I/O PORTS
LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

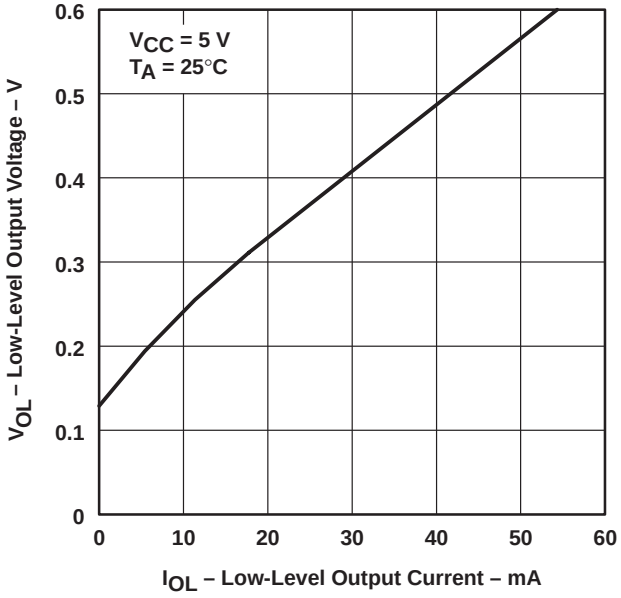


Figure 7

TERMINAL I/O PORTS
OUTPUT VOLTAGE
vs
BUS INPUT VOLTAGE

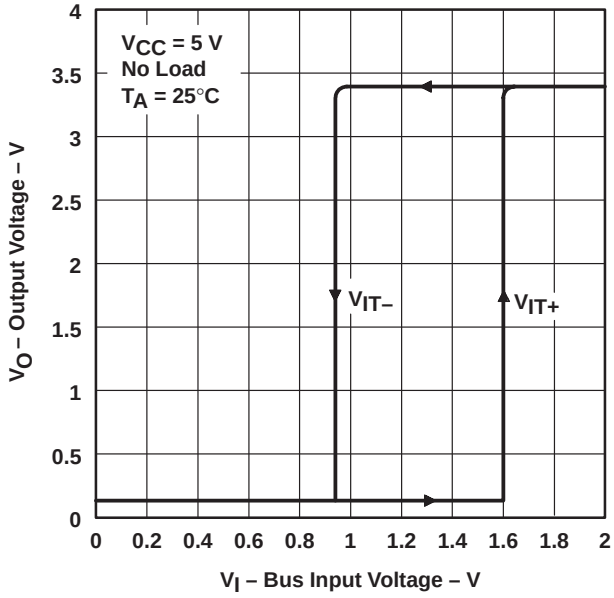


Figure 8

TYPICAL CHARACTERISTICS

GPIB I/O PORTS
HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

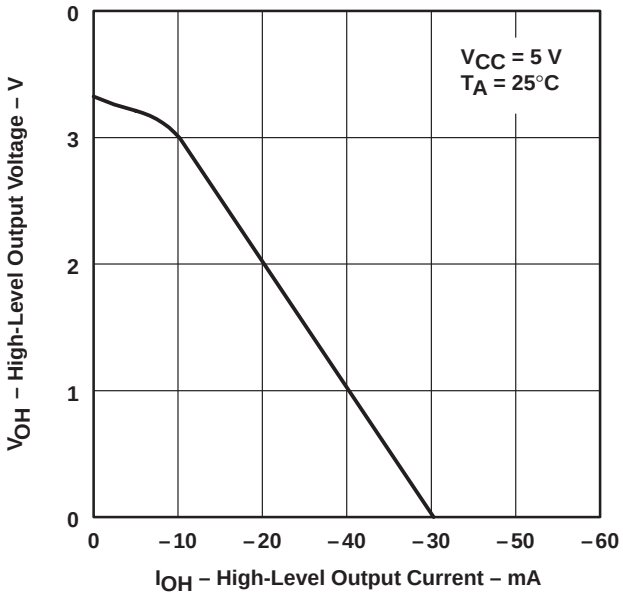


Figure 9

GPIB I/O PORTS
LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

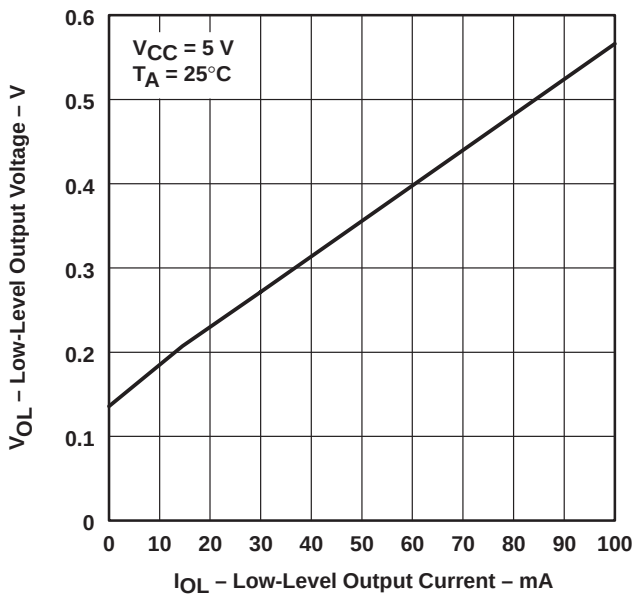


Figure 10

GPIB I/O PORTS
OUTPUT VOLTAGE
vs
THERMAL INPUT VOLTAGE

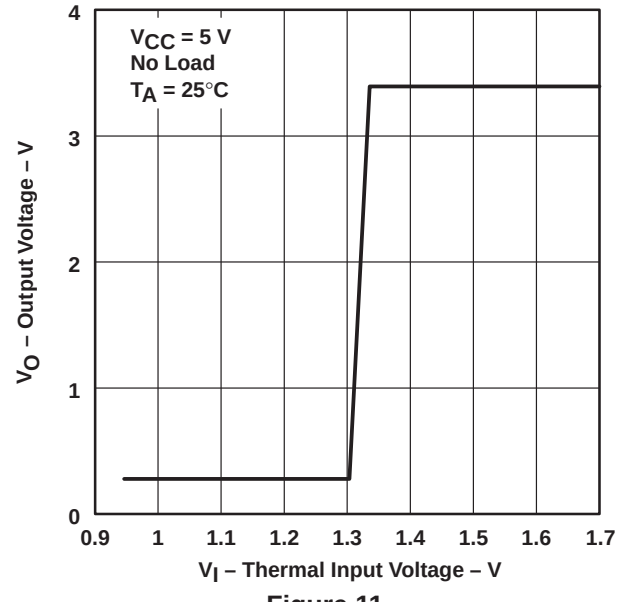


Figure 11

GPIB I/O PORTS
CURRENT
vs
VOLTAGE

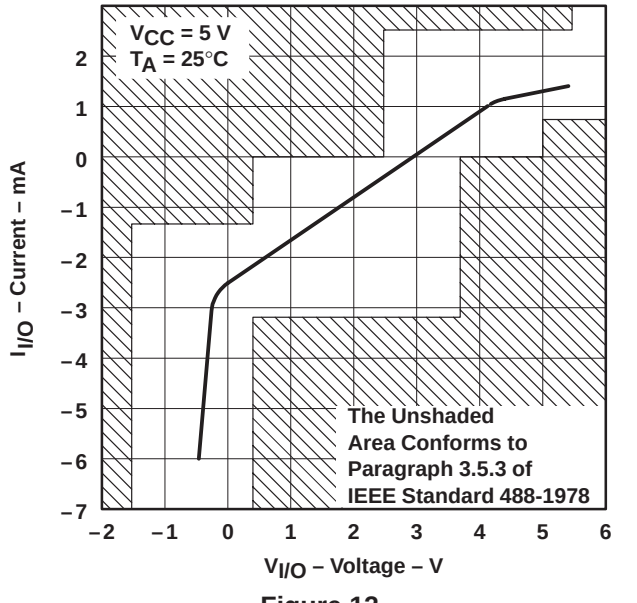


Figure 12

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