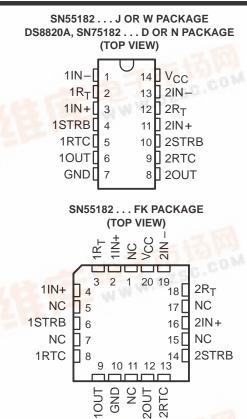
# 捷多邦,专业PCB打**D\$8820A以6N\$5182, SN75182** DUAL DIFFERENTIAL LINE RECEIVERS

SLLS092B - OCTOBER 1972 - REVISED MAY 1995

- Single 5-V Supply
- Differential Line Operation
- Dual Channels
- TTL Compatibility
- ±15-V Common-Mode Input Voltage Range
- ±15-V Differential Input Voltage Range
- Individual Channel Strobes
- Built-In Optional Line-Termination Resistor
- Individual Frequency Response Controls
- Designed for Use With Dual Differential **Drivers SN55183 and SN75183**
- Designed to Be Interchangeable With National Semiconductor DS7820A and **DS8820A**

#### description

The DS8820A, SN55182, and SN75182 dual differential line receivers are designed to sense small differential signals in the presence of large common-mode noise. These devices give TTLcompatible output signals as a function of the polarity of the differential input voltage. The frequency response of each channel may be easily controlled by a single external capacitor to provide immunity to differential noise spikes. The

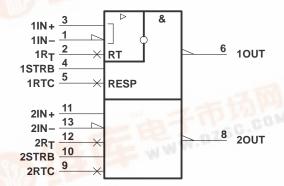


output goes to a high level when the inputs are open circuited. A strobe input is provided which, when in the low level, disables the receiver and forces the output to a high level.

The receiver is of monolithic single-chip construction, and both halves of the dual circuits use common power supply and ground terminals.

The SN55182 is characterized for operation over the full military temperature range of -55°C to 125°C. The DS8820A and SN75182 are characterized for operation from 0°C to 70°C.

# logic symbol†



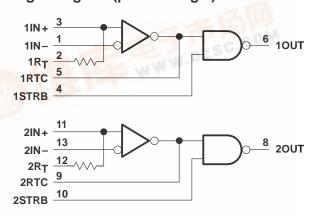
<sup>†</sup>This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for the D, J, N, and W packages.

#### logic diagram (positive logic)

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NC - No internal connection

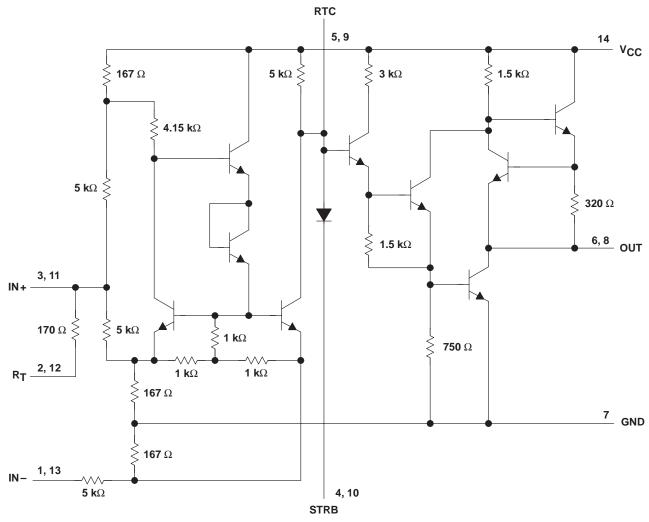




# DS8820A, SN55182, SN75182 DUAL DIFFERENTIAL LINE RECEIVERS

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#### schematic (each receiver)



Resistor values shown are nominal. Pin numbers shown are for the D, J, N, and W packages.

#### **FUNCTION TABLE**

STRB	V <sub>ID</sub>	OUT
L	Χ	Н
Н	Н	Н
Н	L	L

 $H = V_I \ge V_{IH}$  min or  $V_{ID}$  more positive than  $V_{TH}$  max

 $L = V_{I} \le V_{IL} \text{ max or } V_{ID} \text{ more negative}$ than  $V_{TL}$  max

X = irrelevant



## DS8820A, SN55182, SN75182 DUAL DIFFERENTIAL LINE RECEIVERS

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### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

	SN55182	DS8820A SN75182	UNIT	
Supply voltage, V <sub>CC</sub> (see Note 1)	8	8	V	
Common-mode input voltage, V <sub>IC</sub>	±20	±20	V	
Differential input voltage, V <sub>ID</sub> (see Note 2)	±20	±20	V	
Strobe input voltage, VI(STROB)	8	8	V	
Output sink current	50	50	mA	
Continuous total power dissipation	See Dissi	See Dissipation Rating Table		
Operating free-air temperature range, TA	-55 to 125	0 to 70	°C	
Storage temperature range, T <sub>Stg</sub>	-65 to 150	-65 to 150	°C	
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package		260	°C	
Case temperature for 60 seconds, T <sub>C</sub> : FK package	260		°C	
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J or W package	300	300	°C	

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground terminal.

2. Differential voltage values are at the noninverting terminal with respect to the inverting terminal.

#### **DISSIPATION RATING TABLE**

PACKAGE	$\begin{aligned} & \textbf{T}_{\pmb{A}} \leq \textbf{25}^{\circ} \textbf{C} \\ & \textbf{POWER RATING} \end{aligned}$	DERATING FACTOR ABOVE T <sub>A</sub> = 25°C	T <sub>A</sub> = 70°C POWER RATING	T <sub>A</sub> = 125°C POWER RATING
D	950 mW	7.6 mW/°C	608 mW	_
FK <sup>‡</sup>	1375 mW	11.0 mW/°C	880 mW	275 mW
J‡	1375 mW	11.0 mW/°C	880 mW	275 mW
N	1150 mW	9.2 mW/°C	736 mW	_
w‡	1000 mW	8.0 mW/°C	640 mW	200 mW

<sup>‡</sup> In the FK, J, and W packages, SN55182 chips are alloy mounted.

#### recommended operating conditions

	,	SN55182			DS8820A, SN75182		
	MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Supply voltage, V <sub>CC</sub>	4.5	5	5.5	4.5	5	5.5	V
Common-mode input voltage, V <sub>IC</sub>			±15			±15	V
High-level strobe input voltage, VIH(STRB)	2.1		5.5	2.1		5.5	V
Low-level strobe input voltage, V <sub>IL</sub> (STRB)	0		0.9	0		0.9	V
High-level output current, IOH			-400			-400	μΑ
Low-level output current, IOL			16			16	mA
Operating free-air temperature, T <sub>A</sub>	-55		125	0		70	°C



# DS8820A, SN55182, SN75182 DUAL DIFFERENTIAL LINE RECEIVERS

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## electrical characteristics over recommended ranges of $V_{CC}$ , $V_{IC}$ , and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP <sup>‡</sup>	MAX	UNIT	
\/	Positive-going input threshold voltage		$V_O = 2.5 \text{ V},$ $I_{OH} = -400 \mu\text{A}$	$V_{IC} = -3 V \text{ to } 3 V$			0.5	V
V <sub>IT+</sub> Positive-going input thr		old voltage		$V_{IC} = -15 \text{ V to } 15 \text{ V}$			1	V
\/	Negative-going input threst	ald valta as	V <sub>O</sub> = 0.4 V,	$V_{IC} = -3 \text{ V to } 3 \text{ V}$			-0.5	V
V <sub>IT</sub> –	Negative-going input tillesi	ioid voitage	I <sub>OL</sub> = 16 mA	$V_{IC} = -15 \text{ V to } 15 \text{ V}$			-1	V
		$V_{ID} = 1 \text{ V},$ $I_{OH} = -400 \mu\text{A}$	V <sub>(STRB)</sub> = 2.1 V,	2.5	4.2	5.5	V	
VOH	VOH High-level output voltage		$V_{ID} = -1 \text{ V},$ $I_{OH} = -400  \mu\text{A}$	V(STRB) = 0.4 V,	2.5	4.2	5.5	V
V <sub>OL</sub>	Low-level output voltage		$V_{ID} = -1 V$ $I_{OL} = 16 \text{ mA}$	V(STRB) = 2.1 V,		0.25	0.4	V
	Input current	Inverting input	V <sub>IC</sub> = 15 V			3	4.2	mA
			VIC = 0			0	-0.5	
l <sub>i</sub> .			V <sub>IC</sub> = -15 V			-3	-4.2	
'1		Noninverting input	V <sub>IC</sub> = 15 V			5	7	
			VIC = 0			-1	-1.4	mA
			$V_{IC} = -15 \text{ V}$			-7	-9.8	
I <sub>IH</sub> (STRB)	High-level strobe input curr	ent	V <sub>(STRB)</sub> = 5.5 V				5	μΑ
I <sub>IL</sub> (STRB)	Low-level strobe input curre	ent	$V_{(STRB)} = 0$			-1	-1.4	mA
r.	Input resistance	Inverting input			3.6	5		kΩ
r <sub>i</sub>	input resistance	Noninverting input			1.8	2.5		kΩ
	Line terminating resistance		T <sub>A</sub> = 25°C		120	170	250	Ω
los	Short-circuit output current		$V_{CC} = 5.5 \text{ V},$	V <sub>O</sub> = 0	-2.8	-4.5	-6.7	mA
			V <sub>IC</sub> = 15 V,	$V_{ID} = -1 V$		4.2	6	
ICC	Supply current (average pe	er receiver)	$V_{IC} = 0$ ,	$V_{ID} = -0.5 V$		6.8	10.2	mA
			$V_{IC} = -15 \text{ V},$	$V_{ID} = -1 V$		9.4	14	

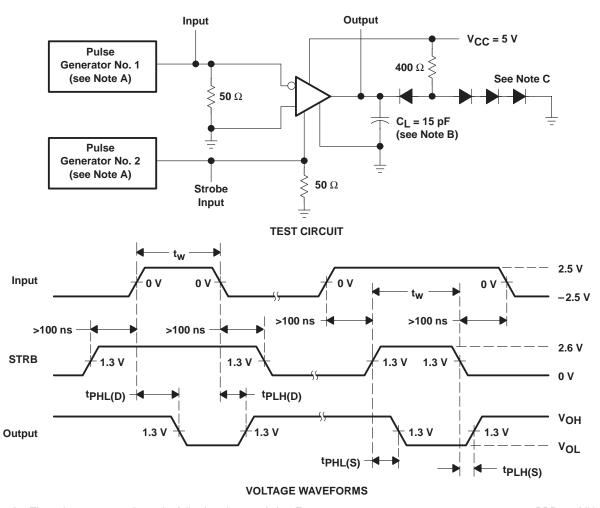
# switching characteristics, $V_{CC} = 5 \text{ V}$ , $T_A = 25^{\circ}\text{C}$

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
tPLH(D)	Propagation delay time, low- to high-level output from differential input			18	40	ns
tPHL(D)	Propagation delay time, high- to low-level output from differential input	$R_L = 400 \Omega,$ $C_L = 15 pF,$ See Figure 1		31	45	ns
tPLH(S)	Propagation delay time, low- to high-level output from STRB input	See Figure 1		9	30	ns
tPHL(S)	Propagation delay time, high- to low-level output from STRB input			15	25	ns



<sup>†</sup> Unless otherwise noted,  $V(STRB) \ge 2.1 \text{ V or open.}$ ‡ All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $V_{IC} = 0$ , and  $T_A = 25 ^{\circ}C$ .

#### PARAMETER MEASUREMENT INFORMATION



NOTES: A. The pulse generators have the following characteristics:  $Z_O = 50~\Omega$ ,  $t_f \le 10~\text{ns}, t_f \le 10~\text{ns}, t_W = 0.5~\pm 0.1~\mu\text{s}, PRR \le 1~\text{MHz}.$ 

- B. C<sub>L</sub> includes probe and jig capacitance.
- C. All diodes are 1N3064 or equivalent.

Figure 1. Test Circuit and Voltage Waveforms

#### TYPICAL CHARACTERISTICS<sup>†</sup>

# **DIFFERENTIAL INPUT THRESHOLD VOLTAGE SUPPLY VOLTAGE** 0.3 V<sub>ID</sub> - Differential Input Threshold Voltage - V $V_{IC} = 0$ T<sub>A</sub> = 25°C 0.2 0.1 $\text{V}_{\mbox{\scriptsize O}}$ = 2.5 V, $\text{I}_{\mbox{\scriptsize O}}$ = $-400~\mu\mbox{\scriptsize A}$ 0 $V_0 = 0.4 \text{ V}, I_0 = 16 \text{ mA}$ -0.1-0.2 -0.35.5 6 4.5

V<sub>CC</sub> - Supply Voltage - V

Figure 2

DIFFERENTIAL INPUT THRESHOLD VOLTAGE

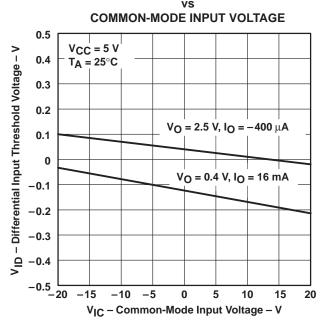


Figure 3

#### **DIFFERENTIAL INPUT THRESHOLD VOLTAGE**

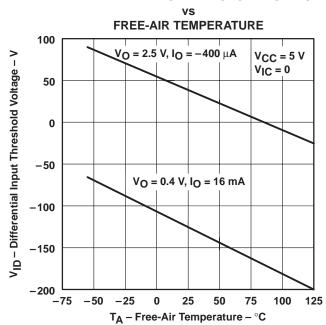


Figure 4

<sup>†</sup> Data for temperatures below 0°C and above 70°C are applicable to SN55182 circuits only.



#### TYPICAL CHARACTERISTICS<sup>†</sup>

# OUTPUT VOLTAGE

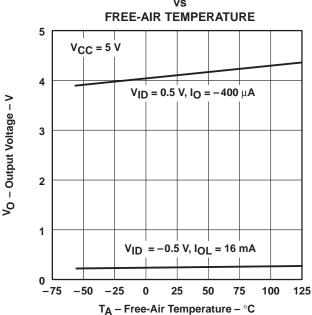
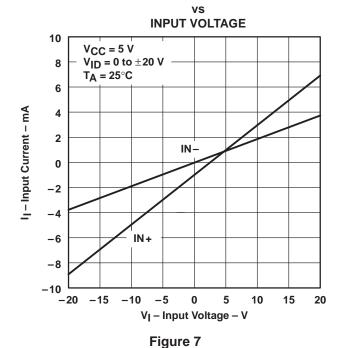


Figure 5

# INPUT CURRENT



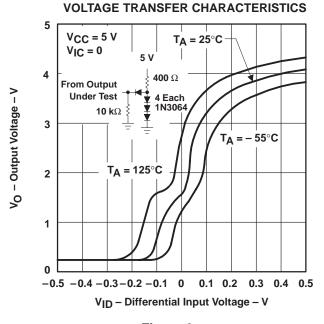


Figure 6

#### **TERMINATING RESISTANCE**

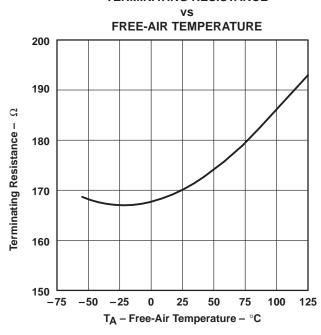
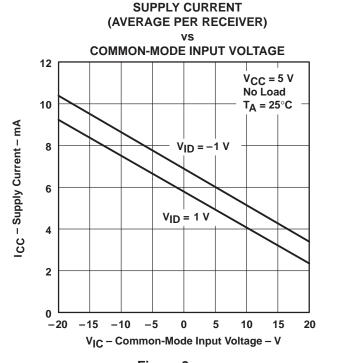


Figure 8

<sup>†</sup> Data for temperatures below 0°C and above 70°C are applicable to SN55182 circuits only.

#### TYPICAL CHARACTERISTICS<sup>†</sup>

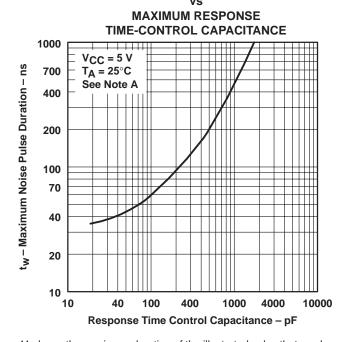


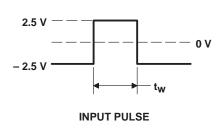
**POWER DISSIPATION** (AVERAGE PER RECEIVER) **COMMON-MODE INPUT VOLTAGE** 300 V<sub>C</sub>C = 5 V  $V_{ID} = -1 V$ 250 Max Rated PD at TA = 125°C P<sub>D</sub> – Power Dissipation – mW (W Package) 200 150 T<sub>A</sub> = 25°C 100 50 T<sub>A</sub> = 125°C -20 -15 -10 0 15 20 V<sub>IC</sub> - Common-Mode Input Voltage - V

Figure 10

Figure 9

MAXIMUM NOISE PULSE DURATION





NOTE A: Figure 11 shows the maximum duration of the illustrated pulse that can be applied differently without the output changing from the low to high level.

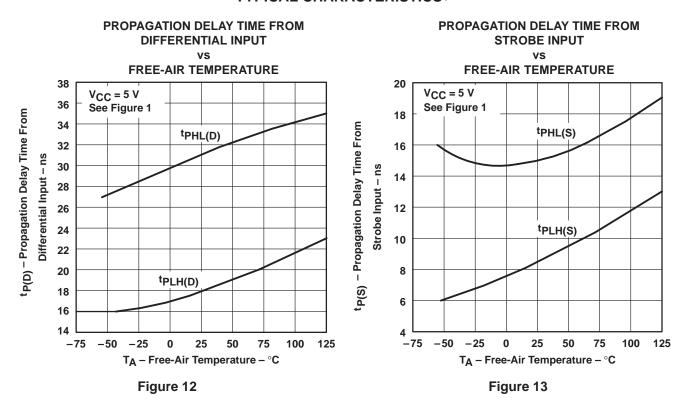
Figure 11

<sup>†</sup> Data for temperatures below 0°C and above 70°C are applicable to SN55182 circuits only.



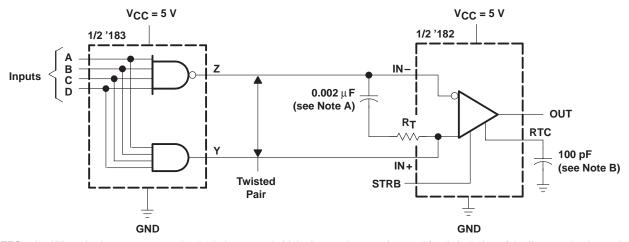
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#### TYPICAL CHARACTERISTICS<sup>†</sup>



† Data for temperatures below 0°C and above 70°C are applicable to SN55182 circuits only.

#### **APPLICATION INFORMATION**



NOTES: A. When the inputs are open circuited, the output is high. A capacitor may be used for dc isolation of the line-terminating resistor. At the frequency of operation, the impedance of the capacitor should be relatively small.

Example: let 
$$f = 5$$
 MHz  $C = 0.002 \, \mu F$  
$$Z_{(C)} = \frac{1}{2\pi f C} = \frac{1}{2\pi \, (5 \, \times \, 10^6) \, (0.002 \, \times \, 10^{-6})}$$
  $Z_{(C)} \approx 16 \, \Omega$ 

B. Use of a capacitor to control response time is optional.

Figure 14. Transmission of Digital Data Over Twisted-Pair Line



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