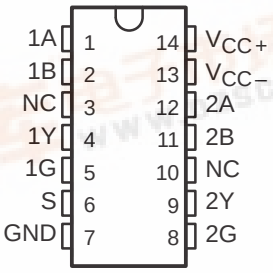
SN75207, SN75207B
DUAL SENSE AMPLIFIER FOR MOS MEMORIES OR DUAL HIGH-SENSITIVITY LINE RECEIVERS

SLLS096B – JULY 1973 – REVISED MAY 1995

- **Plug-In Replacement for SN75107A and SN75107B With Improved Characteristics**
- **±10-mV Input Sensitivity**
- **TTL-Compatible Circuitry**
- **Standard Supply Voltages . . . ±5 V**
- **Differential Input Common-Mode Voltage Range of ±3 V**
- **Strobe Inputs for Channel Selection**
- **Totem-Pole Outputs**
- **SN75207B Has Diode-Protected Input Stage for Power-Off Condition**
- **Sense Amplifier for MOS Memories**
- **Dual Comparator**
- **High-Sensitivity Line Receiver**

D OR N PACKAGE
(TOP VIEW)



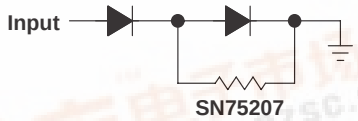
NC – No internal connection

THE SN75207 IS NOT RECOMMENDED FOR NEW DESIGNS.

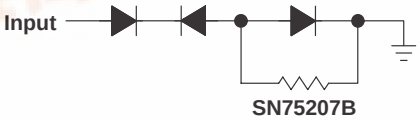
description

The SN75207 and SN75207B are terminal-for-terminal replacements for the SN75107A and SN75107B, respectively. The improved input sensitivity makes them more suitable for MOS memory sense amplifiers and can result in faster memory cycles. Improved sensitivity also makes them more useful in line-receiver applications by allowing use of longer transmission line lengths. The ’207 and ’207B each features a TTL-compatible, active-pullup output.

The essential difference between the SN75207 and SN75207B can be seen in the schematics. Input protection diodes are in series with the collectors of the differential-input transistors of the SN75207B. These diodes are useful in certain party-line systems that may have multiple V_{CC+} power supplies and may be operated with some of the V_{CC+} supplies turned off. In such a system, if a supply is turned off and allowed to go to ground, the equivalent input circuit connected to that supply would be as follows:



SN75207



SN75207B

This would be a problem in specific systems that might have the transmission lines biased to some potential greater than 1.4 V.

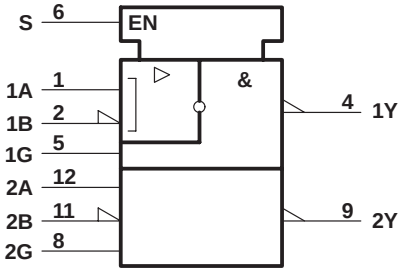
These devices are characterized for operation from 0°C to 70°C.

FUNCTION TABLE

DIFFERENTIAL INPUTS A-B	STROBES G	STROBES S	OUTPUT Y
$V_{ID} \geq 10$ mV	X	X	H
–10 mV < V_{ID} < 10 mV	X	L	H
	L	X	H
	H	H	Indeterminate
$V_{ID} \leq -10$ mV	X	L	H
	L	X	H
	H	H	L

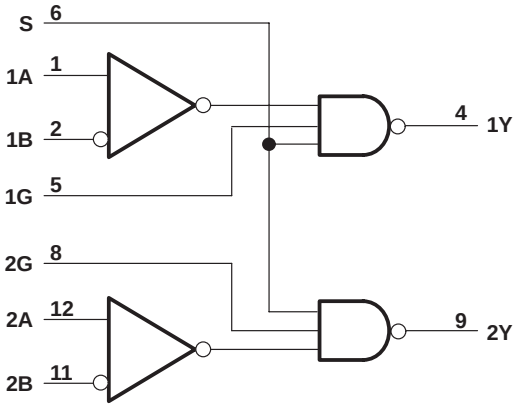
H = high level, L = low level, X = irrelevant

logic symbol†

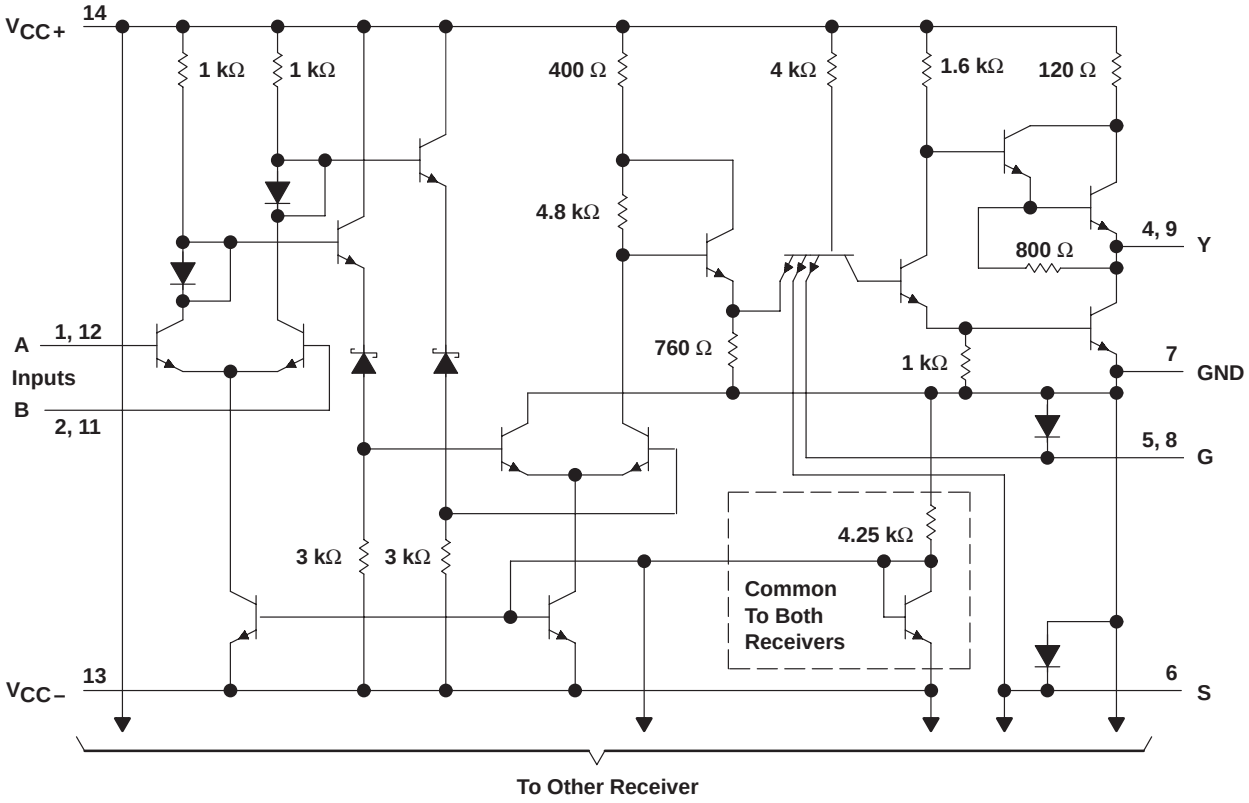


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schematic (each receiver)



Resistor values shown are normal.

design characteristics

The ’207 and ’207B line receivers/sense amplifiers are TTL-compatible, dual circuits intended for use in high-speed, data-transmission systems or MOS memory systems. They are designed to detect low-level differential signals in the presence of common-mode noise and variations of temperature and supplies. The dc specifications reflect worst-case conditions of temperature, supply voltages, and input voltages.

The input common-mode voltage range is ±3 V. This is adequate for application in most systems. In systems with requirements for greater common-mode voltage range, input attenuators may be used to decrease the noise to an acceptable level at the receiver-input terminals.

The circuits feature individual strobe inputs for each channel and a strobe input common to both channels for logic versatility. The strobe inputs are tested to ensure 400 mV of dc noise margin when interfaced with Series 54/74 TTL.

The circuits feature high input impedance and low input currents, which induce very little loading on the transmission line. This makes these devices especially useful in party-line systems. The excellent input sensitivity (3 mV typical) is particularly important when data is to be detected at the end of a long transmission line and the amplitude of the data has deteriorated due to cable losses. The circuits are designed to detect input signals of 10-mV (or greater) amplitude and convert the polarity of the signal into appropriate TTL-compatible output logic levels.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC+} (see Note 1) . . . . . 7 V
Supply voltage, V_{CC-} (see Note 1) . . . . . –7 V
Differential input voltage, V_{ID} (see Note 2) . . . . . ±6 V
Common-mode input voltage, V_{IC} (see Note 3) . . . . . ±5 V
Strobe input voltage . . . . . 5.5 V
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to GND terminal.
2. Differential input voltage values are at the noninverting (A) terminal with respect to the inverting (B) terminal.
3. Common-mode input voltage is the average of the voltages at the A and B inputs.

DISSIPATION RATING TABLE

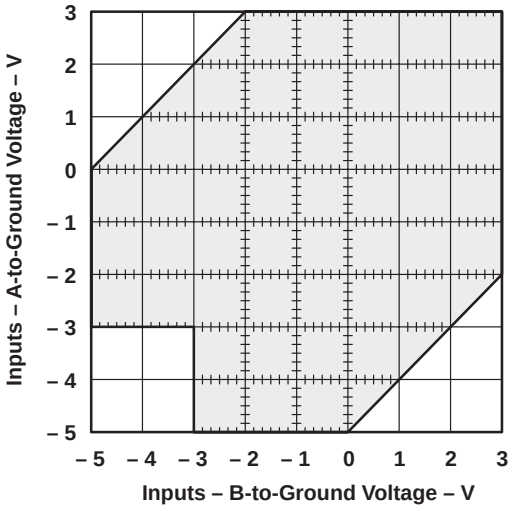
PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW
N	1050 mW	9.2 mW/°C	636 mW

recommended operating conditions (see Note 4)

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC+}	4.75	5	5.25	V
Supply voltage, V_{CC-}	–4.75	–5	–5.25	V
High-level differential input voltage, $V_{ID(H)}$ (see Note 5)	0.01		5	V
Low-level differential input voltage, $V_{ID(L)}$	–5†		–0.01	V
Common-mode input voltage, V_{IC} (see Notes 5 and 6)	–3†		3	V
Input voltage, any differential input to ground (see Note 5)	–5†		3	V
High-level input voltage at strobe inputs, $V_{IH(S)}$	2		5.5	V
Low-level input voltage at strobe inputs, $V_{IL(S)}$	0		0.8	V
Low-level output current, I_{OL}			–16	mA
Operating free-air temperature, T_A	0		70	°C

† The algebraic convention, in which the less positive (more negative) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

NOTES: 4. When using only one channel of the line receiver, the strobe G of the unused channel should be grounded and at least one of the differential inputs of the unused receiver should be terminated at some voltage between –3 V and 3 V.
5. The recommended combinations of input voltages fall within the shaded area of the figure shown.
6. The common-mode voltage may be as low as –4 V provided that the more positive of the two inputs is not more negative than –3 V.



electrical characteristics over recommended free-air temperature range (unless otherwise noted)

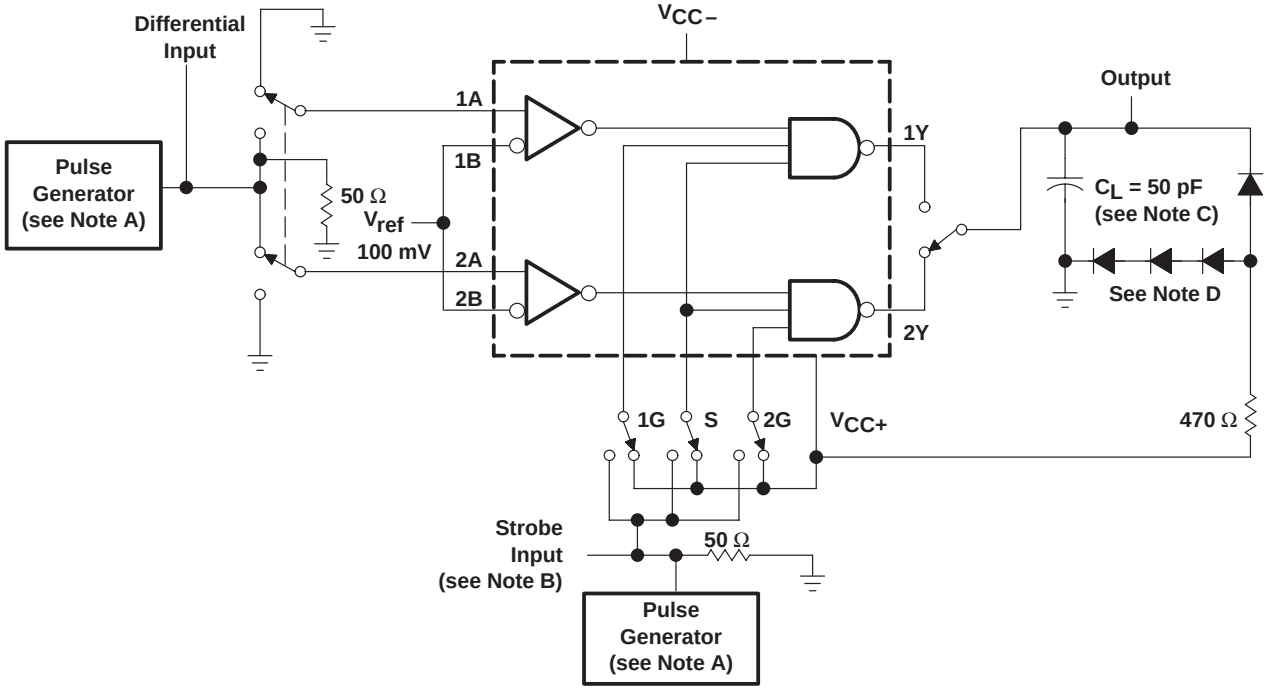
PARAMETER			TEST CONDITIONS			MIN	TYP†	MAX	UNIT
I_{IH}	High-level input current	'207	$V_{CC\pm}$ = ± 5.25 V		V_{ID} = 5 V		30	75	µA
		'207B			V_{ID} = –5 V		30	75	
I_{IL}	Low-level input current	'207	$V_{CC\pm}$ = ± 5.25 V		V_{ID} = –5 V			–10	µA
		'207B			V_{ID} = 5 V			–10	
I_{IH}	High-level input current into 1G or 2G		$V_{CC\pm}$ = ± 5.25 V,	$V_{IH(S)}$ = 2.4 V				40	µA
			$V_{CC\pm}$ = ± 5.25 V,	$V_{IH(S)}$ = ± 5.25 V				1	mA
I_{IL}	Low-level input current into 1G or 2G		$V_{CC\pm}$ = ± 5.25 V,	$V_{IL(S)}$ = 0.4 V				–1.6	mA
I_{IH}	High-level input current into S		$V_{CC\pm}$ = ± 5.25 V,	$V_{IH(S)}$ = 2.4 V				80	µA
			$V_{CC\pm}$ = ± 5.25 V,	$V_{IH(S)}$ = ± 5.25 V				2	mA
I_{IL}	Low-level input current into S		$V_{CC\pm}$ = ± 5.25 V,	$V_{IL(S)}$ = 0.4 V				–3.2	mA
V_{OH}	High-level output voltage		$V_{CC\pm}$ = ± 4.75 V, I_{OH} = –400 µA,	$V_{IL(S)}$ = 0.8 V, V_{IC} = –3 V to 3 V	$V_{ID(H)}$ = 10 mV,	2.4			V
V_{OL}	Low-level output voltage		$V_{CC\pm}$ = ± 4.75 V, I_{OL} = 16 mA,	$V_{IH(S)}$ = 2 V, V_{IC} = –3 V to 3 V	$V_{ID(L)}$ = –10 mV,			0.4	V
I_{OH}	High-level output current		$V_{CC\pm}$ = ± 4.75 V,	V_{OH} = ±5.25 V				400	µA
I_{OS}	Short-circuit output current‡		$V_{CC\pm}$ = ± 5.25 V			–18		–70	mA
I_{CC+}	Supply current from V_{CC+}		$V_{CC\pm}$ = ± 5.25 V,	T_A = 25°C,	Outputs high		18	30	mA
I_{CC-}	Supply current from V_{CC-}		$V_{CC\pm}$ = ± 5.25 V,	T_A = 25°C,	Outputs high		–8.4	–15	mA

† All typical values are at V_{CC+} = 5 V, V_{CC-} = –5 V, T_A = 25°C.
‡ Not more than one output should be shorted at a time.

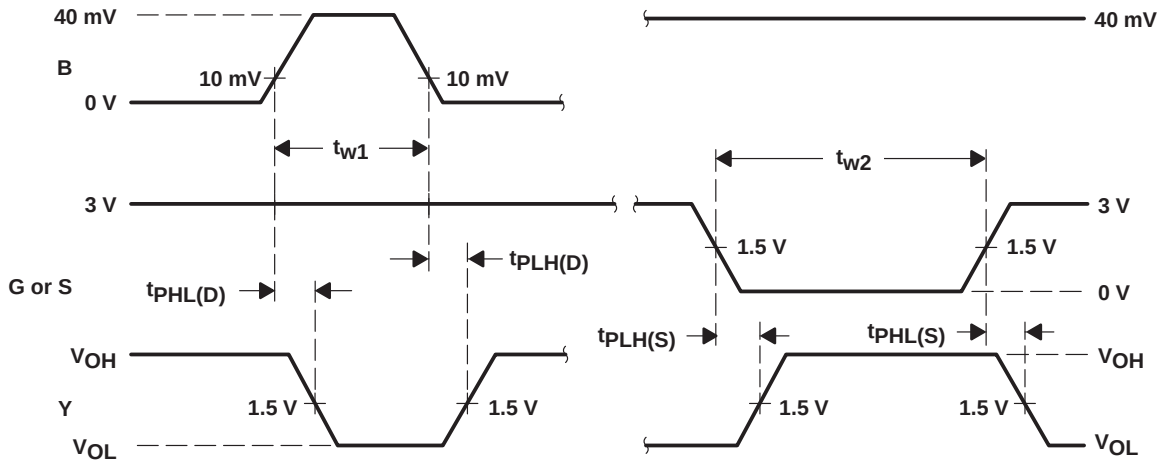
switching characteristics, V_{CC+} = 5 V, V_{CC-} = –5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$t_{PLH(D)}$	Propagation delay time, low- to high-level output, from differential inputs A and B	R_L = 470 Ω, C_L = 50 pF, See Figure 1		35	ns
$t_{PHL(D)}$	Propagation delay time, high- to low-level output, from differential inputs A and B			20	ns
$t_{PLH(S)}$	Propagation delay time, low- to high-level output, from strobe input G or S			17	ns
$t_{PHL(S)}$	Propagation delay time, high- to low-level output, from strobe input G or S			17	ns

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generators have the following characteristics: Z_O = 50 Ω, $t_r \le 5$ ns, $t_f \le 5$ ns, t_{w1} = 500 ns with PRR = 1 MHz, t_{w2} = 1 µs with PRR = 500 kHz.
B. Strobe input pulse is applied to Strobe 1G when inputs 1A-1B are being tested, to Strobe S when inputs 1A-1B or 2A-2B are being tested, and to Strobe 2G when inputs 2A-2B are being tested.
C. C_L includes probe and jig capacitance.
D. All diodes are 1N916.

Figure 1. Test Circuit and Voltage Waveforms

APPLICATION INFORMATION

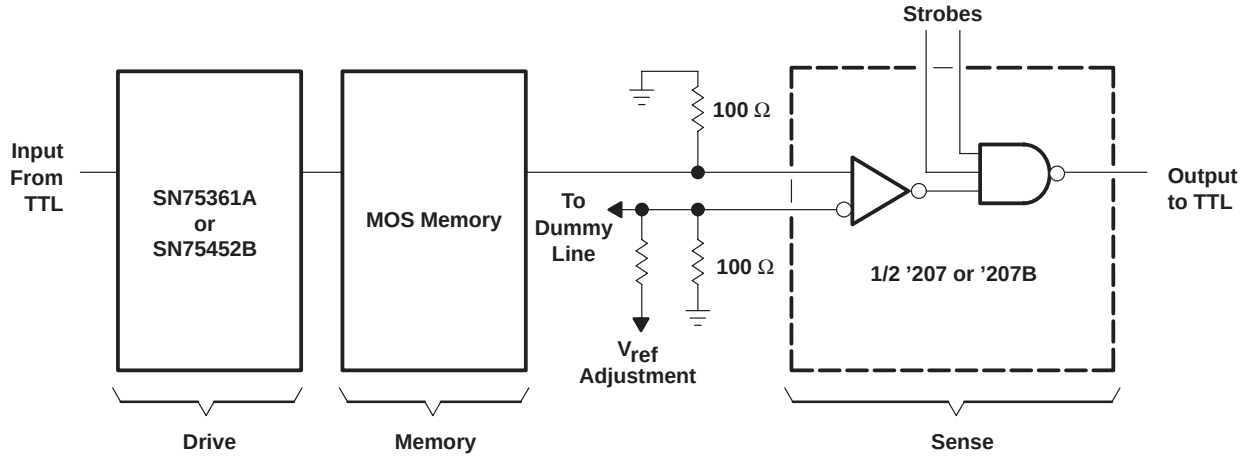
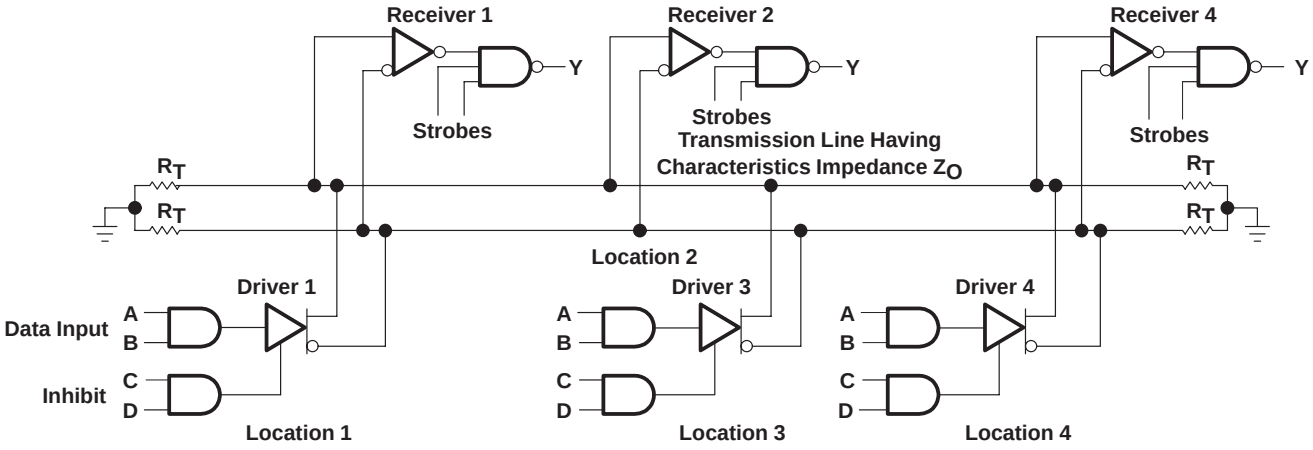


Figure 2. Mos Memory Sense Amplifier



Receivers are '207 or '207B; drivers are SN55109A, SN75109A, SN55110A, SN75110A, or SN75112.

Figure 3. Data-Bus or Parity-Line System

PRECAUTIONS: When only one receiver in a package is being used, at least one of the differential inputs of the unused receiver should be terminated at some voltage between –3 V and 3 V, preferably at GND. Failure to do so will cause improper operation of the unit being used because of common bias circuitry for the current sources of the two receivers. Strobe G of the unused channel should be grounded.

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