



ISO 9001 Registered

IMP5219

9-Line SCSI Terminator

DESCRIPTION

The IMP5219 SCSI terminator is part of IMP's SCSI terminator family of high-performance, adaptive, non-linear mode SCSI products, which are designed to deliver true UltraSCSI performance in SCSI applications. The low voltage BiCMOS architecture employed in its design offers performance superior to older linear passive and active techniques. IMP's SCSI terminator architecture employs high-speed adaptive elements for each channel, thereby providing the fastest response possible — typically 35MHz, which is 100 times faster than the older linear regulator/terminator approach used by other manufacturers. Products using this older linear regulator approach have bandwidths which are dominated by the output capacitor and which are limited to 500KHz (see further discussion in the Functional Description section). This new architecture also eliminates the output compensation capacitor required in earlier terminator designs. Each is approved for use with SCSI-1, -2, -3, UltraSCSI and beyond — providing the highest performance alternative available today.

Another key improvement offered by the IMP5219 lies in its ability to insure reliable, error-free communications even in systems which do not adhere to recommended SCSI hardware design guidelines, such as the use of improper cable lengths and impedances. Frequently, this situation is not

controlled by the peripheral or host designer and, when problems occur, they are the first to be made aware of the problem. The IMP5219 architecture is much more tolerant of marginal system integrations.

Recognizing the needs of portable and configurable peripherals, the IMP5219 has an active high TTL compatible sleep/disable mode. Quiescent current is typically less than 275µA in this mode, while the output capacitance is also less than 3pF. The obvious advantage of extended battery life for portable systems is inherent in the product's sleep-mode feature. Additionally, the disable function permits factory-floor or production-line configurability, reducing inventory and product-line diversity costs. Field configurability can also be accomplished without physically removing components which results in field returns due to mishandling.

Reduced component count is also inherent in the IMP5219 architecture. Traditional termination techniques require large stabilization and transient protection capacitors of up to 20µF in value and size. The IMP5219 architecture does not require these components, allowing all the cost savings associated with reduced inventory, board space, and assembly, plus higher reliability.

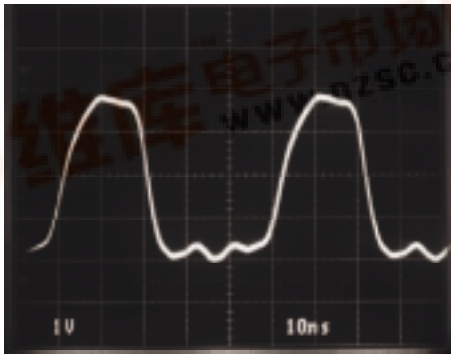
See the IMP5218 for a 9-channel Plug and Play SCSI terminator.

KEY FEATURES

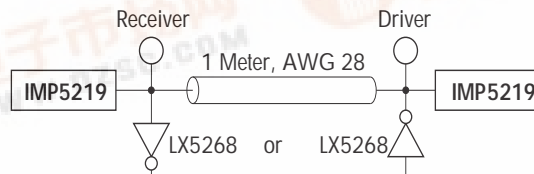
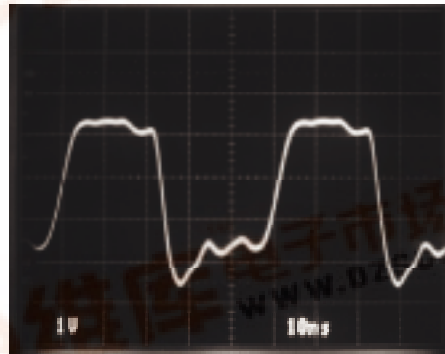
- ULTRA-FAST RESPONSE FOR FAST-20 SCSI APPLICATIONS
- HOT SWAP COMPATIBLE
- 35MHz CHANNEL BANDWIDTH
- 3.5V OPERATION
- LESS THAN 3pF OUTPUT CAPACITANCE
- SLEEP-MODE CURRENT LESS THAN 275µA
- THERMALLY SELF LIMITING
- NO EXTERNAL COMPENSATION CAPACITORS
- IMPLEMENTS 8-BIT OR 16-BIT (WIDE) APPLICATIONS
- COMPATIBLE WITH ACTIVE NEGATION DRIVERS (60mA / CHANNEL)
- COMPATIBLE WITH PASSIVE AND ACTIVE TERMINATIONS
- APPROVED FOR USE WITH SCSI 1, 2, 3 AND ULTRASCSI

PRODUCT HIGHLIGHT

RECEIVING WAVEFORM - 20MHZ



DRIVING WAVEFORM - 20MHZ



PACKAGE ORDER INFORMATION

T _j (°C)	DW Plastic SOWB 16-pin	PW Plastic TSSOP 20-pin
0 to 125	IMP5219CDW	IMP5219CPW

Note: All surface-mount packages are available in Tape & Reel. Append the letter "T" to part number. (i.e. IMP5219CDWT)



ABSOLUTE MAXIMUM RATINGS (Note 1)

Continuous Termination Voltage	10V
Continuous Output Voltage Range	0 to 5.5V
Continuous Disable Voltage Range	0 to 5.5V
Operating Junction Temperature	0°C to 125°C
Storage Temperature Range	-65°C to +150°C
Solder Temperature (Soldering, 10 seconds)	300°C

Note 1. Exceeding these ratings could cause damage to the device.

THERMAL DATA

DW PACKAGE:

THERMAL RESISTANCE-JUNCTION TO AMBIENT, θ_{JA} 95°C/W

PW PACKAGE:

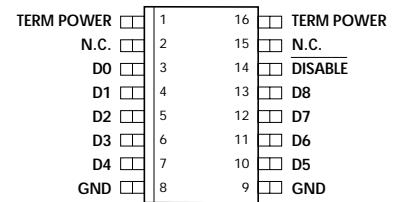
THERMAL RESISTANCE-JUNCTION TO AMBIENT, θ_{JA} 144°C/W

Junction Temperature Calculation: $T_j = T_A + (P_D \times \theta_{JA})$.

The θ_{JA} numbers are guidelines for the thermal performance of the device/pc-board system.

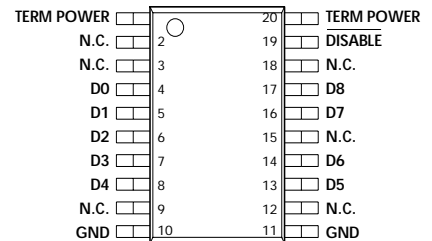
All of the above assume no ambient airflow.

PACKAGE PIN OUTS



DW PACKAGE

(Top View)



PW PACKAGE

(Top View)

RECOMMENDED OPERATING CONDITIONS (Note 2)

Parameter	Symbol	Recommended Operating Conditions			Units
		Min.	Typ.	Max.	
Termination Voltage	V_{TERM}	3.5		5.5	V
High Level Disable Input Voltage	V_{IH}	2		V_{TERM}	V
Low Level Disable Input Voltage	V_{IL}	0		0.8	V
Operating Virtual Junction Temperature Range		0		125	°C

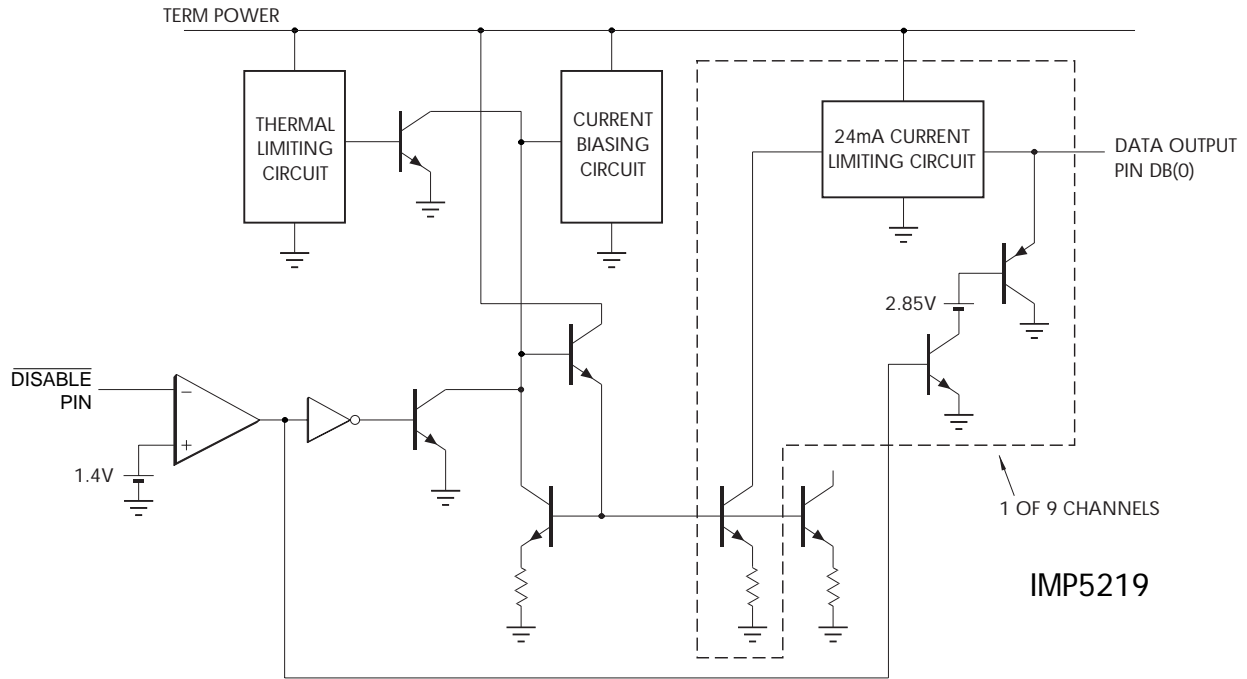
Note 2. Range over which the device is functional.

ELECTRICAL CHARACTERISTICS

Term Power = 4.75V unless otherwise specified. Unless otherwise specified, these specifications apply at the recommended operating ambient temperature of $T_A = 25^\circ\text{C}$. Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.

Parameter	Symbol	Test Conditions	IMP5219			Units
			Min.	Typ.	Max.	
Output High Voltage	V_{OUT}		2.65	2.85		V
TermPwr Supply Current	I_{CC}	All data lines = open		6	9	mA
		All data lines = 0.5V		215	225	mA
		Disable < 0.8V		375		μA
Output Current	I_{OUT}	$V_{OUT} = 0.5V$	-21	-23	-24	mA
Disable Input Current	I_{IN}	Disable = 4.75V		10		nA
		Disable = 0V		-90		μA
Output Leakage Current		Disable = < 0.8V, $V_O = 0.5V$		10		nA
Capacitance in Disabled Mode	C_{OUT}	$V_{OUT} = 0V$, frequency = 1MHz		3		pF
Channel Bandwidth	BW			35		MHz
Termination Sink Current, per Channel	I_{SINK}	$V_{OUT} = 4V$		60		mA

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

Cable transmission theory suggests to optimize signal speed and quality, the termination should act both as an ideal voltage reference when the line is released (deasserted) and as an ideal current source when the line is active (asserted). Common active terminators, which consist of Linear Regulators in series with resistors (typically 110Ω), are a compromise. As the line voltage increases, the amount of current decreases linearly by the equation $V = I * R$. The IMP5219, with its unique new architecture applies the maximum amount of current regardless of line voltage until the termination high threshold (2.85V) is reached.

Acting as a near ideal line terminator, the IMP5219 closely reproduces the optimum case when the device is enabled. To enable the device the Disable Pin must be pulled logic **High** or left **Open**. During this mode of operation, quiescent current is

6mA and the device will respond to line demands by delivering 24mA on assertion and by imposing 2.85V on deassertion. In order to disable the device, the Disable pin must be driven logic **Low**. This mode of operation places the device in a sleep state where a meager 275μA of quiescent current is consumed. Additionally, all outputs are in a Hi-Z (impedance) state. Sleep mode can be used for power conservation or to completely eliminate the terminator from the SCSI chain. In the second case, termination node capacitance is important to consider. The terminator will appear as a parasitic distributed capacitance on the line, which can detract from bus performance. For this reason, the IMP5219 has been optimized to have only 3pF of capacitance per output in the

sleep state.

An additional feature of the IMP5219 is its compatibility with active negation drivers. The device handles up to 60mA of sink current for drivers which exceed the 2.85V output **High**.

POWER UP / POWER DOWN FUNCTION TABLE

Disable	Outputs	Quiescent Current
H	Enabled	6mA
L	HI Z	375μA
Open	Enabled	6mA

GRAPH / CURVE INDEX

Waveforms

FIGURE

- 1A. RECEIVING WAVEFORM (Freq. = 1.0MHz)
- 1B. DRIVING WAVEFORM
- 2A. RECEIVING WAVEFORM (Freq. = 5.0MHz)
- 2B. DRIVING WAVEFORM
- 3. 10MHz WAVEFORM
- 4. 20MHz WAVEFORM

Characteristic Curves

FIGURE

- 5. OUTPUT HIGH VOLTAGE vs. JUNCTION TEMPERATURE
- 6. OUTPUT CURRENT vs. JUNCTION TEMPERATURE
- 7. OUTPUT CURRENT vs. OUTPUT HIGH VOLTAGE ($V_T = 4.75V$)
- 8. OUTPUT CURRENT vs. OUTPUT HIGH VOLTAGE ($V_T = 3.3V$)
- 9. TERMINATION VOLTAGE vs. SUPPLY CURRENT
- 10. TERMPWR SUPPLY CURRENT vs. TERMINATION VOLTAGE (Disabled)
- 11. OUTPUT HIGH VOLTAGE vs. JUNCTION TEMPERATURE ($V_T = 3.3V$)
- 12. OUTPUT CURRENT vs. JUNCTION TEMPERATURE ($V_T = 3.3V$)
- 13. OUTPUT HIGH VOLTAGE vs. TERMINATION VOLTAGE
- 14. OUTPUT CURRENT vs. TERMINATION VOLTAGE
- 15. OUTPUT CURRENT MATCHING CHANNEL TO CHANNEL

FIGURE INDEX

Application Circuits

FIGURE

- 16. 8-BIT SCSI SYSTEM APPLICATION

CHARACTERISTIC CURVES

FIGURE 1A. — RECEIVING WAVEFORM

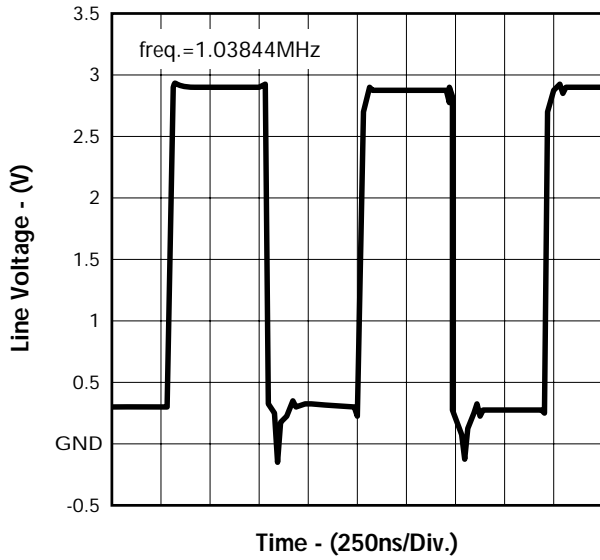
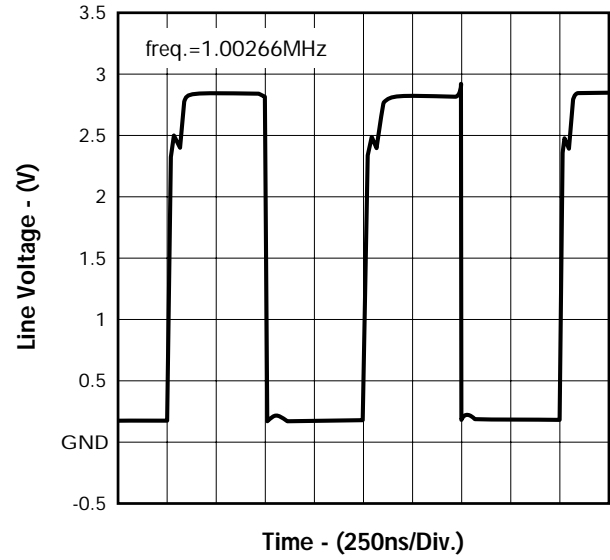
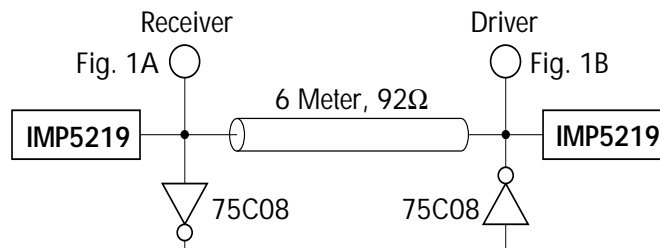


FIGURE 1B. — DRIVING WAVEFORM



END-DRIVEN CABLE



CHARACTERISTIC CURVES

FIGURE 2A. — RECEIVING WAVEFORM

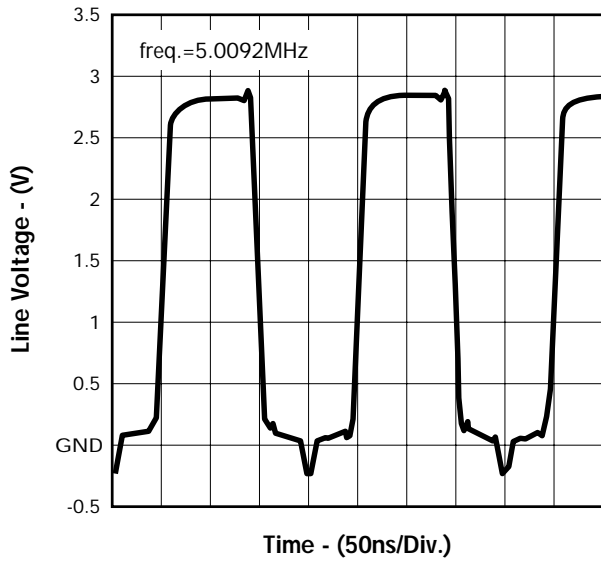
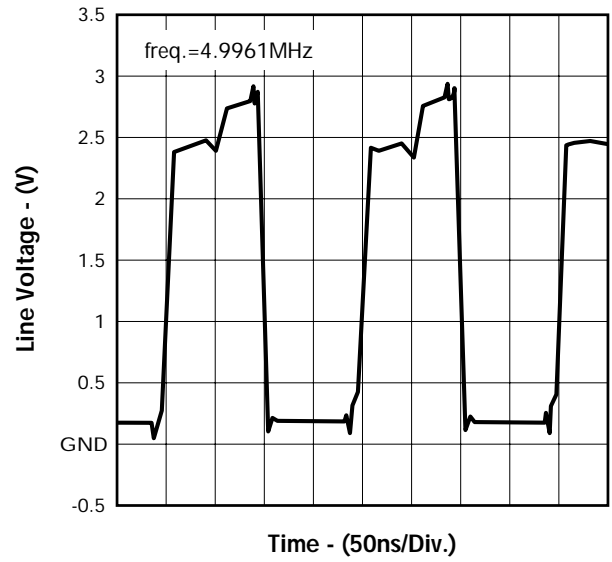
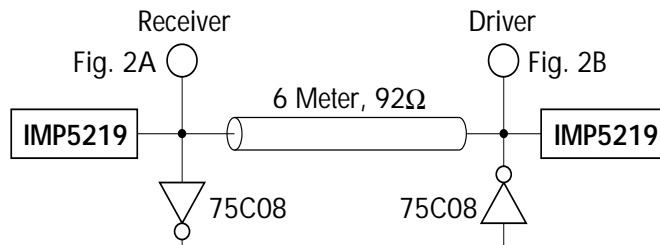


FIGURE 2B. — DRIVING WAVEFORM



END-DRIVEN CABLE



CHARACTERISTIC CURVES

FIGURE 3. — 10MHz WAVEFORM

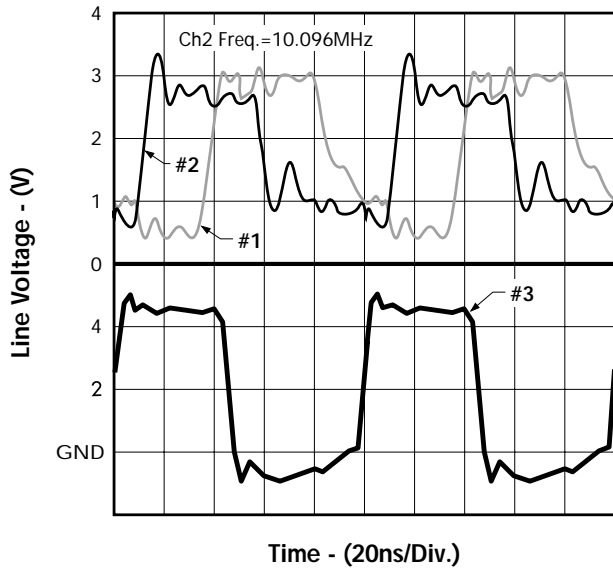
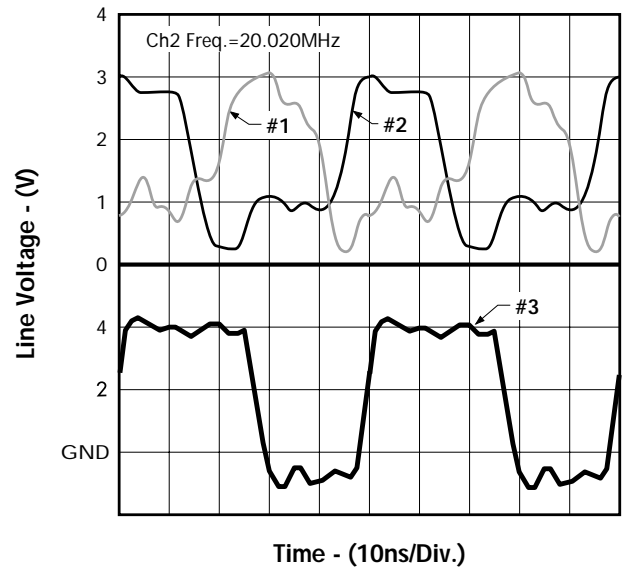
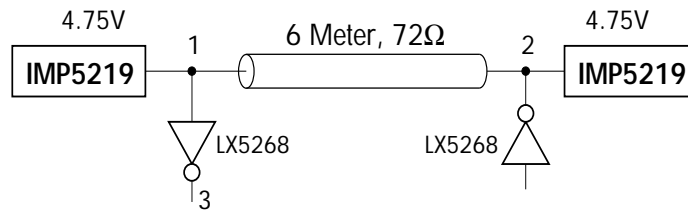


FIGURE 4. — 20MHz WAVEFORM



END-DRIVEN CABLE



CHARACTERISTIC CURVES

FIGURE 5. — OUTPUT HIGH VOLTAGE vs. JUNCTION TEMP.

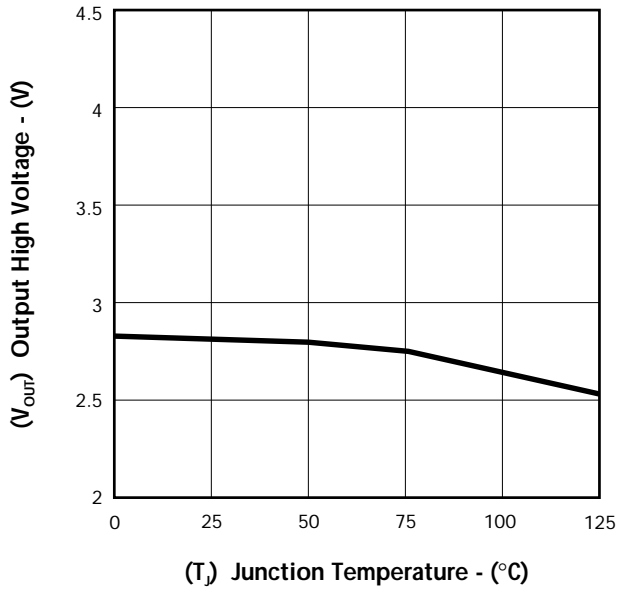


FIGURE 6. — OUTPUT CURRENT vs. JUNCTION TEMP.

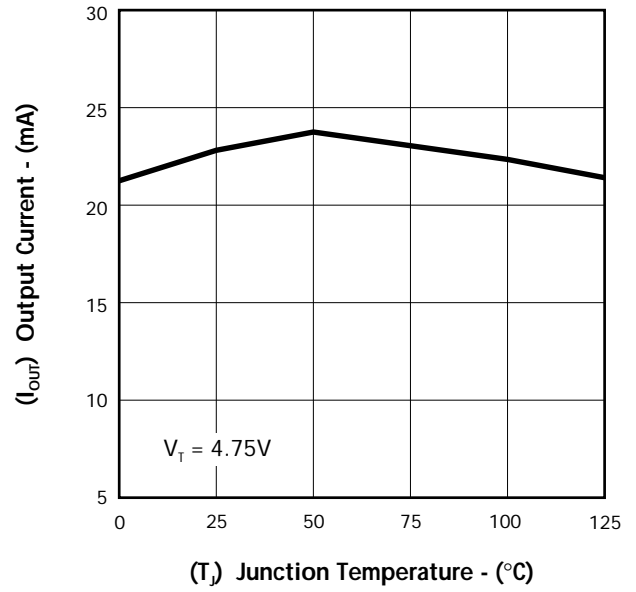


FIGURE 7. — OUTPUT CURRENT vs. OUTPUT HIGH VOLTAGE

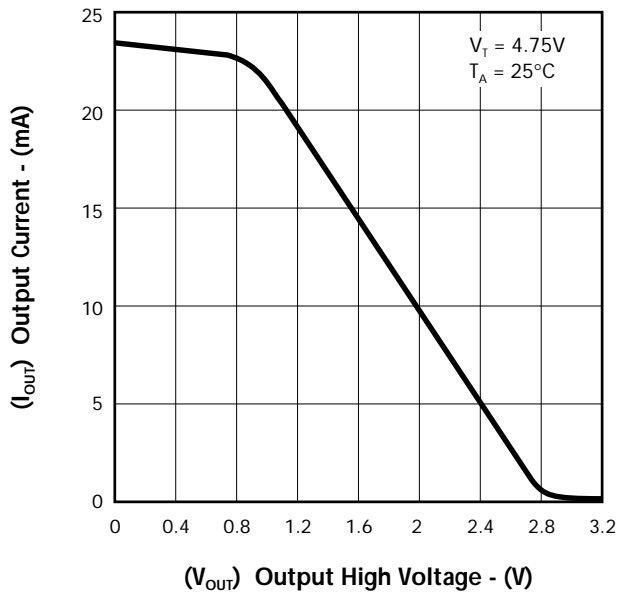
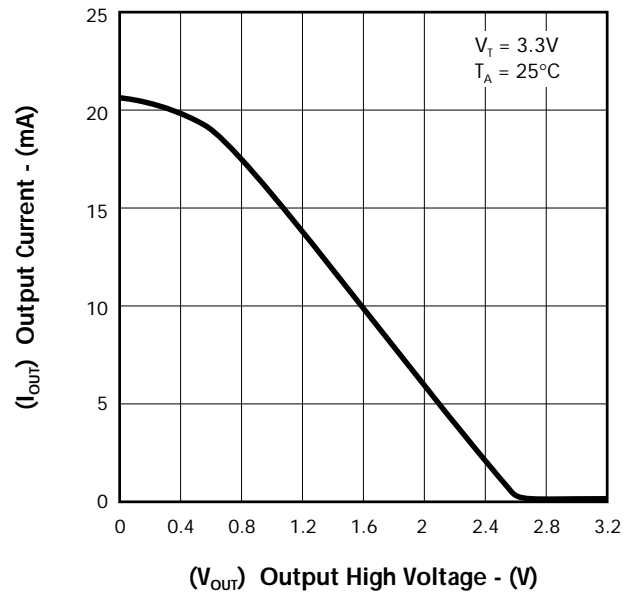


FIGURE 8. — OUTPUT CURRENT vs. OUTPUT HIGH VOLTAGE



CHARACTERISTIC CURVES

FIGURE 9. — TERMPWR SUPPLY CURRENT vs. TERMINATION VOLTAGE

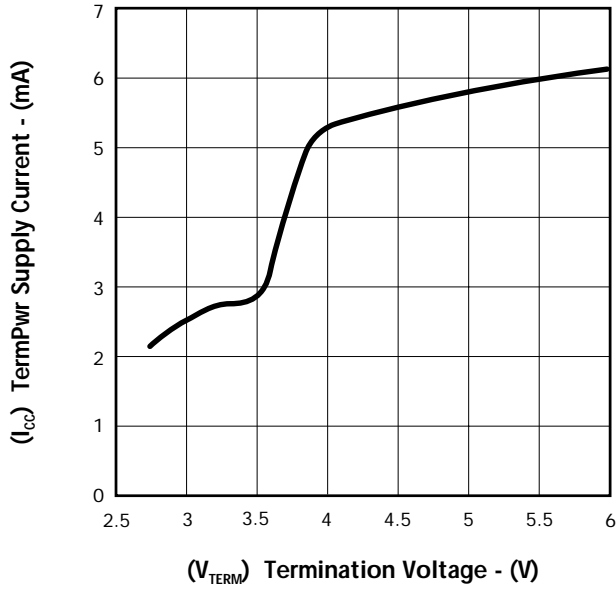


FIGURE 10. — TERMPWR SUPPLY CURRENT vs. TERMINATION VOLTAGE (Disabled)

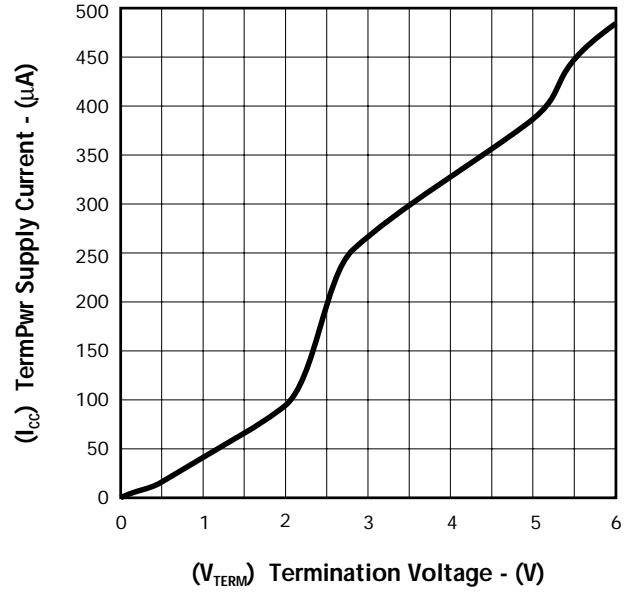


FIGURE 11. — OUTPUT HIGH VOLTAGE vs. JUNCTION TEMP.

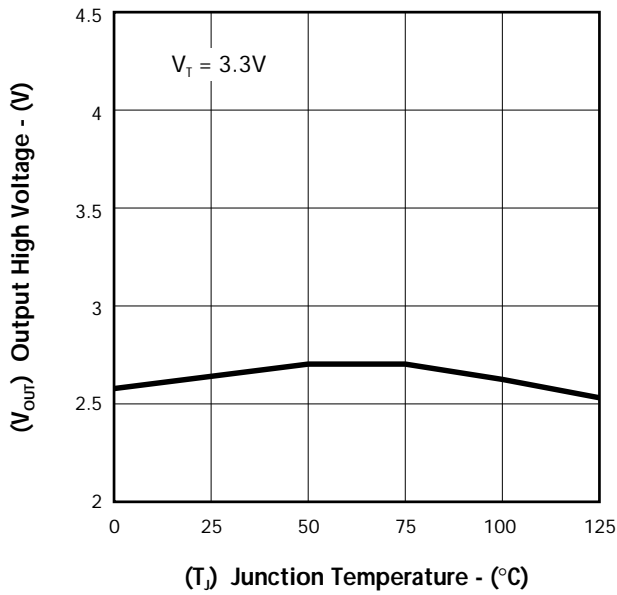
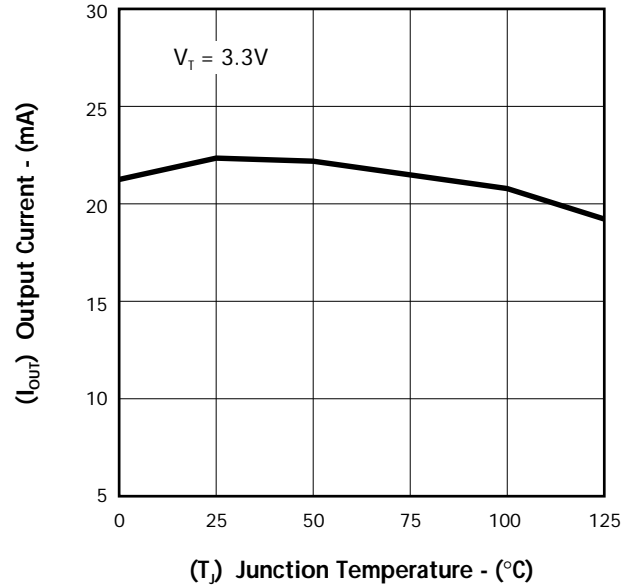


FIGURE 12. — OUTPUT CURRENT vs. JUNCTION TEMP.



CHARACTERISTIC CURVES

FIGURE 13. — OUTPUT HIGH VOLTAGE vs. TERMINATION VOLTAGE

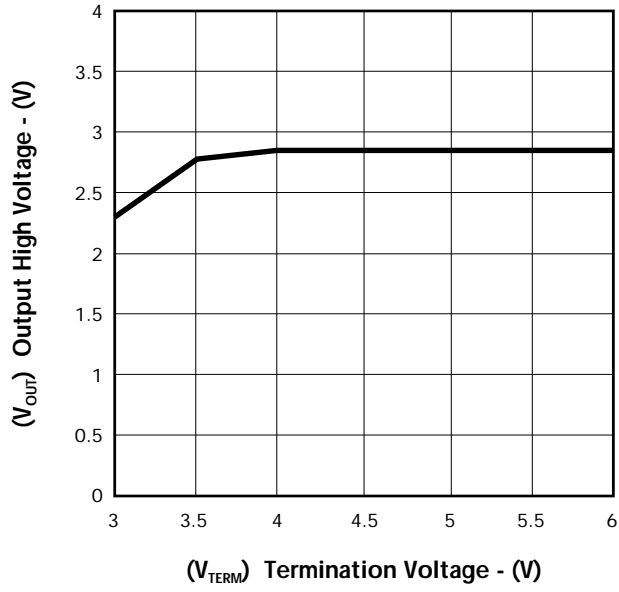
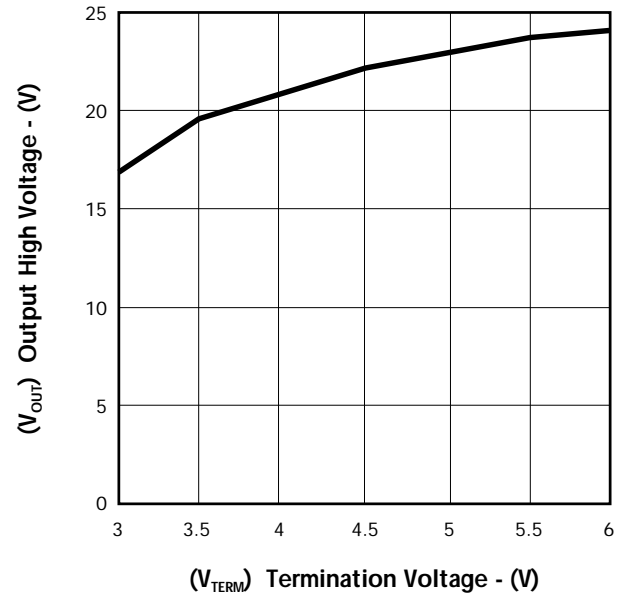
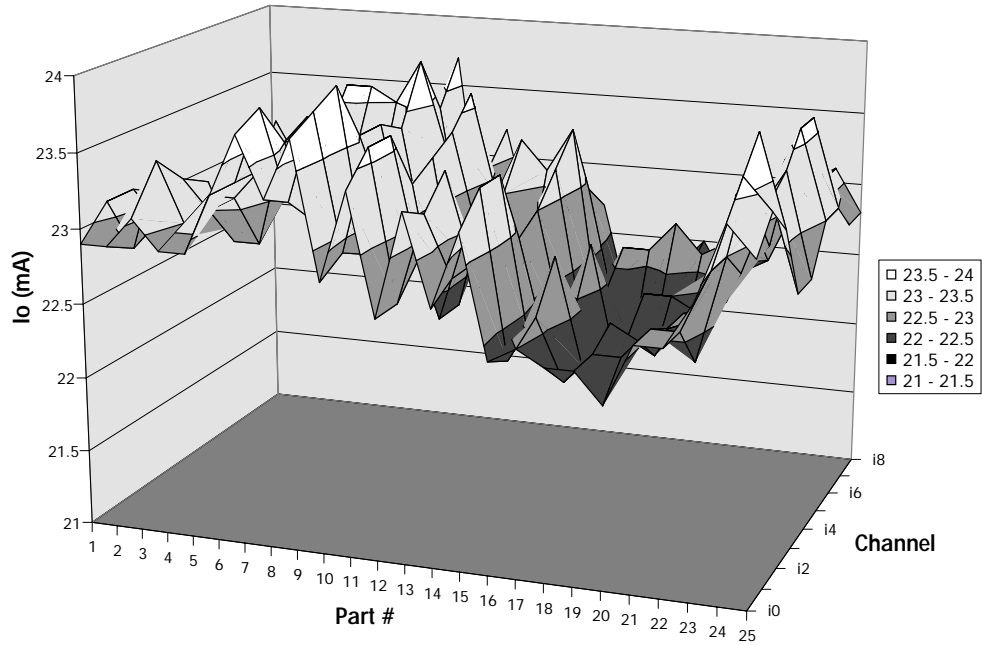


FIGURE 14. — OUTPUT CURRENT vs. TERMINATION VOLTAGE



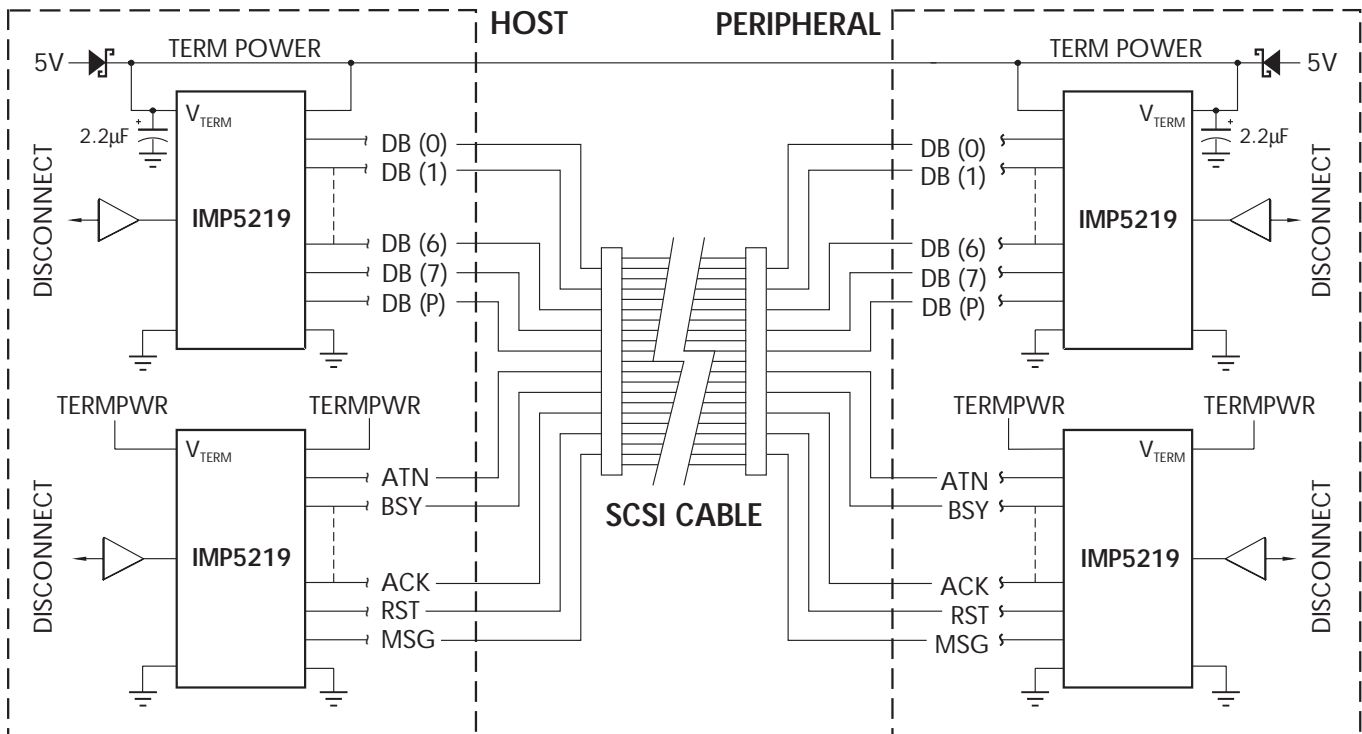
CHARACTERISTIC CURVES

FIGURE 16. — OUTPUT CURRENT CHANNEL TO CHANNEL MATCHING



APPLICATION SCHEMATIC

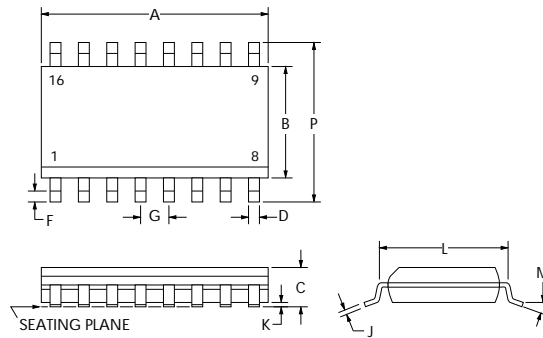
FIGURE 17 — 8-BIT SCSI SYSTEM APPLICATION



Note: Add third IMP5219 for 16-bit SCSI

PACKAGE DIMENSIONS

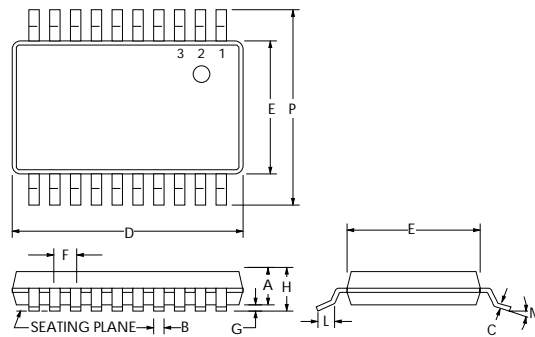
DW 16-Pin Plastic (SOWB)
Widebody S.O.I.C.



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	10.67	—	0.420
B	7.49	7.75	0.295	0.305
C	2.35	2.65	0.093	0.104
D	0.25	0.46	0.010	0.018
F	0.64	0.89	0.025	0.035
G	1.27 BSC		0.050 BSC	
J	0.23	0.32	0.009	0.013
K	0.10	0.30	0.004	0.012
L	8.13	8.64	0.320	0.340
M	0°		8°	
P	10.26	10.65	0.404	0.419

* See NOTE: 1

PWP 20-Pin Thin Small Shrink
Outline (TSSOP)



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	0.90	—	0.354
B	0.18	0.30	0.0071	0.0118
C	0.90	0.180	0.0035	0.0071
D	6.40	6.60	0.252	0.260
E	4.30	4.48	0.169	0.176
F	0.65 BSC		0.025 BSC	
G	0.05	0.15	0.002	0.005
H	—	1.10	—	0.0433
L	0.50	0.70	0.020	0.028
M	0°		8°	
P	6.25	6.50	0.246	0.256



ISO 9001 Registered

IMP, Inc.
Corporate Headquarters
2830 N. First Street
San Jose, CA 95134
Tel: 408.432.9100 Main
Tel: 800.438.3722
Fax: 408.434.0335
Fax-on-Demand: 800.249.1614 (USA)
Fax-on-Demand: 303.575.6156 (International)
e-mail: info@impinc.com
<http://www.impweb.com>

The IMP logo is a registered trademark of IMP, Inc.
All other company and product names are trademarks of their respective owners.

© 1997 IMP, Inc.
Printed in USA
Part No.: IMP5219
Document Number: IMP5219-02-10/97