ISO 9001 Registered

IMP5225

18-Line SCSI Terminator

DESCRIPTION

The IMP5225 SCSI terminator is part of IMP's family of high-performance, adaptive, non-linear mode SCSI products, which are designed to deliver true UltraSCSI performance in SCSI applications. The low voltage BiCMOS architecture employed in its design offers superior performance to older linear passive and active techniques. IMP's new architecture employs high-speed adaptive elements for each channel, thereby providing the fastest response possible — typically 35MHz, which is 100 times faster than the older linear regulator/terminator approach used by other manufacturers. Products using this older linear regulator approach have bandwidths which are dominated by the output capacitor and which are limited to 500KHz (see further discussion in the Functional Description section). The IMP architecture also eliminates the output compensation capacitor required in earlier terminator designs. Each is approved for use with SCSI-1, -2, -3, UltraSCSI and beyond — providing the highest performance alternative available today.

The IMP5225 architecture is much more tolerant of marginal system integrations. A key improvement offered by the IMP5225 lies in its ability to insure reliable, error-free communications even in systems which do not adhere to recommended SCSI hardware design guidelines, such as the use of improper cable lengths and impedances. Frequently, this situation is not controlled by the peripheral or host designer and, when problems occur, they are the first to be made aware of the problem.

Quiescent current is typically less than (375µA) in this mode, while the output capacitance is also less than 4pF.

Reduced component count is also inherent in the IMP5225 architecture. Traditional termination techniques require large stabilization and transient protection capacitors of up to 20µF in value and size. The IMP5225 architecture does not require these components, allowing all the cost savings associated with inventory, board space, assembly, reliability, and component costs.

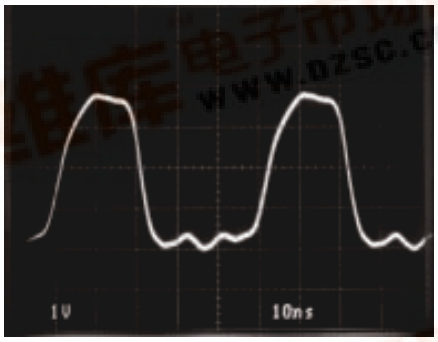
The IMP5225 is a superior pin-for-pin replacement for the LX5205, UC5607/5611/5617 or the DS2109.

KEY FEATURES

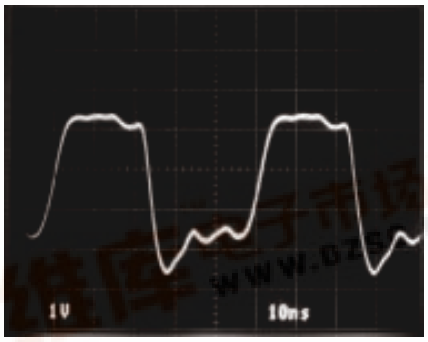
- ULTRA-FAST RESPONSE FOR FAST-20 SCSI APPLICATIONS
- 35MHz CHANNEL BANDWIDTH
- 3.5V OPERATION
- LESS THAN 4pF OUTPUT CAPACITANCE
- SLEEP-MODE CURRENT LESS THAN 275µA
- THERMALLY SELF LIMITING
- NO EXTERNAL COMPENSATION CAPACITORS
- COMPATIBLE WITH ACTIVE NEGATION DRIVERS (60mA / CHANNEL)
- COMPATIBLE WITH PASSIVE AND ACTIVE TERMINATIONS
- APPROVED FOR USE WITH SCSI 1, 2, 3 AND ULTRA SCSI
- HOT SWAP COMPATIBLE
- PIN-FOR-PIN COMPATIBLE WITH LX5205, UC5607/5611/5617 AND DS2109

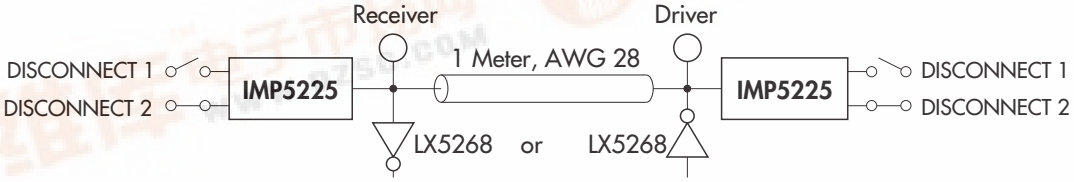
PRODUCT HIGHLIGHT

RECEIVING WAVEFORM - 20MHz



DRIVING WAVEFORM - 20MHz





PACKAGE ORDER INFORMATION

T_A (°C)	DB Plastic SSOP 28-pin	DWP Plastic SOWB 28-pin, Power
0 to 70	IMP5225CDB	IMP5225CDWP

Note: All surface-mount packages are available in Tape & Reel. Append the letter "T" to part number. (i.e. IMP5225CDWPT)

ABSOLUTE MAXIMUM RATINGS (Note 1)

TermPwr Voltage ..... +7V
Signal Line Voltage ..... 0V to +7V
Regulator Output Current 1.2A
Operating Junction Temperature
Plastic (DB, DWP Packages) ..... 150°C
Storage Temperature Range ..... -65°C to 150°C
Lead Temperature (Soldering, 10 seconds) ..... 300°C

Note 1. Exceeding these ratings could cause damage to the device. All voltages are with respect to Ground. Currents are positive into, negative out of the specified terminal.

THERMAL DATA

DB PACKAGE:

THERMAL RESISTANCE-JUNCTION TO AMBIENT, Θ_{JA} ..... 117°C/W

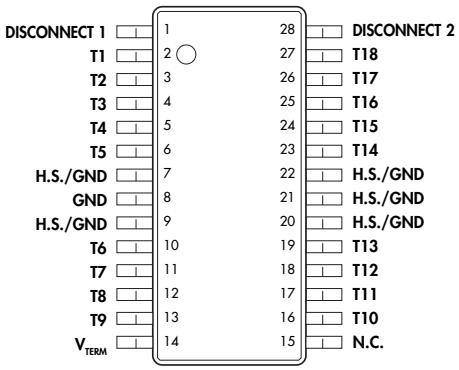
DWP PACKAGE:

THERMAL RESISTANCE-JUNCTION TO LEADS, Θ_{JL} ..... 18°C/W

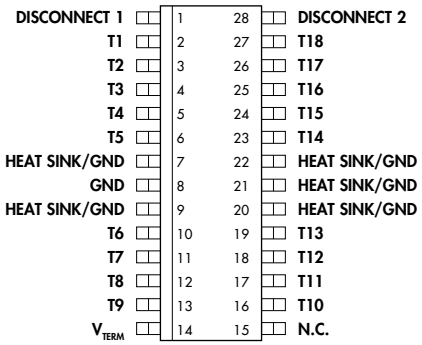
THERMAL RESISTANCE-JUNCTION TO AMBIENT, Θ_{JA} ..... 40°C/W

Junction Temperature Calculation: $T_J = T_A + (P_D \times \theta_{JA})$.
The θ_{JA} numbers are guidelines for the thermal performance of the device/pc-board system.
All of the above assume no ambient airflow.

PACKAGE PIN OUTS



DB PACKAGE
(Top View)



DWP PACKAGE
(Top View)

RECOMMENDED OPERATING CONDITIONS (Note 2)

Parameter	Symbol	Recommended Operating Conditions			Units
		Min.	Typ.	Max.	
Termpwr Voltage	V_{TERM}	3.3		5.5	V
Signal Line Voltage		0		5	V
Disconnect Input Voltage		0		V_{TERM}	V
Operating Virtual Junction Temperature Range					
IMP5225C		0		125	°C

Note 2. Range over which the device is functional.

ELECTRICAL CHARACTERISTICS

Term Power = 4.75V unless otherwise specified. Unless otherwise specified, these specifications apply at the recommended operating ambient temperature of T_A = 25°C. Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.

Parameter	Symbol	Test Conditions	LX5225			Units
			Min.	Typ.	Max.	
Output High Voltage	V_{OUT}		2.65	2.85		V
TermPwr Supply Current	I_{CC}	All data lines = open	10		18	mA
		All data lines = 0.5V		400	450	mA
		DISCONNECT Pins < 0.8V or > 2.0V		200		µA
Output Current	I_{OUT}	V_{OUT} = 0.5V	-21	-23	-24	mA
DISCONNECT Input Current	I_{IN}	DISCONNECT Pins = 4.75V		10		nA
		DISCONNECT Pins = 0V		-90		µA
Output Leakage Current	I_{OL}	DISCONNECT Pins = < 0.8V, V_O = 0.5V		10		nA
Capacitance in DISCONNECT Mode	C_{OUT}	V_{OUT} = 0V, frequency = 1MHz		3		pF
Channel Bandwidth	BW			35		MHz
Termination Sink Current, per Channel	I_{SINK}	V_{OUT} = 4V		60		mA

FUNCTIONAL DESCRIPTION

Cable transmission theory suggests to optimize signal speed and quality, the termination should act both as an ideal voltage reference when the line is released (deasserted) and as an ideal current source when the line is active (asserted). Common active terminators, which consist of Linear Regulators in series with resistors (typically 110Ω), are a compromise. As the line voltage increases, the amount of current decreases linearly by the equation V = I * R. The IMP5225, with its unique new architecture applies the maximum amount of current regardless of line voltage until the termination high threshold (2.85V) is reached.

Acting as a near ideal line terminator, the IMP5225 closely reproduces the optimum case when the device is enabled. In the disable mode, the device is in a sleep state where a meager 200µA of quiescent current is consumed. Additionally, all outputs are in a Hi-Z (impedance) state. Sleep mode can be used for power conservation or to completely eliminate the terminator from the SCSI chain. In the second case, termination node capacitance is important to consider. The terminator will appear as a parasitic distributed capacitance on the line, which can detract from bus performance. For this reason, the IMP5225 has been optimized to have only 4pF of capacitance per output in the sleep state.

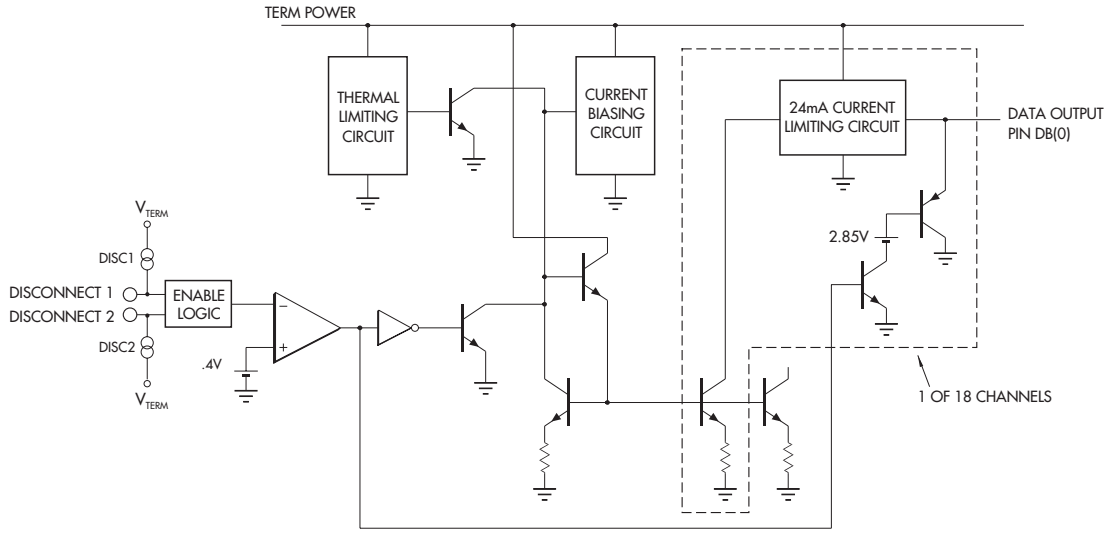
POWER UP / POWER DOWN FUNCTION TABLE

DISCONNECT 1	DISCONNECT 2	Outputs	Quiescent Current
H	H	Disabled	200µA
H	L	Enabled	10mA
L	H	Disabled	200µA
L	L	Disabled	200µA
Open	Open	Disabled	200µA

An additional feature of the IMP5225 is its compatibility with active negation drivers. The device handles up to 60mA of sink current for drivers which exceed the 2.85V output high.

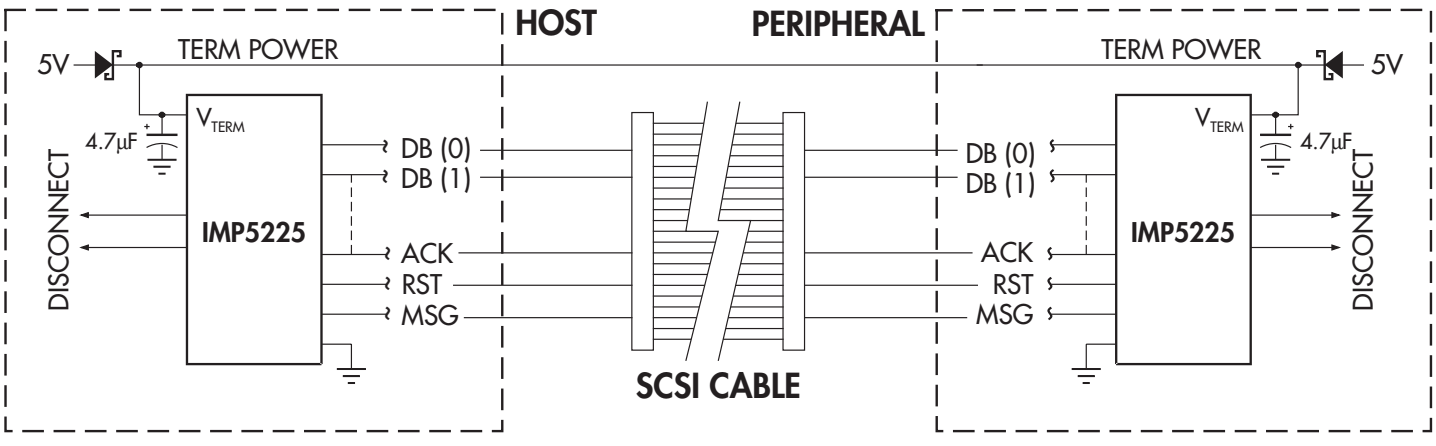
BLOCK DIAGRAM

FIGURE 1 — IMP5225 BLOCK DIAGRAM



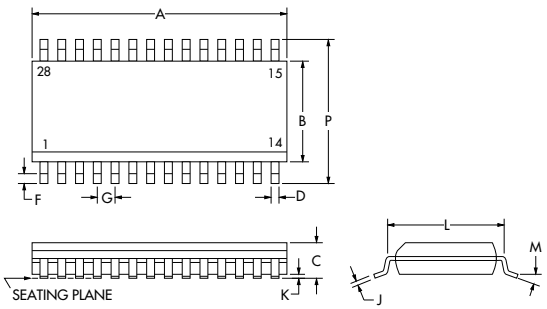
APPLICATION SCHEMATIC

FIGURE 2 — 8-BIT SCSI SYSTEM APPLICATION



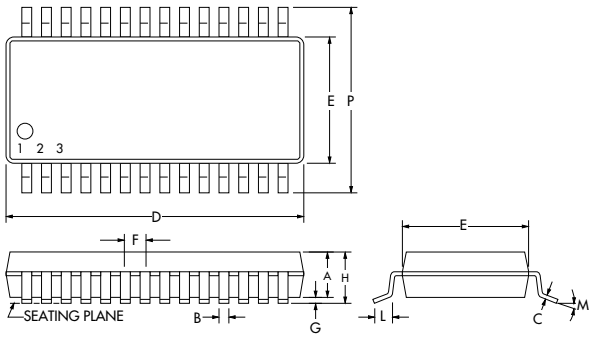
PACKAGE DIMENSIONS

DWP 28-Pin Plastic SOWB POWER



	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	17.73	17.93	0.698	0.705
B	7.40	7.60	0.291	0.299
C	2.44	2.64	0.096	0.104
D	0.36	0.46	0.014	0.018
F	0.51	1.01	0.020	0.040
G	1.27 BSC		0.050 BSC	
J	0.123	0.32	0.005	0.013
K	0.10	0.30	0.004	0.012
L	8.13	8.64	0.320	0.390
M	0°	8°	0°	8°
P	10.26	10.65	0.404	0.419

DB 28-Pin Shrink Small Outline Package (SSOP)



	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	1.73	1.99	0.068	0.078
B	0.25	0.38	0.009	0.015
C	0.13	0.22	0.005	0.008
D	10.07	10.33	0.396	0.407
E	5.20	5.38	0.205	0.212
F	0.65 BSC		0.025 BSC	
G	0.05	0.21	0.002	0.008
H	1.63	1.83	0.064	0.072
L	0.65	0.95	0.025	0.037
M	0°	8°	0°	8°
P	7.65	7.90	0.301	0.311

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