

MOS FIELD EFFECT TRANSISTOR
2SK2480

SWITCHING
N-CHANNEL POWER MOS FET
INDUSTRIAL USE

DESCRIPTION

The 2SK2480 is N-Channel MOS Field Effect Transistor designed for high voltage switching applications.

FEATURES

- Low On-Resistance
 $R_{DS(on)} = 4.0 \Omega$ ($V_{GS} = 10 V, I_D = 2.0 A$)
- Low C_{iss} $C_{iss} = 900 pF$ TYP.
- High Avalanche Capability Ratings
- Isolated TO-220 Package

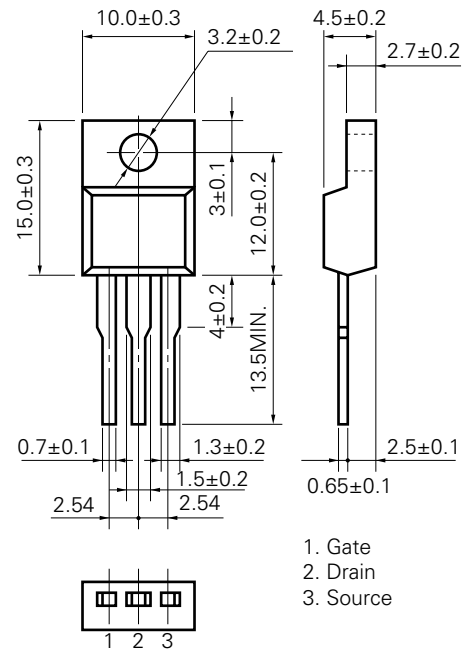
ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ C$)

| | | | |
|--|----------------|-------------|------------|
| Drain to Source Voltage | V_{BSS} | 900 | V |
| Gate to Source Voltage | V_{GSS} | ± 30 | V |
| Drain Current (DC) | $I_{D(DC)}$ | ± 3.0 | A |
| Drain Current (pulse)* | $I_{D(pulse)}$ | ± 12 | A |
| Total Power Dissipation ($T_c = 25^\circ C$) | P_{T1} | 35 | W |
| Total Power Dissipation ($T_A = 25^\circ C$) | P_{T2} | 2.0 | W |
| Channel Temperature | T_{ch} | 150 | $^\circ C$ |
| Storage Temperature | T_{stg} | -55 to +150 | $^\circ C$ |
| Single Avalanche Current** | I_{AS} | 3.0 | A |
| Single Avalanche Energy** | E_{AS} | 37.1 | mJ |

* $PW \leq 10 \mu s, Duty\ Cycle \leq 1\%$

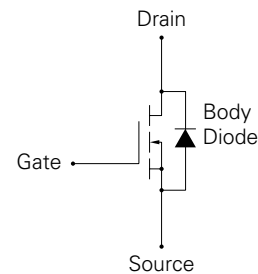
** Starting $T_{ch} = 25^\circ C, R_G = 25 \Omega, V_{GS} = 20 V \rightarrow 0$

PACKAGE DIMENSIONS
(in millimeter)



1. Gate
2. Drain
3. Source

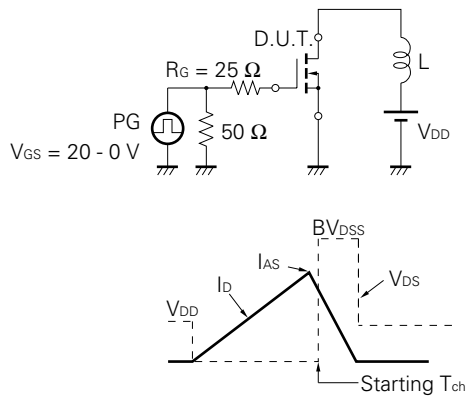
MP-45F (ISOLATED TO-220)



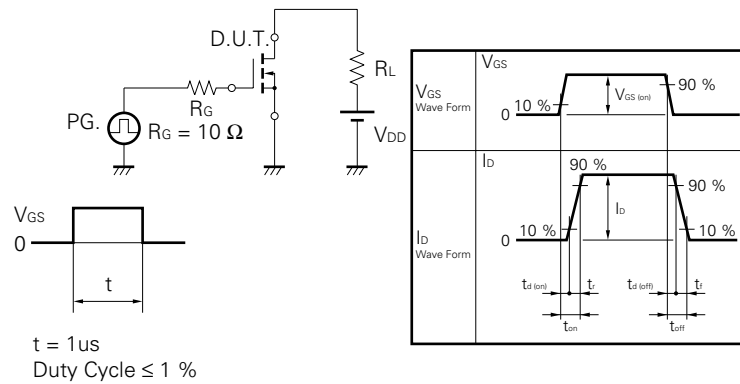
ELECTRICAL CHARACTERISTICS (T_A = 25 °C)

| CHARACTERISTIC | SYMBOL | MIN. | TYP. | MAX. | UNIT | TEST CONDITIONS |
|--------------------------------|----------------------|------|------|------|------|--|
| Drain to Source On-Resistance | R _{DS(on)} | | 3.2 | 4.0 | Ω | V _{GS} = 10 V, I _D = 2.0 A |
| Gate to Source Cutoff Voltage | V _{GS(off)} | 2.5 | | 3.5 | V | V _{DS} = 10 V, I _D = 1 mA |
| Forward Transfer Admittance | y _{fs} | 1.0 | | | S | V _{DS} = 20 V, I _D = 2.0 A |
| Drain Leakage Current | I _{DSS} | | | 100 | μA | V _{DS} = V _{DSS} , V _{GS} = 0 |
| Gate to Source Leakage Current | I _{GSS} | | | ±100 | nA | V _{GS} = ±30 V, V _{DS} = 0 |
| Input Capacitance | C _{iss} | | 900 | | pF | V _{DS} = 10 V |
| Output Capacitance | C _{oss} | | 130 | | pF | V _{GS} = 0 |
| Reverse Transfer Capacitance | C _{rss} | | 25 | | pF | f = 1 MHz |
| Turn-On Delay Time | t _{d(on)} | | 17 | | ns | I _D = 2.0 A |
| Rise Time | t _r | | 7 | | ns | V _{GS} = 10 V |
| Turn-Off Delay Time | t _{d(off)} | | 63 | | ns | V _{DD} = 150 V |
| Fall Time | t _f | | 8 | | ns | R _G = 75 Ω |
| Total Gate Charge | Q _G | | 30 | | nC | I _D = 3.0 A |
| Gate to Source Charge | Q _{GS} | | 5 | | nC | V _{DD} = 450 V |
| Gate to Drain Charge | Q _{GD} | | 16 | | nC | V _{GS} = 10 V |
| Body Diode Forward Voltage | V _{F(S-D)} | | 1.0 | | V | I _F = 3.0 A, V _{GS} = 0 |
| Reverse Recovery Time | t _{rr} | | 650 | | ns | I _F = 3.0 A, V _{GS} = 0 |
| Reverse Recovery Charge | Q _{rr} | | 2.8 | | μC | di/dt = 50 A/μs |

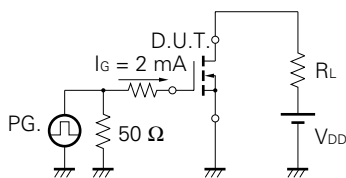
Test Circuit 1 Avalanche Capability



Test Circuit 2 Switching Time

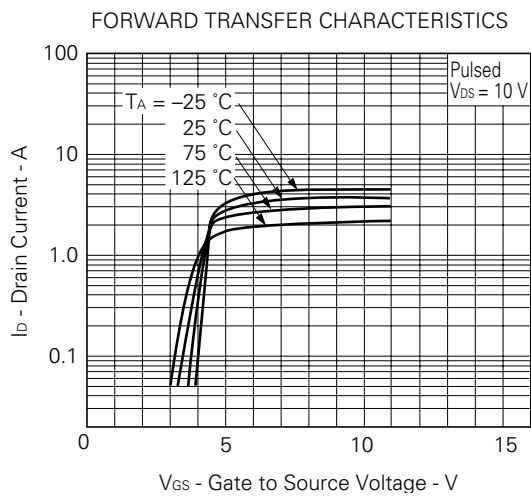
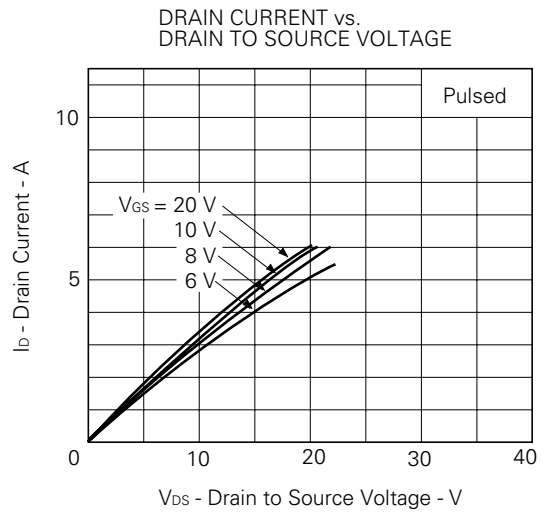
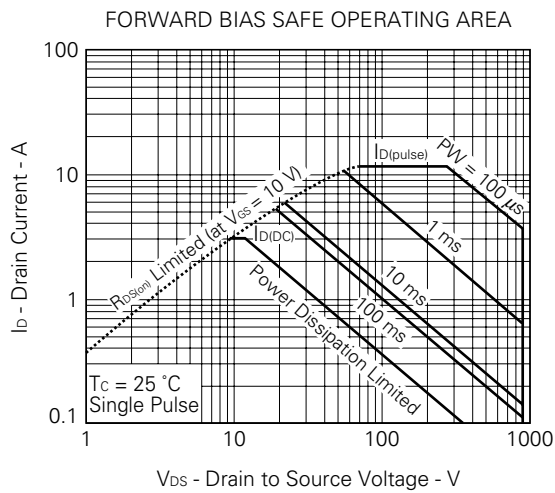
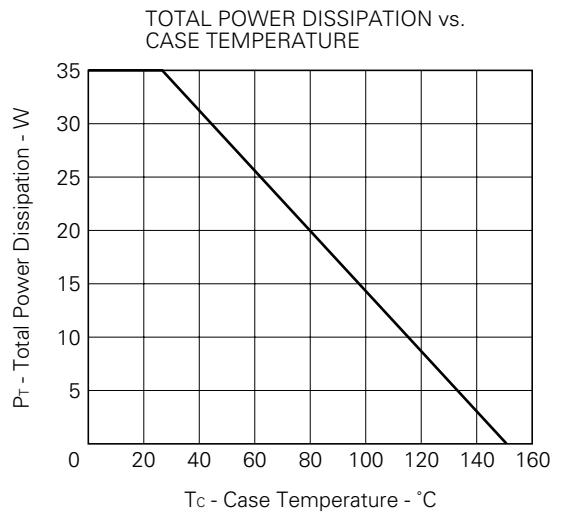
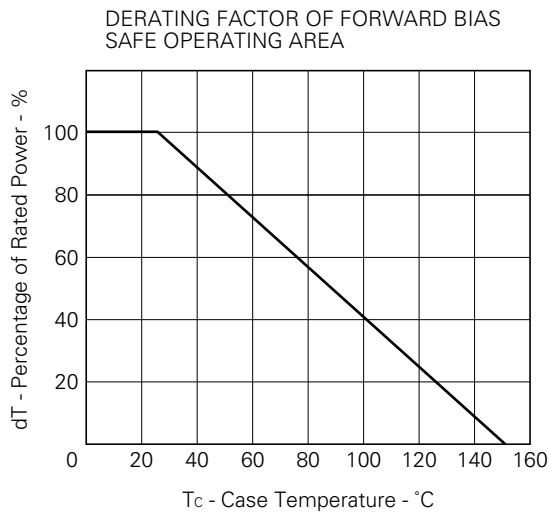


Test Circuit 3 Gate Charge

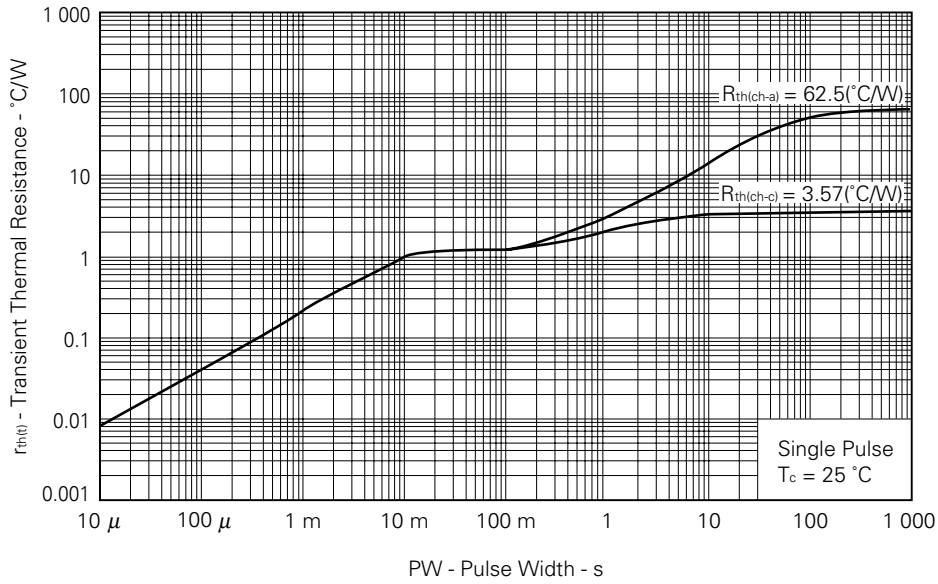


The application circuits and their parameters are for references only and are not intended for use in actual design-in's.

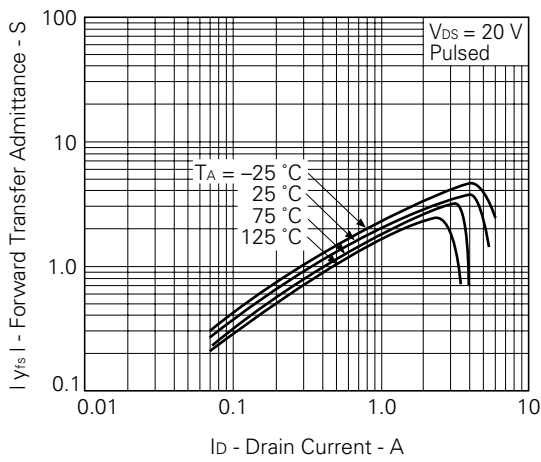
TYPICAL CHARACTERISTICS (T_A = 25 °C)



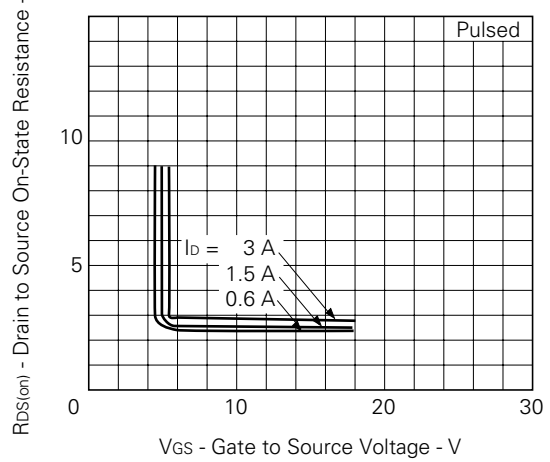
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



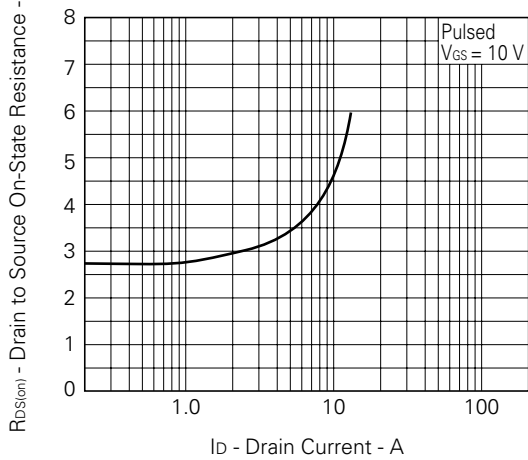
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



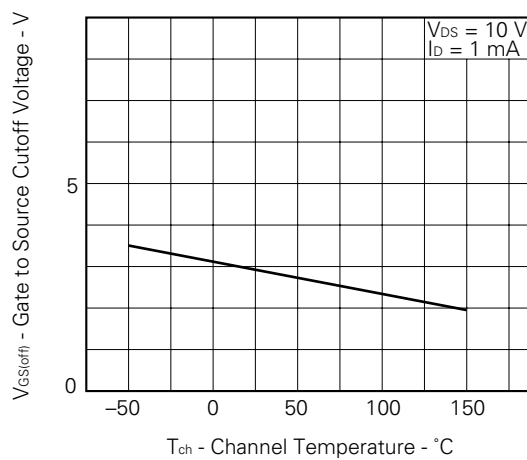
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

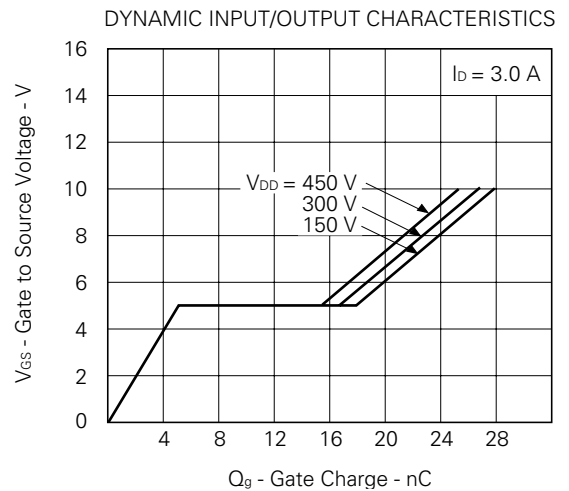
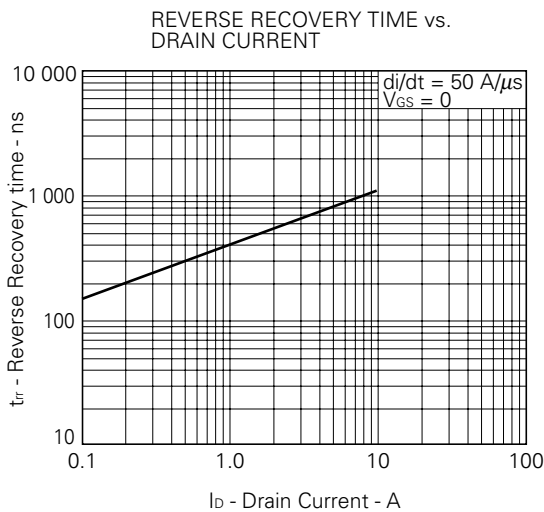
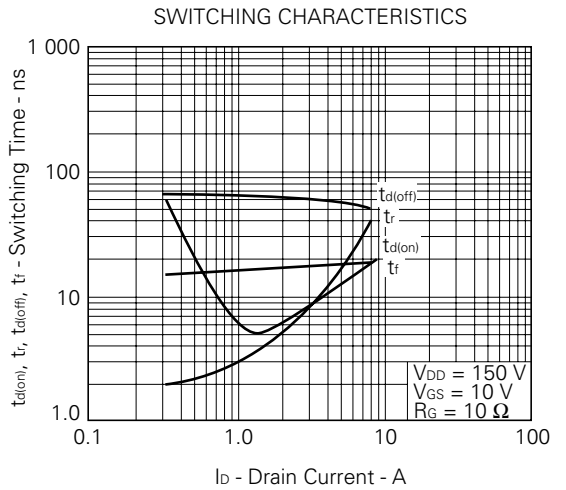
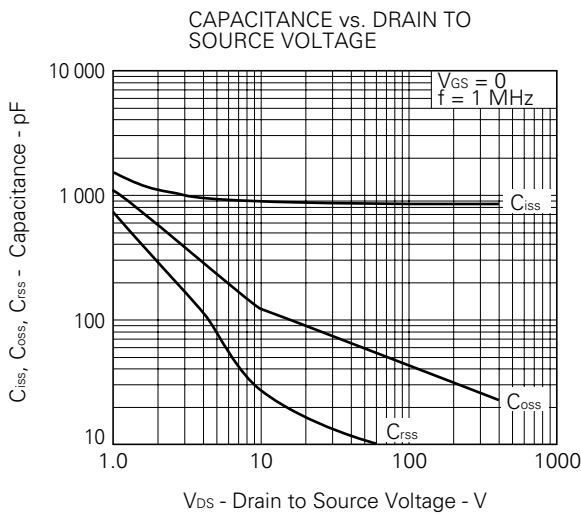
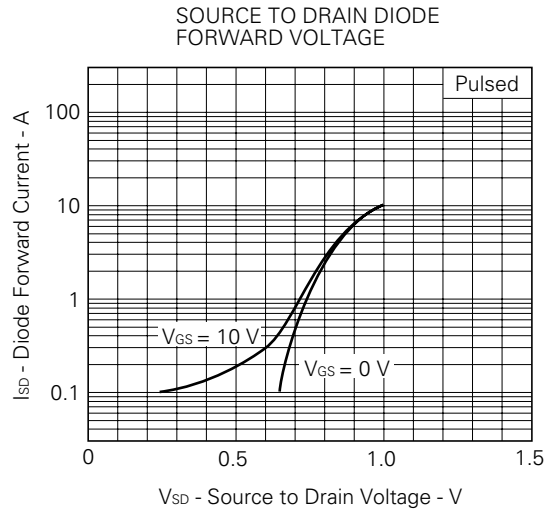
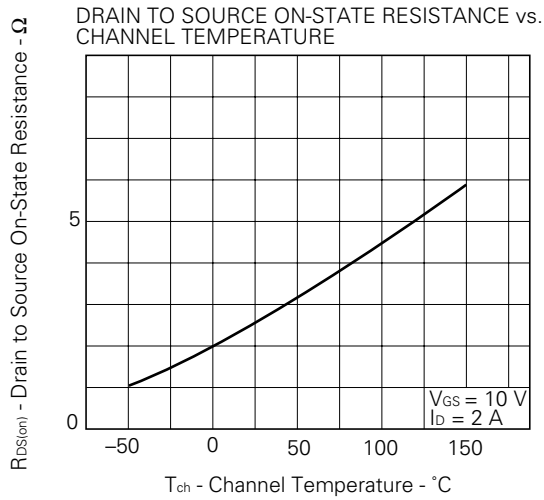


DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT

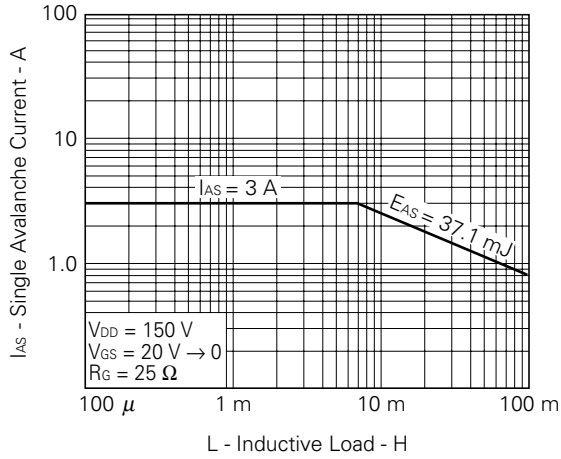


GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE

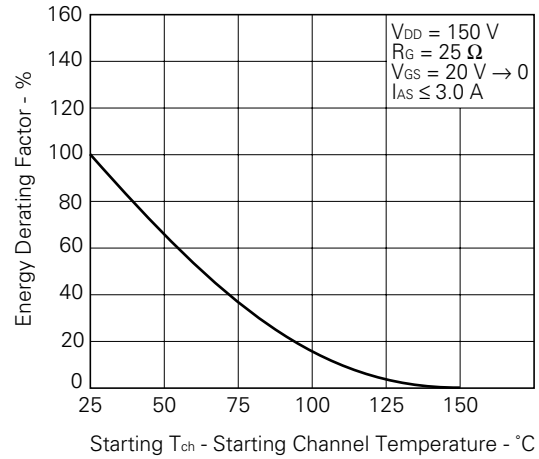




SINGLE AVALANCHE CURRENT vs. INDUCTIVE LOAD



SINGLE AVALANCHE ENERGY DERATING FACTOR



REFERENCE

| Document Name | Document No. |
|--|--------------|
| NEC semiconductor device reliability/quality control system. | TEI-1202 |
| Quality grade on NEC semiconductor devices. | IEI-1209 |
| Semiconductor device mounting technology manual. | IEI-1207 |
| Semiconductor device package manual. | IEI-1213 |
| Guide to quality assurance for semiconductor devices. | MEI-1202 |
| Semiconductor selection guide. | MF-1134 |
| Power MOS FET features and application switching power supply. | TEA-1034 |
| Application circuits using Power MOS FET. | TEA-1035 |
| Safe operating area of Power MOS FET. | TEA-1037 |

[MEMO]

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Anti-radioactive design is not implemented in this product.