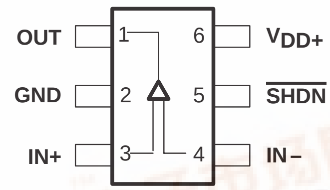
TLV2460, TLV2461, TLV2462, TLV2463, TLV2464, TLV2465, TLV246xA
FAMILY OF LOW-POWER RAIL-TO-RAIL INPUT/OUTPUT OPERATIONAL AMPLIFIERS WITH SHUTDOWN

SLOS220G – JULY 1998 – REVISED JULY 2000

- **Input Common-Mode Range Exceeds Both Supply Rails . . . – 0.2 V to V_{DD+} + 0.2 V**
- **Gain Bandwidth Product . . . 6.4 MHz**
- **Supply Current . . . 500µA/channel**
- **Input Offset Voltage . . . 100 µV**
- **Input Noise Voltage . . . 11nV/√Hz**
- **Rail-to-Rail Output Swing**
- **Slew Rate . . . 1.6 V/µs**
- **±90mA Output Drive Capability**
- **Micropower Shutdown Mode (TLV2460/3/5) . . . 0.3 µA/channel**
- **Available in 5- or 6-pin SOT23, 8- or 10-Pin MSOP, CDIP, LCC, and EPAK**
- **Characterized From T_A = –55°C to 125°C**
- **Universal Operational Amplifier EVM**
- **Available in Q-Temp Automotive**
  HighRel Automotive Applications
  Configuration Control/Print Support
  Qualification to Automotive Standards

TLV2460
DBV PACKAGE
(TOP VIEW)



description

The TLV246x is a family of low-power rail-to-rail input/output operational amplifiers specifically designed for portable applications. The input common-mode voltage range extends beyond the supply rails for maximum dynamic range in low-voltage systems. The amplifier output has rail-to-rail performance with high-output-drive capability, solving one of the limitations of older rail-to-rail input/output operational amplifiers. This rail-to-rail dynamic range and high output drive make the TLV246x ideal for buffering analog-to-digital converters.

The operational amplifier has 6.4 MHz of bandwidth and 1.6 V/µs of slew rate with only 500 µA of supply current, providing good ac performance with low power consumption. Three members of the family offer a shutdown terminal, which places the amplifier in an ultralow supply current mode (I_{DD} = 0.3 µA/ch). While in shutdown, the operational-amplifier output is placed in a high-impedance state. DC applications are also well served with an input noise voltage of 11 nV/√Hz and input offset voltage of 100 µV.

This family is available in the low-profile SOT23, MSOP, TSSOP, CDIP, LCC, and EPAK packages. The TLV2460 is the first rail-to-rail input/output operational amplifier with shutdown available in the 6-pin SOT23, making it perfect for high-density circuits. The family is specified over an expanded temperature range (T_A = –40°C to 125°C) for use in industrial control and automotive systems, and over the military temperature range (T_A = –55°C to 125°C) for use in military systems.

FAMILY PACKAGE TABLE

DEVICE	NO. OF Ch	PACKAGE TYPES								SHUTDOWN	UNIVERSAL EVM BOARD
		PDIP	SOIC	SOT-23	TSSOP	MSOP	CDIP	LCC	CFP		
TLV2460	1	8	8	6	8	—	8	20	10	Yes	Refer to the EVM Selection Guide (Lit# SLOU060)
TLV2461	1	8	8	5	8	—	8	20	10	—	
TLV2462	2	8	8	—	8	8	8	20	10	—	
TLV2463	2	14	14	—	14	10	14	20	10	Yes	
TLV2464	4	14	14	—	14	—	14	20	14	—	
TLV2465	4	16	16	—	16	—	16	20	14	Yes	

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

This document contains information on products in more than one phase of development. The status of each device is indicated on the page(s) specifying its electrical characteristics.

On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

TLV2460C/I/AI and TLV2461C/I/AI AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C	PACKAGED DEVICES			CHIP FORM‡ (Y)
		SMALL OUTLINE (D)	SOT-23† (DBV)	PLASTIC DIP (P)	
0°C to 70°C	2000 µV	TLV2460CD TLV2461CD	TLV2460CDBV TLV2461CDBV	TLV2460CP TLV2461CP	TLV2460Y TLV2461Y
-40°C to 125°C	2000 µV	TLV2460ID TLV2461ID	TLV2460IDBV TLV2461IDBV	TLV2460IP TLV2461IP	— —
	1500 µV	TLV2460AID TLV2461AID	— —	TLV2460AIP TLV2461AIP	— —

† This package is available taped and reeled. To order this packaging option, add an R suffix to the part number (e.g., TLV2460CDR).
‡ Chip forms are tested at T_A = 25°C only.

TLV2460M/AM/Q/AQ and TLV2461M/AM/Q/AQ AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C	PACKAGED DEVICES				
		SMALL OUTLINE† (D)	SMALL OUTLINE† (PW)	CERAMIC DIP (JG)	CERAMIC FLATPACK (U)	CHIP CARRIER (FK)
-40°C to 125°C	2000 µV	TLV2460QD TLV2461QD	TLV2460QPW TLV2461QPW	— —	— —	— —
	1500 µV	TLV2460AQD TLV2461AQD	TLV2460AQPW TLV2461AQPW	— —	— —	— —
–55°C to 125°C	2000 µV	— —	— —	TLV2460MJG TLV2461MJG	TLV2460MU TLV2461MU	TLV2460MFK TLV2461MFK
	1500 µV	— —	— —	TLV2460AMJG TLV2461AMJG	TLV2460AMU TLV2461AMU	TLV2460AMFK TLV2461AMFK

† This package is available taped and reeled. To order this packaging option, add an R suffix to the part number (e.g., TLV2460QDR).

TLV2462C/I/AI and TLV2463C/I/AI AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C	PACKAGED DEVICES					CHIP FORM‡ (Y)
		SMALL OUTLINE† (D)	MSOP (DGK)	MSOP† (DGS)	PLASTIC DIP (N)	PLASTIC DIP (P)	
0°C to 70°C	2000 µV	TLV2462CD TLV2463CD	TLV2462CDGK —	— TLV2463CDGS	— TLV2463CN	TLV2462CP —	TLV2462Y TLV2463Y
–40°C to 125°C	2000 µV	TLV2462ID TLV2463ID	TLV2462IDGK —	— TLV2463IDGS	— TLV2463IN	TLV2462IP —	— —
	1500 µV	TLV2462AID TLV2463AID	— —	— —	— TLV2463AIN	TLV2462AIP —	— —

† This package is available taped and reeled. To order this packaging option, add an R suffix to the part number (e.g., TLV2462CDR).
‡ Chip forms are tested at T_A = 25°C only.

TLV2462M/AM/Q/AQ and TLV2463M/AM/Q/AQ AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C	PACKAGED DEVICES					
		SMALL OUTLINE† (D)	SMALL OUTLINE† (PW)	CERAMIC DIP (JG)	CERAMIC DIP (J)	CERAMIC FLATPACK (U)	CHIP CARRIER (FK)
-40°C to 125°C	2000 µV	TLV2462QD TLV2463QD	TLV2462QPW TLV2463QPW	— —	— —	— —	— —
	1500 µV	TLV2462AQD TLV2463AQD	TLV2462AQPW TLV2463AQPW	— —	— —	— —	— —
–55°C to 125°C	2000 µV	— —	— —	TLV2462MJG —	— TLV2463MJ	TLV2462MU TLV2463MU	TLV2462MFK TLV2463MFK
	1500 µV	— —	— —	TLV2462AMJG —	— TLV2463AMJ	TLV2462AMU	TLV2462AMFK TLV2463AMFK

† This package is available taped and reeled. To order this packaging option, add an R suffix to the part number (e.g., TLV2462QDR).

TLV2464C/I/AI and TLV2465C/I/AI AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C	PACKAGED DEVICES			CHIP FORM‡ (Y)
		SMALL OUTLINE (D)	PLASTIC DIP (N)	TSSOP (PW)	
0°C to 70°C	2000 µV	TLV2464CD TLV2465CD	TLV2464CN TLV2465CN	TLV2464CPW TLV2465CPW	TLV2464Y TLV2465Y
–40°C to 125°C	2000 µV	TLV2464ID TLV2465ID	TLV2464IN TLV2465IN	TLV2464IPW TLV2465IPW	— —
–40°C to 125°C	1500 µV	TLV2464AID TLV2465AID	TLV2464AIN TLV2465AIN	TLV2464AIPW TLV2465AIPW	— —

† This package is available taped and reeled. To order this packaging option, add an R suffix to the part number (e.g., TLV2464CDR).
‡ Chip forms are tested at T_A = 25°C only.

TLV2464M/AM/Q/AQ and TLV2465M/AM/Q/AQ AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C	PACKAGED DEVICES				
		SMALL OUTLINE† (D)	SMALL OUTLINE† (PW)	CERAMIC DIP (J)	CERAMIC FLATPACK (W)	CHIP CARRIER (FK)
-40°C to 125°C	2000 µV	TLV2464QD TLV2465QD	TLV2464QPW TLV2465QPW	— —	— —	— —
	1500 µV	TLV2464AQD TLV2465AQD	TLV2464AQPW TLV2465AQPW	— —	— —	— —
–55°C to 125°C	2000 µV	— —	— —	TLV2464MJ TLV2465MJ	TLV2464MW TLV2465MW	TLV2464MFK TLV2465MFK
	1500 µV	— —	— —	TLV2464AMJ TLV2465AMJ	TLV2464AMW TLV2465AMW	TLV2464AMFK TLV2465AMFK

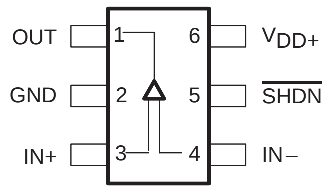
† This package is available taped and reeled. To order this packaging option, add an R suffix to the part number (e.g., TLV2464QDR).

SOT-23 AND MSOP DEVICE SYMBOLS

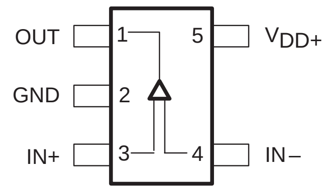
DEVICE TYPE	NO. OF TERMINALS	PACKAGE NAME	SYMBOL
SOT-23	6 Pin	TLV2460CDBV	VAOC
		TLV2460IDBV	VAOI
	5 Pin	TLV2461CDBV	VAPC
		TLV2461IDBV	VAPI
MSOP	8 Pin	TLV2462CDGK	xxTIAAI
		TLV2462IDGK	xxTIAAJ
	10 Pin	TLV2463CDGS	xxTIAAK
		TLV2463IDGS	xxTIAAL

TLV246x PACKAGE PINOUTS

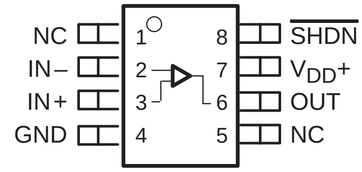
TLV2460
DBV PACKAGE
(TOP VIEW)



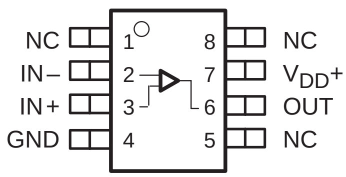
TLV2461
DBV PACKAGE
(TOP VIEW)



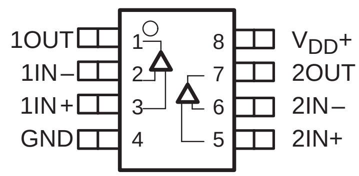
TLV2460
D, P, JG, OR PW PACKAGE
(TOP VIEW)



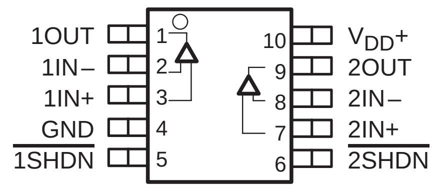
TLV2461
D, P, JG, OR PW PACKAGE
(TOP VIEW)



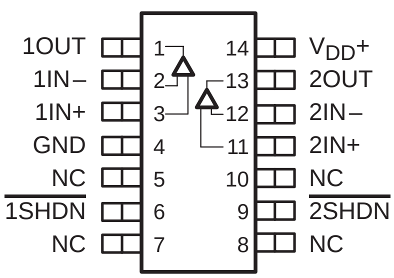
TLV2462
D, DGK, P, JG, OR PW PACKAGE
(TOP VIEW)



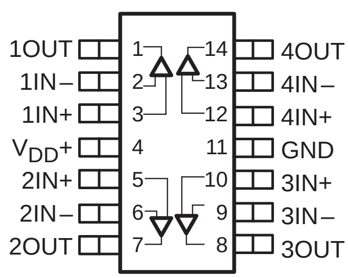
TLV2463
DGS PACKAGE
(TOP VIEW)



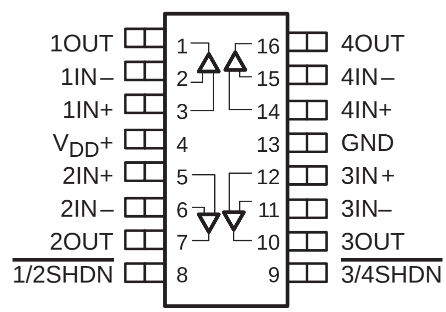
TLV2463
D, N, J, OR PW PACKAGE
(TOP VIEW)



TLV2464
D, N, PWP, J, W, OR PW PACKAGE
(TOP VIEW)



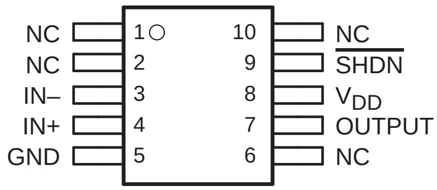
TLV2465
D, N, PWP, J, W, OR PW PACKAGE
(TOP VIEW)



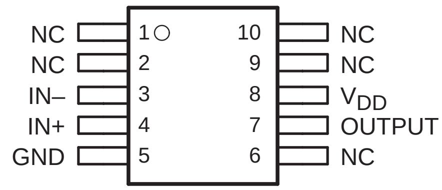
NC – No internal connection

TLV246x PACKAGE PINOUTS (continued)

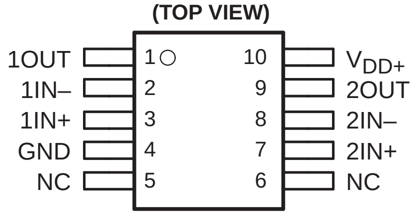
TLV2460
U PACKAGE
(TOP VIEW)



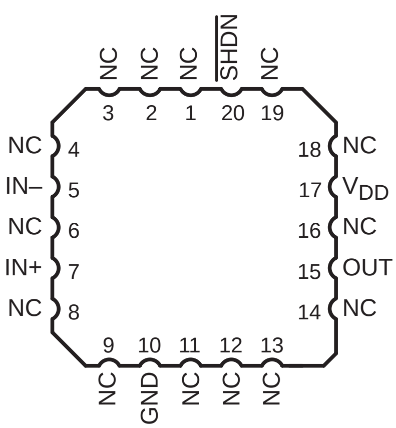
TLV2461
U PACKAGE
(TOP VIEW)



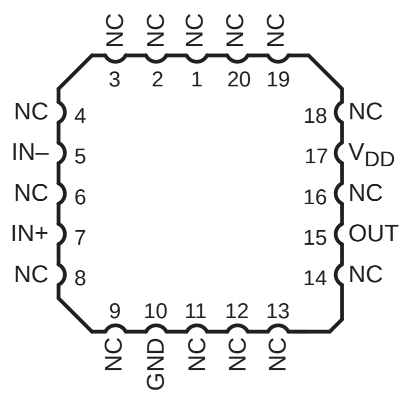
TLV2462
U PACKAGE
(TOP VIEW)



TLV2460
FK PACKAGE
(TOP VIEW)



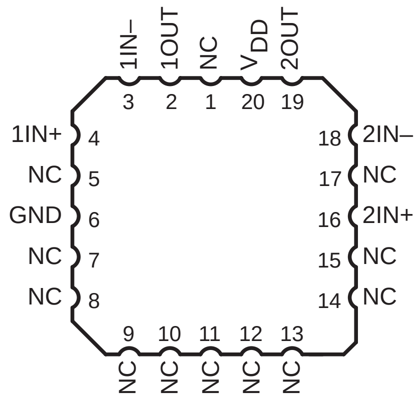
TLV2461
FK PACKAGE
(TOP VIEW)



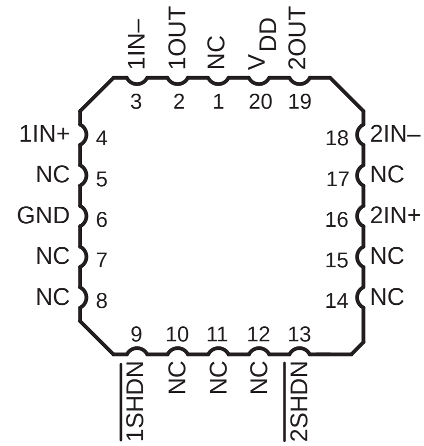
NC – No internal connection

TLV246x PACKAGE PINOUTS (continued)

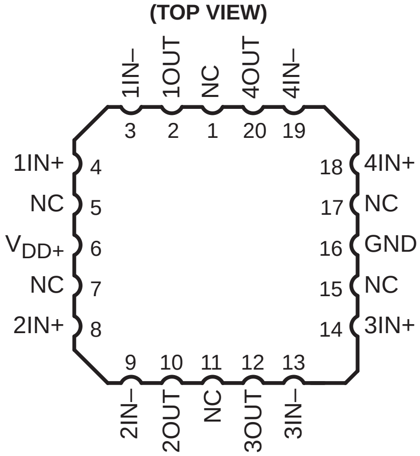
TLV2462
FK PACKAGE
(TOP VIEW)



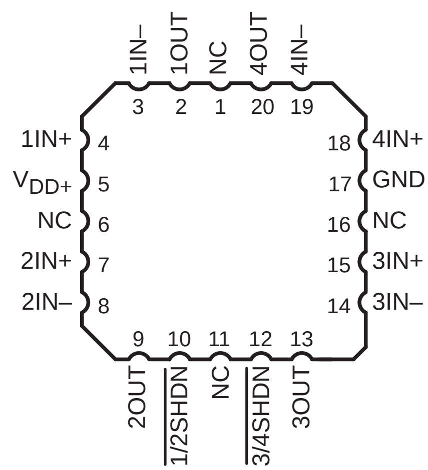
TLV2463
FK PACKAGE
(TOP VIEW)



TLV2464
FK PACKAGE
(TOP VIEW)



TLV2465
FK PACKAGE
(TOP VIEW)



NC – No internal connection

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1) . . . . 6 V
Differential input voltage, V_{ID} . . . . V_{DD} – 0.2 V to V_{DD} + 0.2 V
Input current, I_I (any input) . . . . ± 200 mA
Output current, I_O . . . . ± 175 mA
Total input current, I_I (into V_{DD+}) . . . . 175 mA
Total output current, I_O (out of GND) . . . . 175 mA
Continuous total power dissipation . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A: C suffix . . . . 0°C to 70°C
I and Q suffix . . . . –40°C to 125°C
M suffix . . . . –55°C to 125°C
Maximum junction temperature, T_J . . . . 150°C
Storage temperature range, T_{stg} . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values, except differential voltages, are with respect to GND.

DISSIPATION RATING TABLE FOR C and I SUFFIX

PACKAGE	Θ_{JC} (°C/W)	Θ_{JA} (°C/W)	$T_A \le 25°C$ POWER RATING
D (8)	38.3	176	725 mW
D (14)	26.9	122.6	725 mW
D (16)	25.7	114.7	725 mW
DBV (5)	55	324.1	437 mW
DBV (6)	55	294.3	437 mW
DGK	54.23	259.96	424 mW
DGS	54.1	257.71	424 mW
N (14)	32	78	1150 mW
N (16)	32	78	1150 mW
P	41	104	1000 mW
PW (14)	29.3	173.6	700 mW
PW (16)	28.7	161.4	700 mW

DISSIPATION RATING TABLE FOR Q and M SUFFIX

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$‡	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	145 mW
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
PW	700 mW	5.6 mW/°C	448 mW	364 mW	140 mW
U	675 mW	5.4 mW/°C	432 mW	350 mW	135 mW

‡ This is the inverse of the traditional Junction-to-Ambient thermal Resistance ($R\Theta_{JA}$). Thermal Resistances are not production tested and are for informational purposes only.

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{DD}	Single supply	2.7	6	V
	Split supply	±1.35	±3	
Common-mode input voltage range, V_{ICR}		GND	V_{DD+}	V
Operating free-air temperature, T_A	C-suffix	0	70	°C
	I-suffix and Q–suffix	–40	125	
	M-suffix	–55	125	

electrical characteristics at specified free-air temperature, V_{DD} = 3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage (TLV246x)	V_{DD} = ±1.5 V, V_{IC} = 0,	V_O = 0, R_S = 50 Ω	25°C		100	2000	μV
				Full range			2200	
V_{IO}	Input offset voltage (TLV246xA)			25°C		150	1500	μV
				Full range			1700	
α_{VIO}	Temperature coefficient of input offset voltage					2		μV/°C
V_{IO}	Input offset voltage (TLV246x)	V_O = 1.5 V, R_S = 50 Ω	TLV246xQ, TLV246xM	25°C		150	2000	μV
				Full range			2200	
V_{IO}	Input offset voltage (TLV246xA)			25°C		150	1500	μV
				Full range			1700	
I_{IO}	Input offset current	V_{DD} = ±1.5 V, V_{IC} = 0, V_O = 0, R_S = 50 Ω		25°C		2.8	7	nA
			TLV246xC	Full range			20	
			TLV246xI/Q/M	Full range			75	
I_{IB}	Input bias current			25°C		4.4	14	nA
			TLV246xC	Full range			25	
			TLV246xI/Q/M	Full range			75	
V_{ICR}	Common-mode input voltage range	CMRR > 66 dB,	R_S = 50 Ω	25°C	–0.2 to 3.2			V
		CMRR > 60 dB,	R_S = 50 Ω	Full range	–0.2 to 3.2			
V_{OH}	High-level output voltage	I_{OH} = –2.5 mA		25°C		2.9		V
				Full range	2.8			
		I_{OH} = –10 mA		25°C		2.7		
				Full range	2.5			
V_{OL}	Low-level output voltage	V_{IC} = 1.5 V,	I_{OL} = 2.5 mA	25°C		0.1		V
				Full range			0.2	
		V_{IC} = 1.5 V,	I_{OL} = 10 mA	25°C		0.3		
				Full range			0.5	
I_{OS}	Short-circuit output current	Sourcing		25°C		50		mA
				Full range	20			
		Sinking		25°C		40		
				Full range	20			

† Full range is 0°C to 70°C for the C suffix, –40°C to 125°C for the I and Q suffixes, and –55°C to 125°C for the M suffix.

electrical characteristics at specified free-air temperature, V_{DD} = 3 V (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
I_O	Output current			25°C		±30		mA
A_{VD}	Large-signal differential voltage amplification	R_L = 10 kΩ		25°C	90	105		dB
				Full range	89			
$r_{i(d)}$	Differential input resistance			25°C		10^9		Ω
$c_{i(c)}$	Common-mode input capacitance	f = 10 kHz		25°C		7		pF
z_o	Closed-loop output impedance	f = 100 kHz,	A_V = 10	25°C		33		Ω
CMRR	Common-mode rejection ratio	V_{ICR} = –0.2 V to 3.2 V, R_S = 50 Ω		25°C	66	80		dB
			TLV246xC	Full range	64			
			TLV246xI/Q/M	Full range	60			
k_{SVR}	Supply voltage rejection ratio (ΔV_{DD} /ΔV_{IO})	V_{DD} = 2.7 V to 6 V, No load	V_{IC} = V_{DD}/2,	25°C	80	85		dB
				Full range	75			
		V_{DD} = 3 V to 5 V, No load	V_{IC} = V_{DD}/2,	25°C	85	95		
				Full range	80			
I_{DD}	Supply current (per channels)	V_O = 1.5 V, $\overline{SHDN}$ > 1.02 V	No load,	25°C		0.5	0.575	mA
				Full range			0.9	
$V_{(ON)}$	Turnon voltage level	A_V = 1	Channel 1	25°C		1.021		V
			Channel 2			1.02		
$V_{(OFF)}$	Turnoff voltage level	A_V = 1	Channel 1	25°C		0.822		V
			Channel 2			0.817		
$I_{DD(SHDN)}$	Supply current in shutdown (TLV2460, TLV2463, TLV2465)	$\overline{SHDN}$ < 0.8 V, Per channel in shutdown		25°C		0.3		μA
				Full range			2.5	

† Full range is 0°C to 70°C for the C suffix, –40°C to 125°C for the I and Q suffixes, and –55°C to 125°C for the M suffix.

operating characteristics at specified free-air temperature, V_{DD} = 3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	$V_{O(PP)}$ = 2 V, R_L = 10 kΩ	C_L = 160 pF,	25°C	1	1.6		V/μs
				Full range	0.8			
V_n	Equivalent input noise voltage	f = 100 Hz		25°C		16		nV/√Hz
		f = 1 kHz		25°C		11		
I_n	Equivalent input noise current	f = 1 kHz		25°C		0.13		pA/√Hz
THD + N	Total harmonic distortion plus noise	$V_{O(PP)}$ = 2 V, R_L = 10 kΩ, f = 1 kHz	A_V = 1	25°C		0.006%		
			A_V = 10			0.02%		
			A_V = 100			0.08%		
$t_{(on)}$	Amplifier turnon time	A_V = 1, R_L = 10 kΩ	Both channels	25°C		7.6		μs
			Channel 1 only, Channel 2 on			7.65		
			Channel 2 only, Channel 1 on			7.25		

† Full range is 0°C to 70°C for the C suffix, –40°C to 125°C for the I and Q suffixes, and –55°C to 125°C for the M suffix.

operating characteristics at specified free-air temperature, V_{DD} = 3 V (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
$t_{(off)}$	Amplifier turnoff time	A_V = 1, R_L = 10 kΩ	Both channels	25°C		333		ns
			Channel 1 only, Channel 2 on			328		
			Channel 2 only, Channel 1 on			329		
	Gain-bandwidth product	f = 10 kHz, C_L = 160 pF	R_L = 10 kΩ,	25°C		5.2		MHz
t_s	Settling time	$V_{(STEP)PP}$ = 2 V, A_V = –1, C_L = 10 pF, R_L = 10 kΩ	0.1%	25°C		1.47		µs
			0.01%			1.78		
		$V_{(STEP)PP}$ = 2 V, A_V = –1, C_L = 56 pF, R_L = 10 kΩ	0.1%			1.77		
			0.01%			1.98		
ϕ_m	Phase margin at unity gain	R_L = 10 kΩ,	C_L = 160 pF	25°C		44°		
	Gain margin			25°C		7		dB

† Full range is 0°C to 70°C for the C suffix, –40°C to 125°C for the I and Q suffixes, and –55°C to 125°C for the M suffix.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage (TLV246x)	V_{DD} = ±2.5 V, V_{IC} = 0,	V_O = 0, R_S = 50 Ω	25°C		150	2000	µV
				Full range			2200	
V_{IO}	Input offset voltage (TLV246xA)			25°C		150	1500	µV
				Full range			1700	
α_{VIO}	Temperature coefficient of input offset voltage			25°C		2		µV/°C
V_{IO}	Input offset voltage (TLV246x)	V_O = 2.5 V, R_S = 50 Ω	TLV246xQ, TLV246xM	25°C		150	2000	µV
				Full range			2200	
V_{IO}	Input offset voltage (TLV246xA)			25°C		150	1500	µV
				Full range			1700	
I_{IO}	Input offset current	V_{DD} = ±2.5 V, V_{IC} = 0, V_O = 0, R_S = 50 Ω		25°C		0.3	7	nA
			TLV246xC	Full range			15	
			TLV246xI/Q/M	Full range			60	
I_{IB}	Input bias current			25°C		1.3	14	nA
			TLV246xC	Full range			30	
			TLV246xI/Q/M	Full range			60	
V_{ICR}	Common-mode input voltage range	CMRR > 71 dB,	R_S = 50 Ω	25°C	–0.2 to 5.2			V
		CMRR > 60 dB,	R_S = 50 Ω	Full range	0 to 5			

† Full range is 0°C to 70°C for the C suffix, –40°C to 125°C for the I and Q suffixes, and –55°C to 125°C for the M suffix.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –2.5 mA		25°C		4.9		V
				Full range	4.8			
		I_{OH} = –10 mA		25°C		4.8		
				Full range	4.7			
V_{OL}	Low-level output voltage	V_{IC} = 2.5 V,	I_{OL} = 2.5 mA	25°C		0.1		V
				Full range			0.2	
		V_{IC} = 2.5 V,	I_{OL} = 10 mA	25°C		0.2		
				Full range			0.3	
I_{OS}	Short-circuit output current	Sourcing		25°C		145		mA
				Full range	60			
		Sinking		25°C		100		
				Full range	60			
I_O	Output current			25°C		±90		mA
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 2.5 V, V_O = 1 V to 4 V	R_L = 10 kΩ,	25°C	92	109		dB
				Full range	90			
$r_{i(d)}$	Differential input resistance			25°C		10^9		Ω
$c_{i(c)}$	Common-mode input capacitance	f = 10 kHz		25°C		7		pF
z_o	Closed-loop output impedance	f = 100 kHz,	A_V = 10	25°C		29		Ω
CMRR	Common-mode rejection ratio	V_{ICR} = –0.2 V to 5.2 V, R_S = 50 Ω		25°C	71	85		dB
			TLV246xC	Full range	69			
			TLV246xI/Q/M	Full range	60			
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 2.7 V to 6 V, No load	$V_{IC} = V_{DD}/2$,	25°C	80	85		dB
				Full range	75			
		V_{DD} = 3 V to 5 V, No load	$V_{IC} = V_{DD}/2$,	25°C	85	95		dB
				Full range	80			
I_{DD}	Supply current (per channel)	V_O = 2.5 V, $\overline{SHDN}$ > 1.38 V	No load,	25°C		0.55	0.65	mA
				Full range			1	
$V_{(ON)}$	Turnon voltage level	A_V = 1	Channel 1	25°C		1.372		V
			Channel 2			1.368		
$V_{(OFF)}$	Turnoff voltage level	A_V = 1	Channel 1	25°C		1.315		V
			Channel 2			1.309		
$I_{DD(SHDN)}$	Supply current in shutdown (TLV2460, TLV2463, TLV2465)	$\overline{SHDN}$ < 1.3 V, Per channels in shutdown		25°C		1		µA
				Full range			3	

† Full range is 0°C to 70°C for the C suffix, –40°C to 125°C for the I and Q suffixes, and –55°C to 125°C for the M suffix.

operating characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	$V_{O(PP)}$ = 2 V, R_L = 10 kΩ	C_L = 160 pF,	25°C	1	1.6		V/µs
				Full range	0.8			
V_n	Equivalent input noise voltage	f = 100 Hz		25°C		14		nV/√Hz
		f = 1 kHz		25°C		11		
I_n	Equivalent input noise current	f = 100 Hz		25°C		0.13		pA/√Hz
THD + N	Total harmonic distortion plus noise	$V_{O(PP)}$ = 4 V, R_L = 10 kΩ, f = 10 kHz	A_V = 1	25°C		0.004%		
			A_V = 10			0.01%		
			A_V = 100			0.04%		
$t_{(on)}$	Amplifier turnon time	A_V = 1, R_L = 10 kΩ	Both channels	25°C		7.6		µs
			Channel 1 only, Channel 2 on			7.65		
			Channel 2 only, Channel 1 on			7.25		
$t_{(off)}$	Amplifier turnoff time	A_V = 1, R_L = 10 kΩ	Both channels	25°C		333		ns
			Channel 1 only, Channel 2 on			328		
			Channel 2 only, Channel 1 on			329		
	Gain-bandwidth product	f = 10 kHz, C_L = 160 pF	R_L = 10 kΩ,	25°C		6.4		MHz
t_s	Settling time	$V_{(STEP)PP}$ = 2 V, A_V = –1, C_L = 10 pF, R_L = 10 kΩ	0.1%	25°C		1.53		µs
			0.01%			1.83		
		$V_{(STEP)PP}$ = 2 V, A_V = –1, C_L = 56 pF, R_L = 10 kΩ	0.1%			3.13		
			0.01%			3.33		
ϕ_m	Phase margin at unity gain	R_L = 10 kΩ,	C_L = 160 pF	25°C		45°		
	Gain margin			25°C		7		dB

† Full range is 0°C to 70°C for the C suffix, –40°C to 125°C for the I and Q suffixes, and –55°C to 125°C for the M suffix.

TYPICAL CHARACTERISTICS

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TYPICAL CHARACTERISTICS

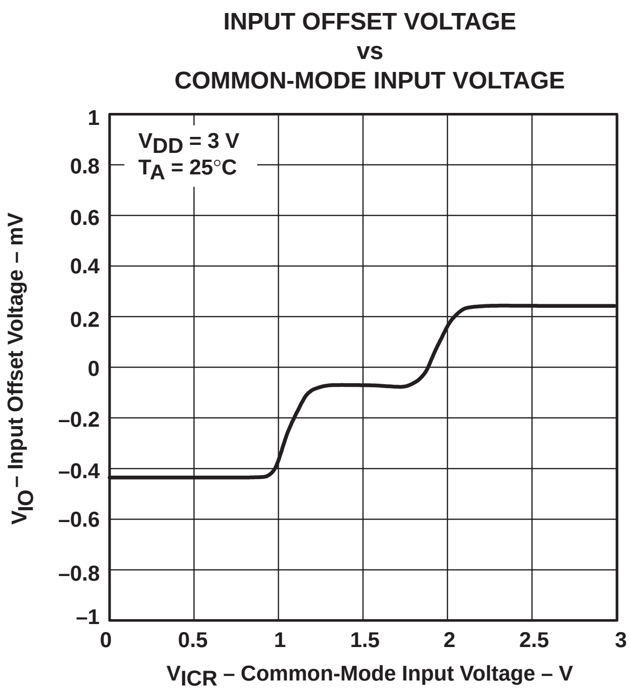


Figure 1

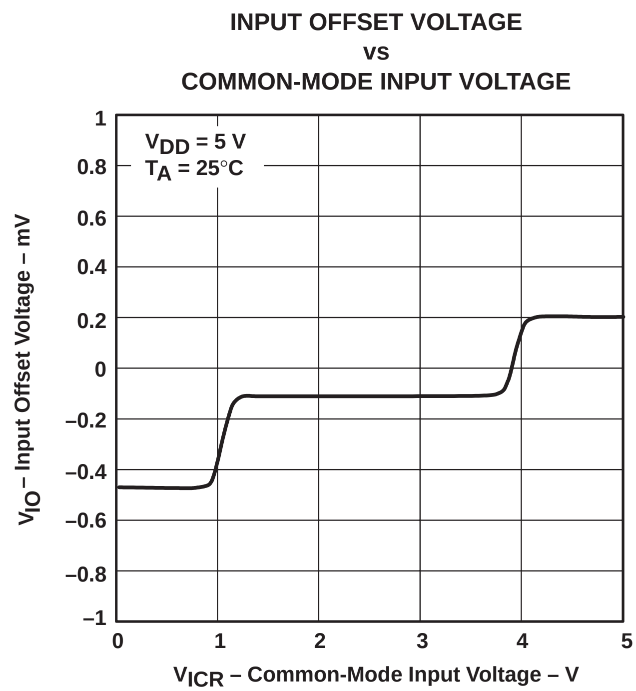


Figure 2

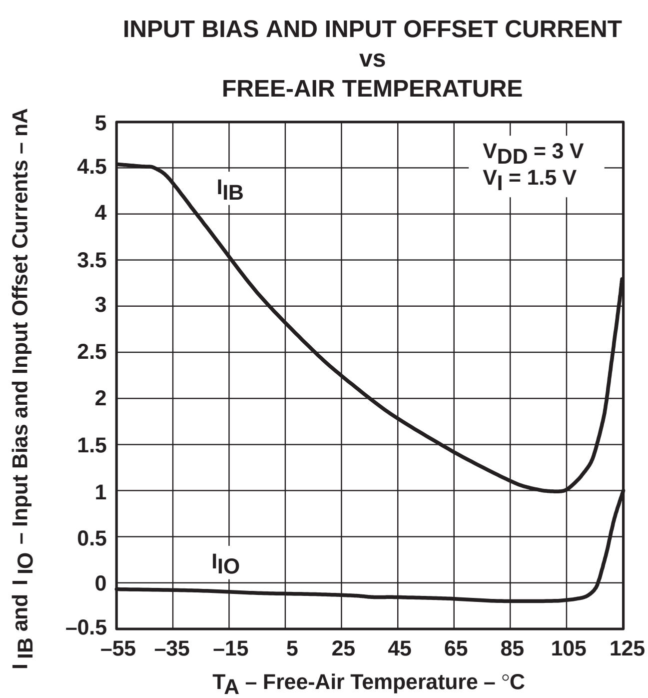


Figure 3

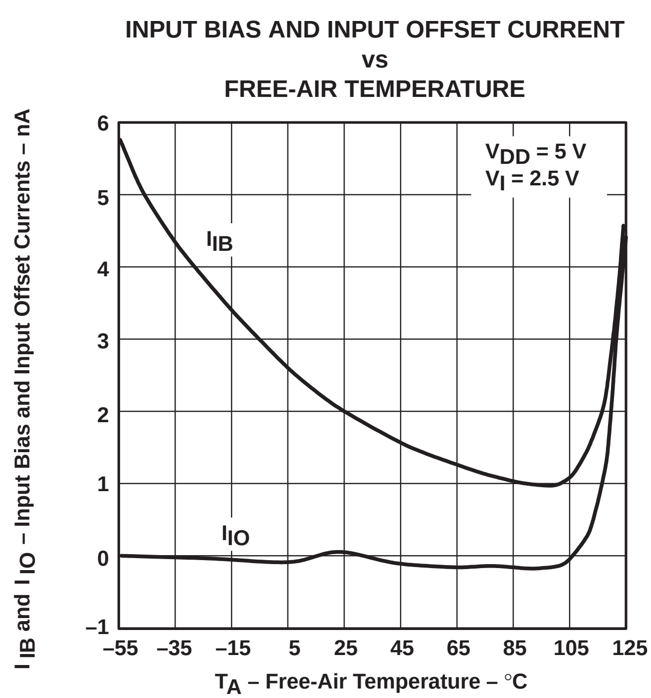


Figure 4

TYPICAL CHARACTERISTICS

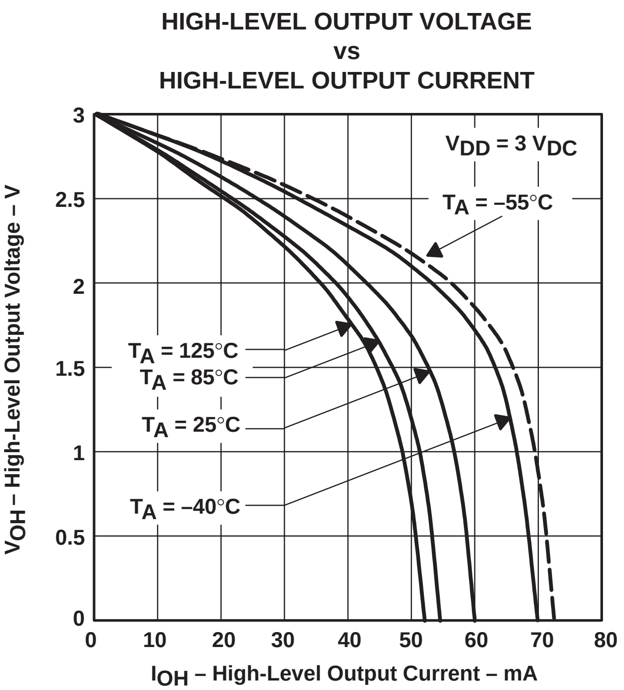


Figure 5

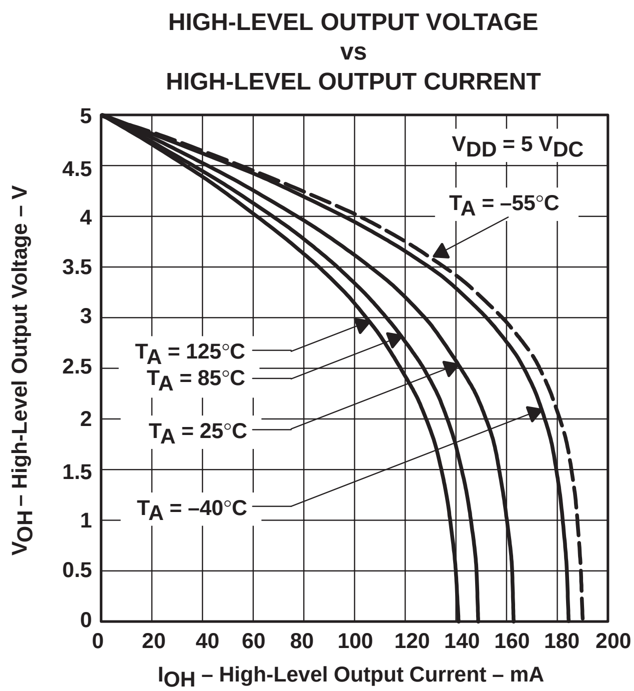


Figure 6

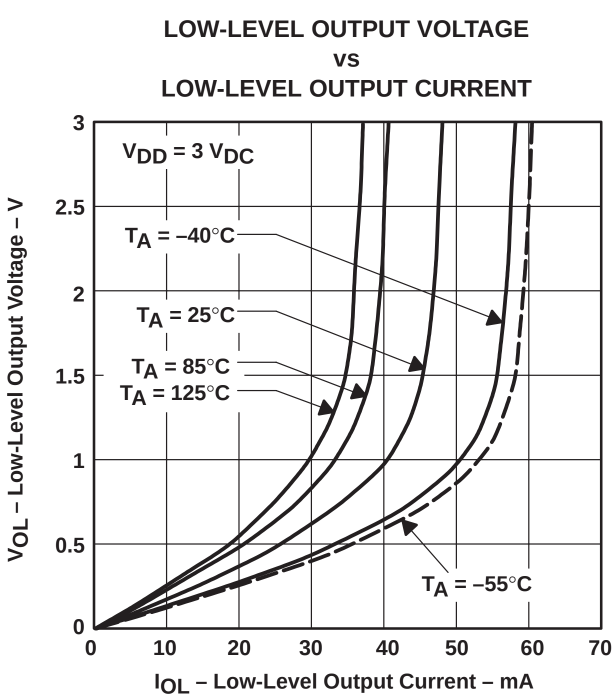


Figure 7

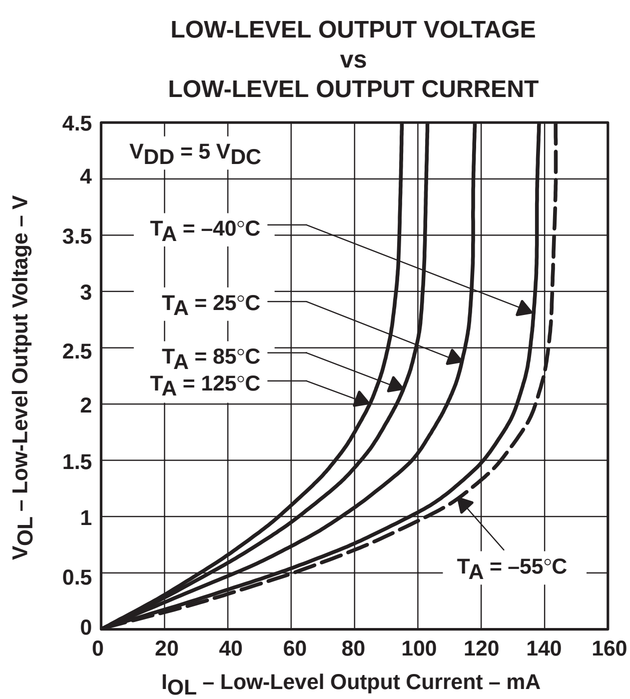


Figure 8

TYPICAL CHARACTERISTICS

PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

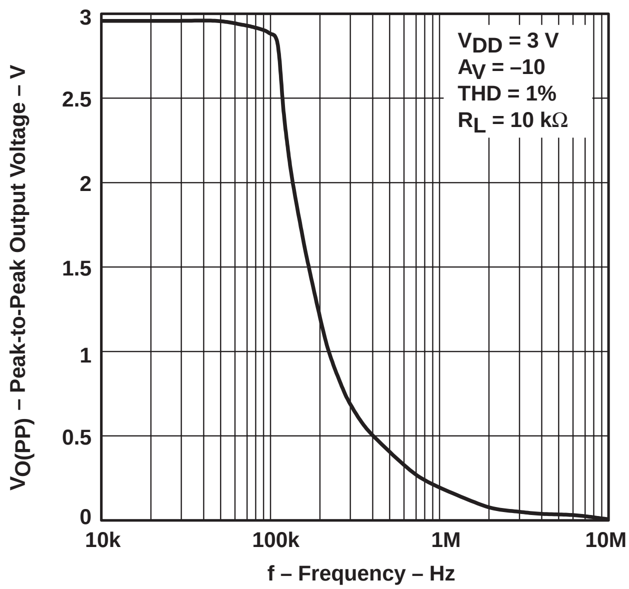


Figure 9

PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

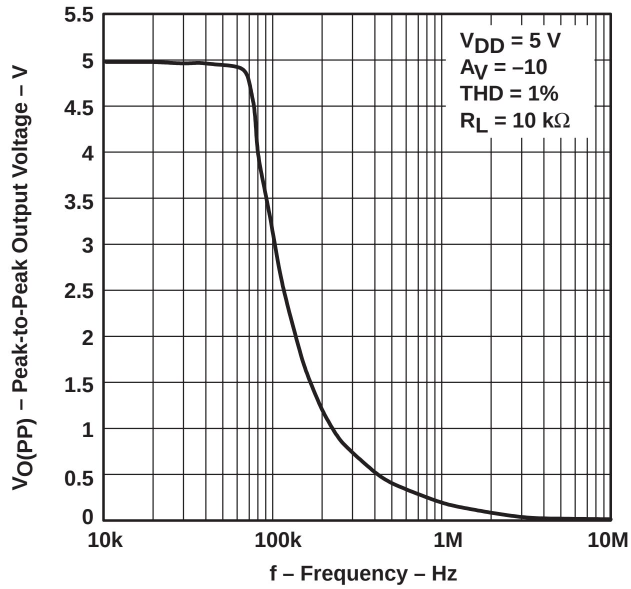


Figure 10

OPEN-LOOP GAIN AND PHASE
vs
FREQUENCY

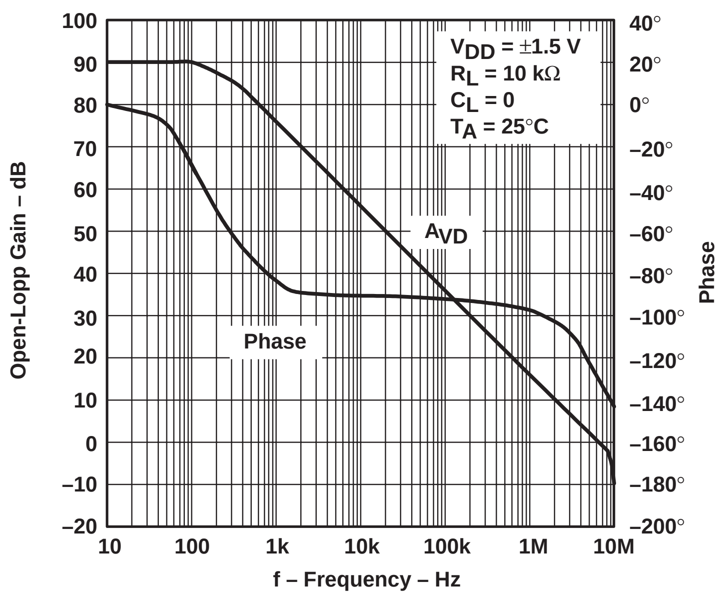


Figure 11

TYPICAL CHARACTERISTICS

**OPEN-LOOP GAIN AND PHASE
vs
FREQUENCY**

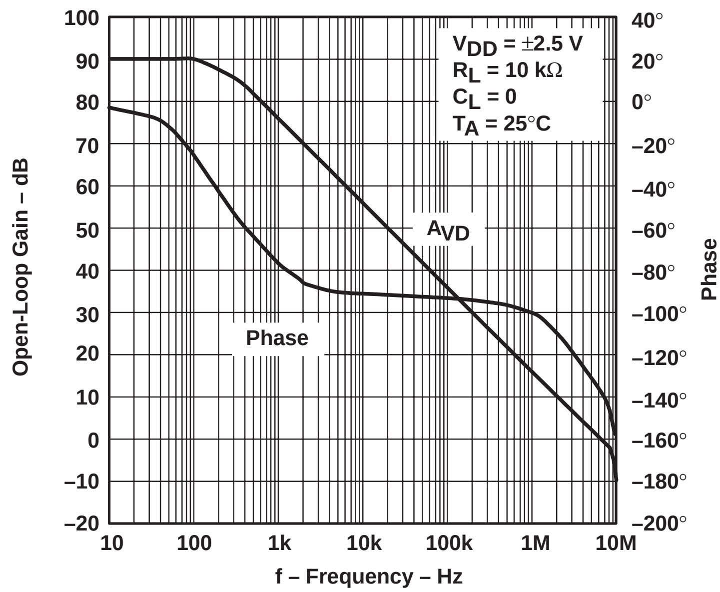


Figure 12

**DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
LOAD RESISTANCE**

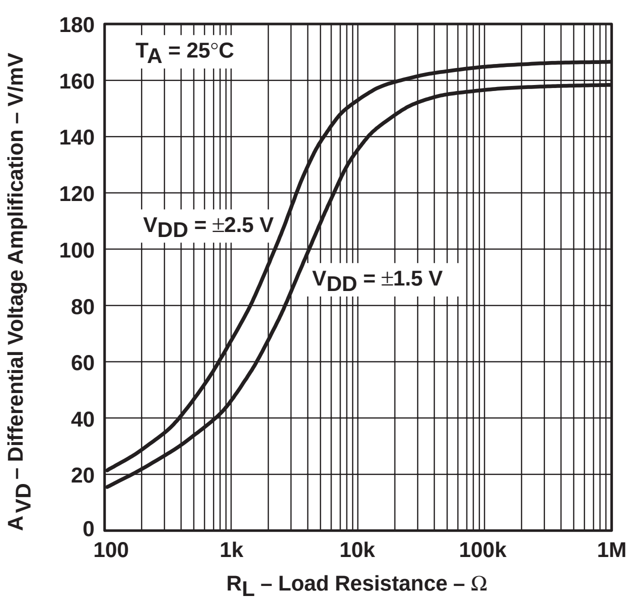


Figure 13

**AMPLIFIER STABILITY
vs
LOAD**

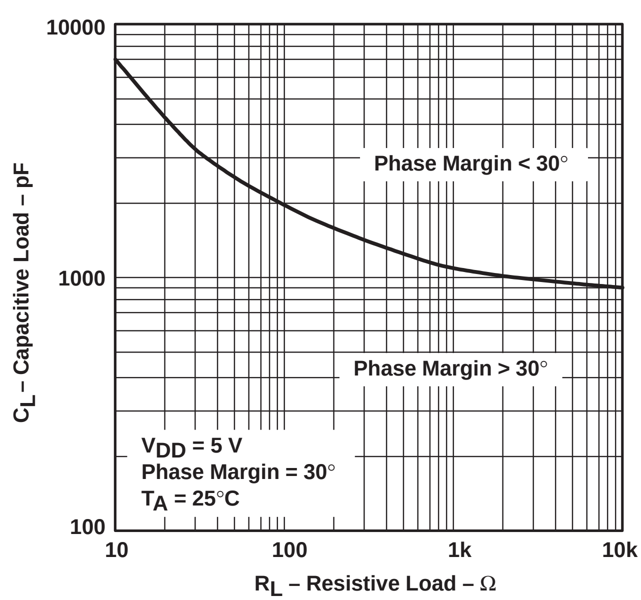


Figure 14

TYPICAL CHARACTERISTICS

OUTPUT IMPEDANCE vs FREQUENCY

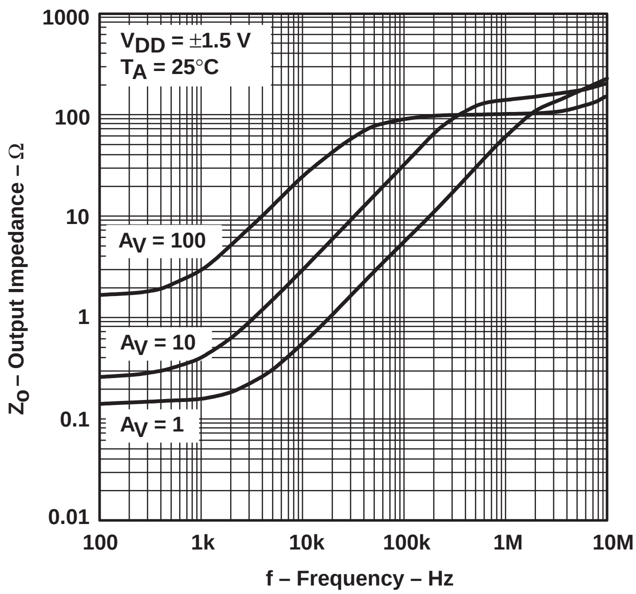


Figure 15

OUTPUT IMPEDANCE vs FREQUENCY

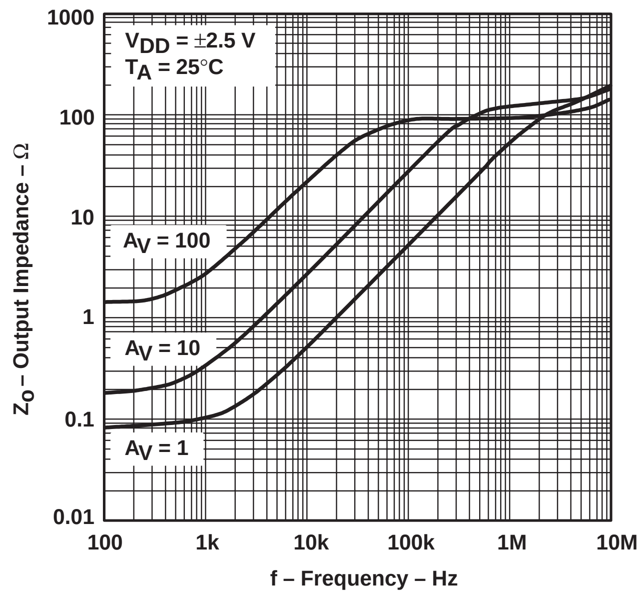


Figure 16

COMMON-MODE REJECTION RATIO vs FREQUENCY

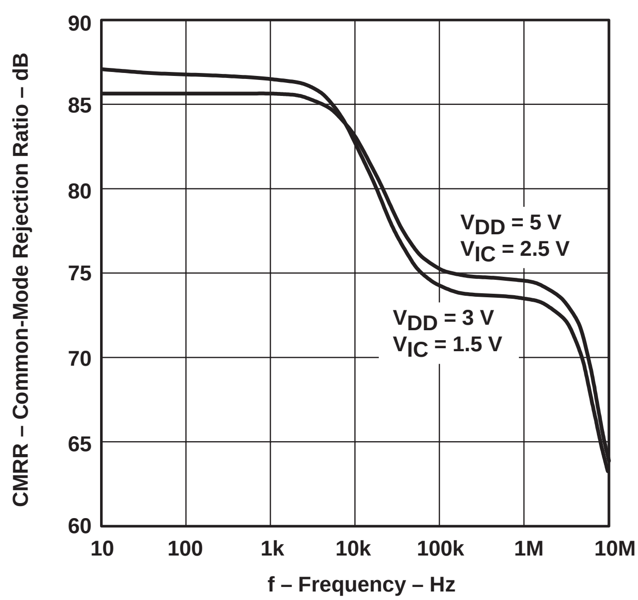


Figure 17

TYPICAL CHARACTERISTICS

SUPPLY-VOLTAGE REJECTION RATIO
vs
FREQUENCY

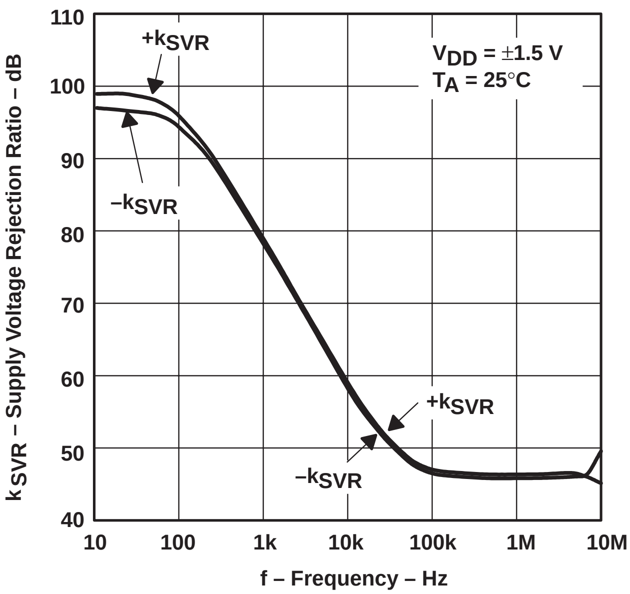


Figure 18

SUPPLY-VOLTAGE REJECTION RATIO
vs
FREQUENCY

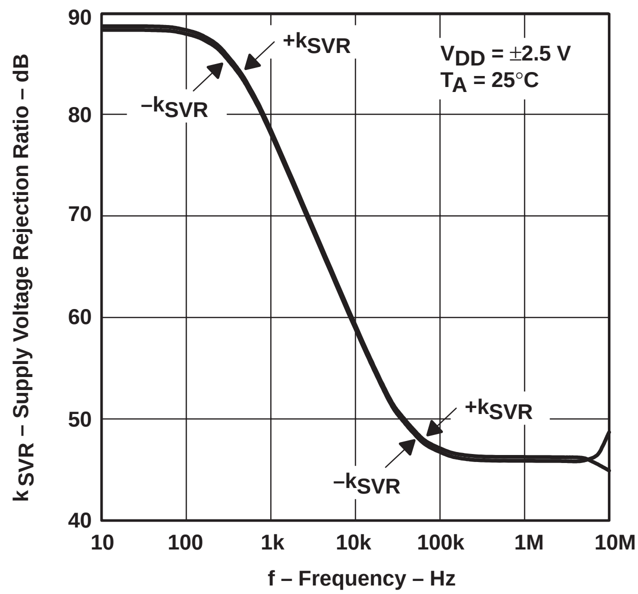


Figure 19

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

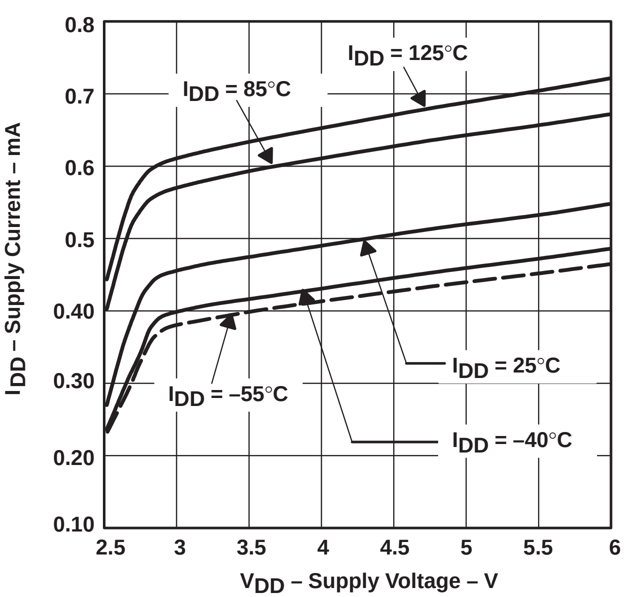


Figure 20

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

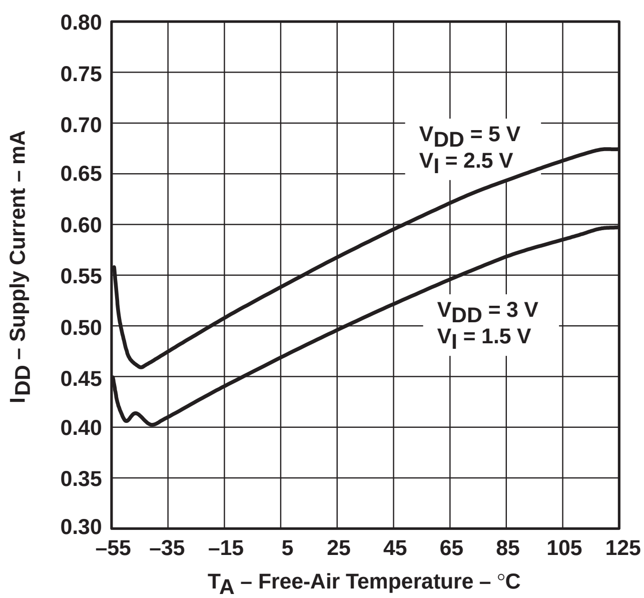


Figure 21

TYPICAL CHARACTERISTICS

AMPLIFIER WITH A SHUTDOWN PULSE TURNON CHARACTERISTICS

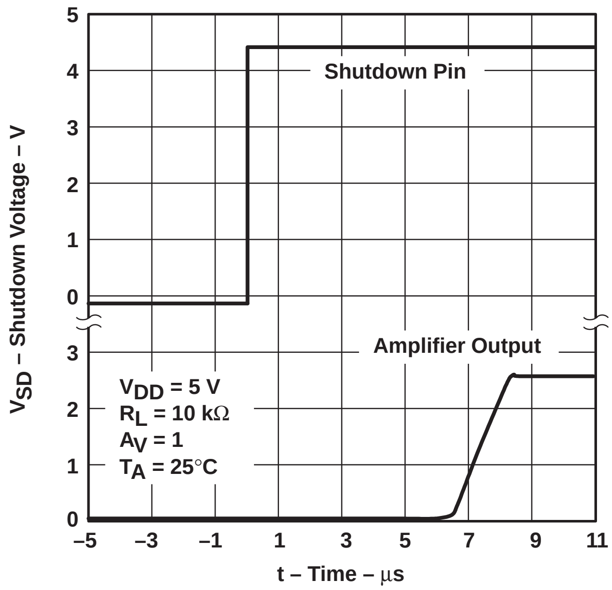


Figure 22

AMPLIFIER WITH A SHUTDOWN PULSE TURNOFF CHARACTERISTICS

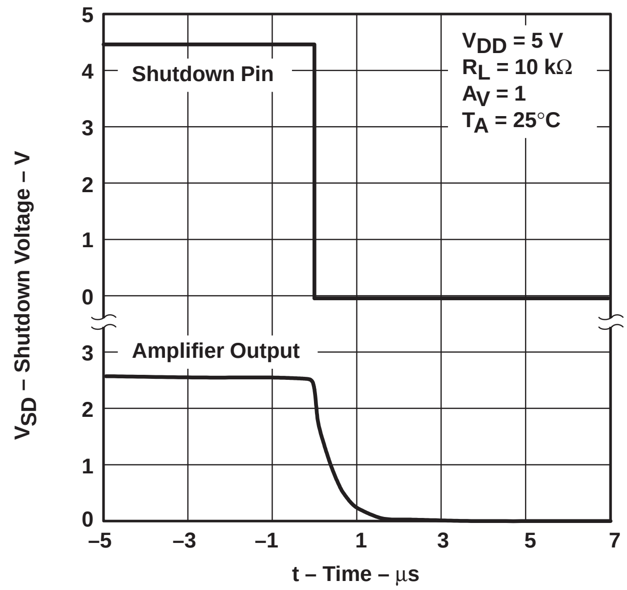


Figure 23

SUPPLY CURRENT WITH A SHUTDOWN PULSE TURNON CHARACTERISTICS

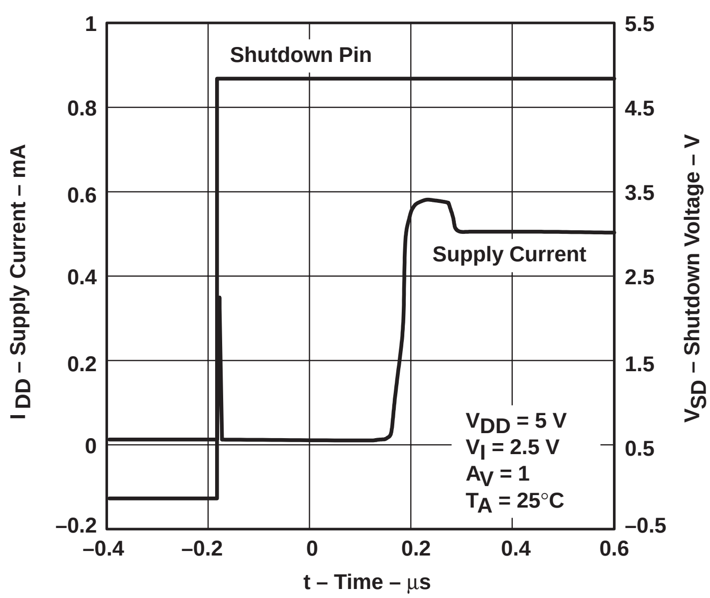


Figure 24

TYPICAL CHARACTERISTICS

TURNOFF SUPPLY CURRENT
WITH A SHUTDOWN PULSE

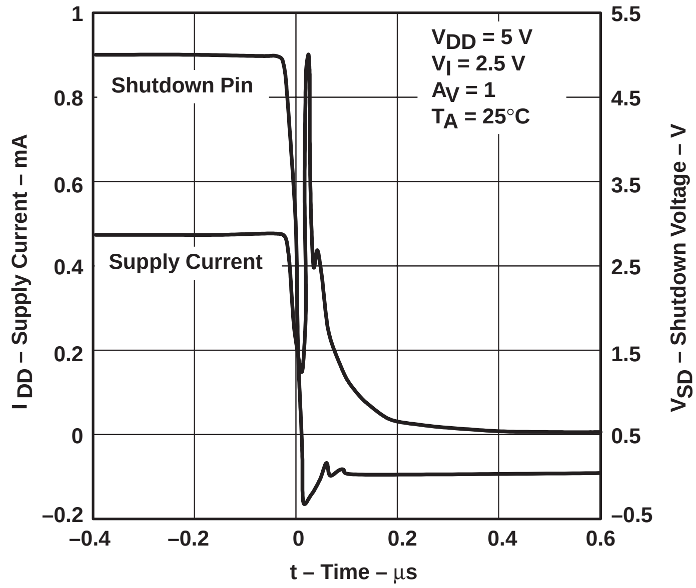


Figure 25

SHUTDOWN SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

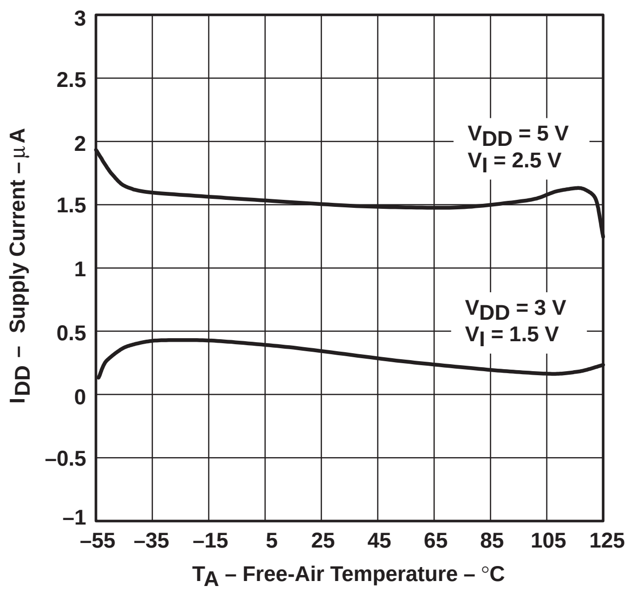


Figure 26

SLEW RATE
vs
SUPPLY VOLTAGE

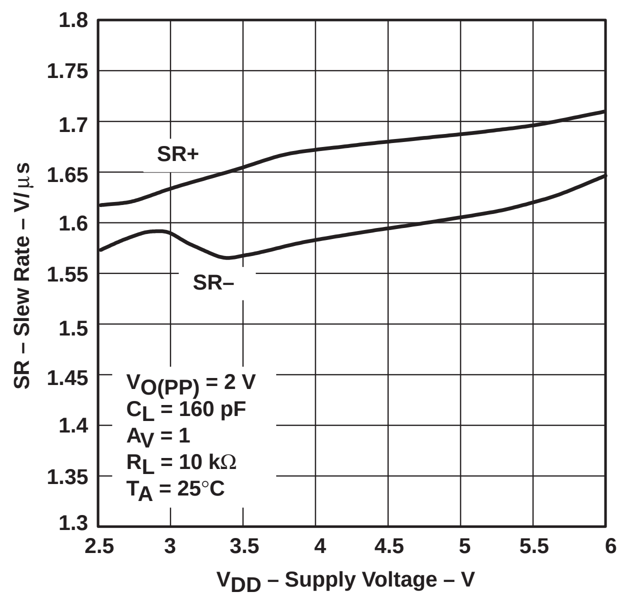


Figure 27

TYPICAL CHARACTERISTICS

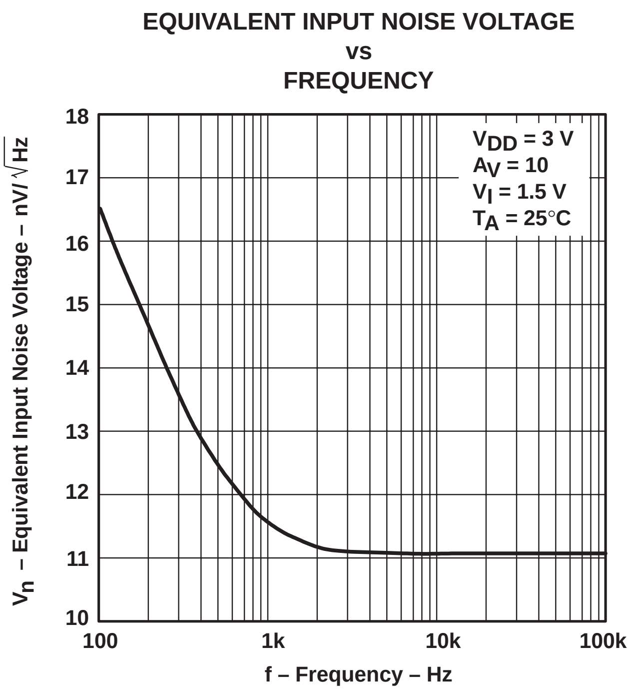


Figure 28

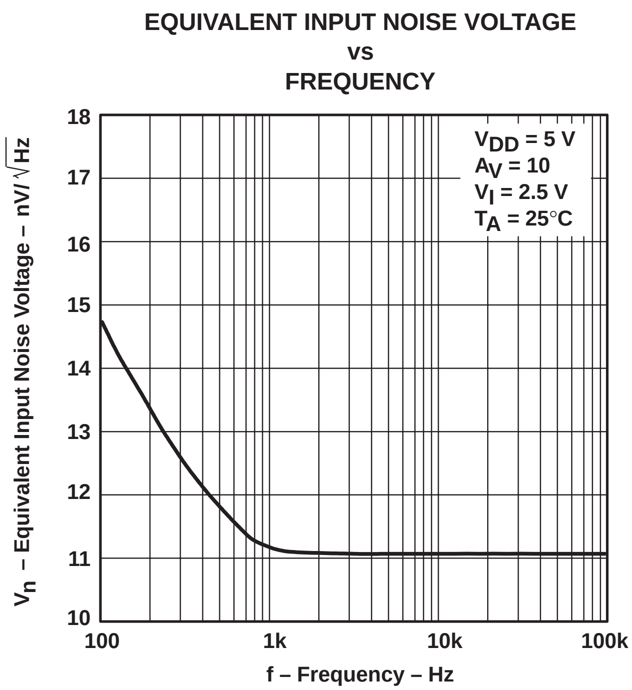


Figure 29

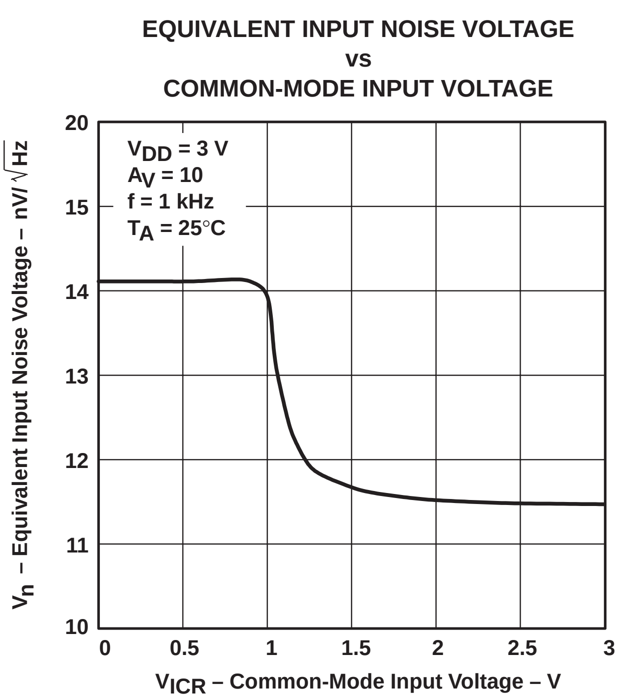


Figure 30

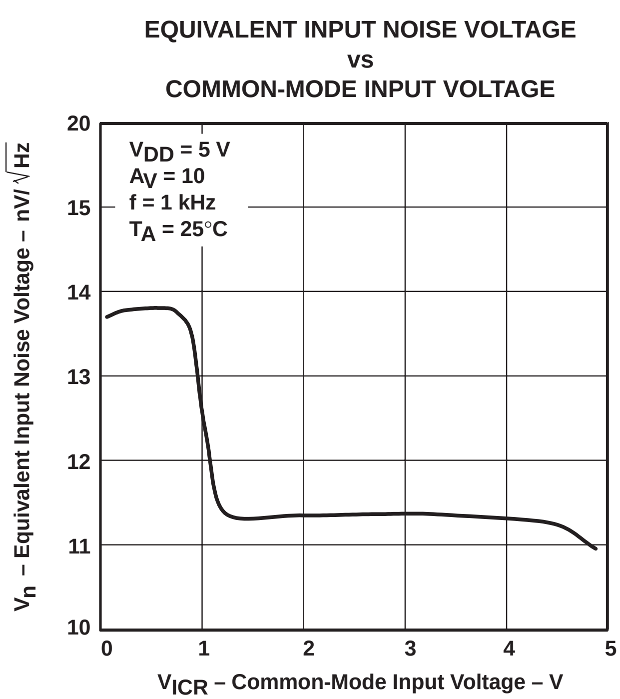


Figure 31

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION vs FREQUENCY

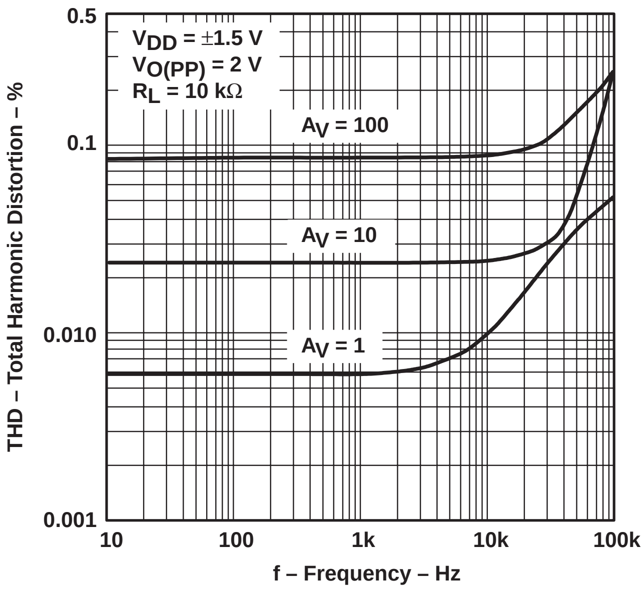


Figure 32

TOTAL HARMONIC DISTORTION vs FREQUENCY

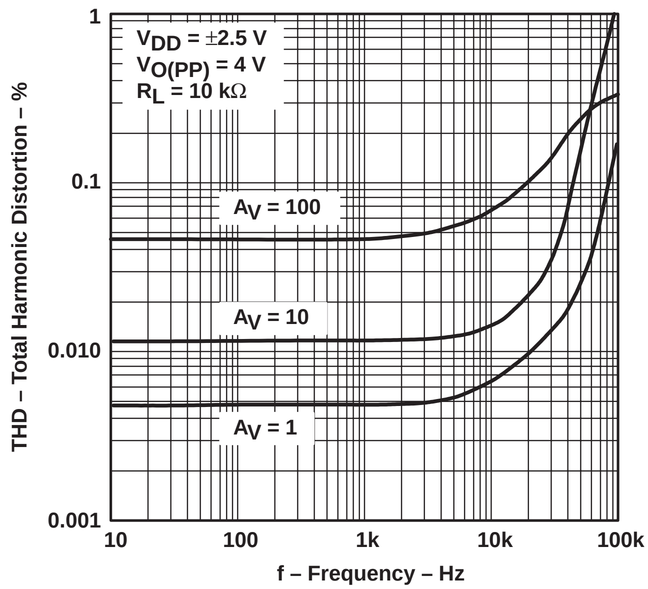


Figure 33

TOTAL HARMONIC DISTORTION PLUS NOISE vs PEAK-TO-PEAK SIGNAL AMPLITUDE

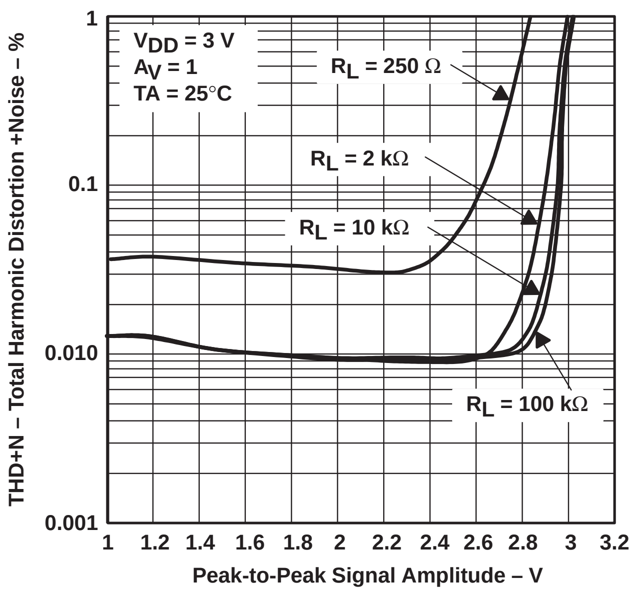


Figure 34

TOTAL HARMONIC DISTORTION PLUS NOISE vs PEAK-TO-PEAK SIGNAL AMPLITUDE

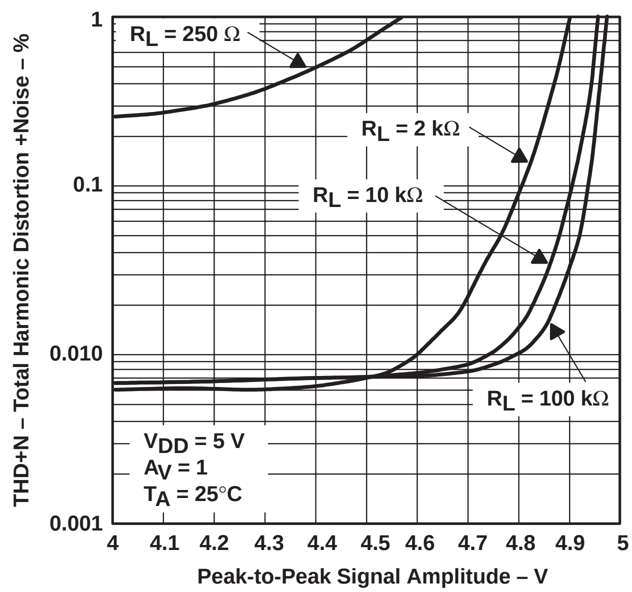


Figure 35

TYPICAL CHARACTERISTICS

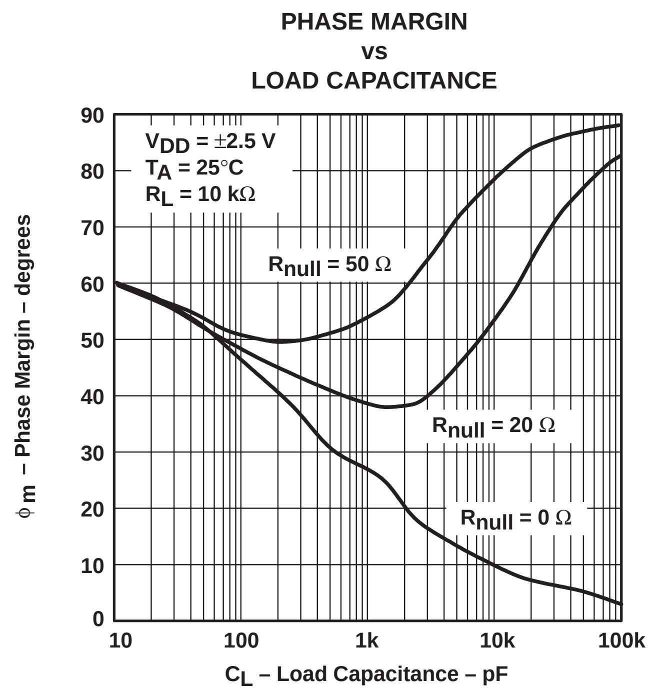


Figure 36

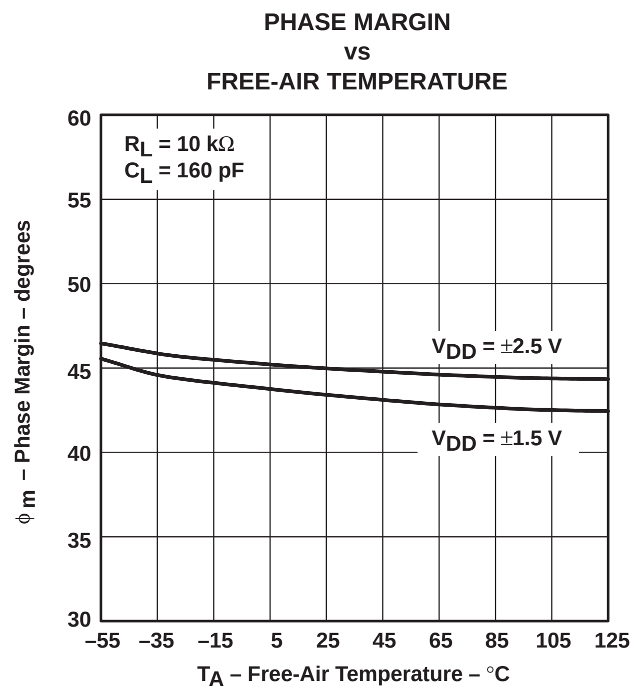


Figure 37

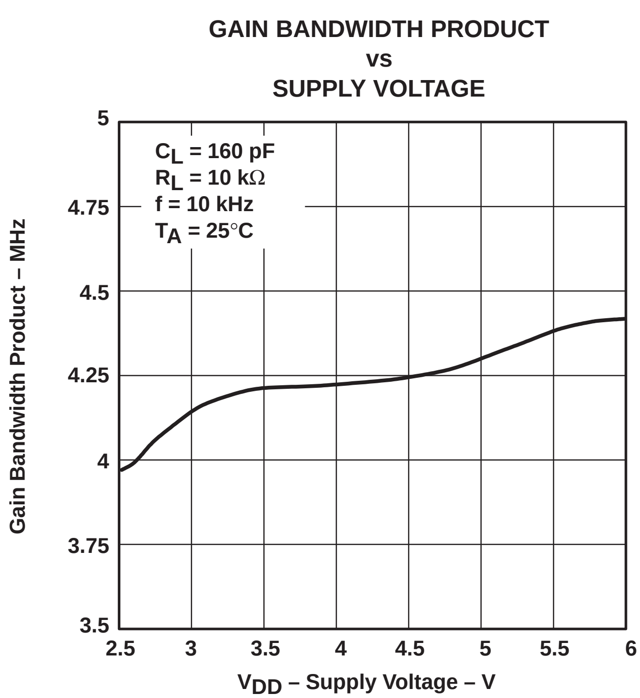


Figure 38

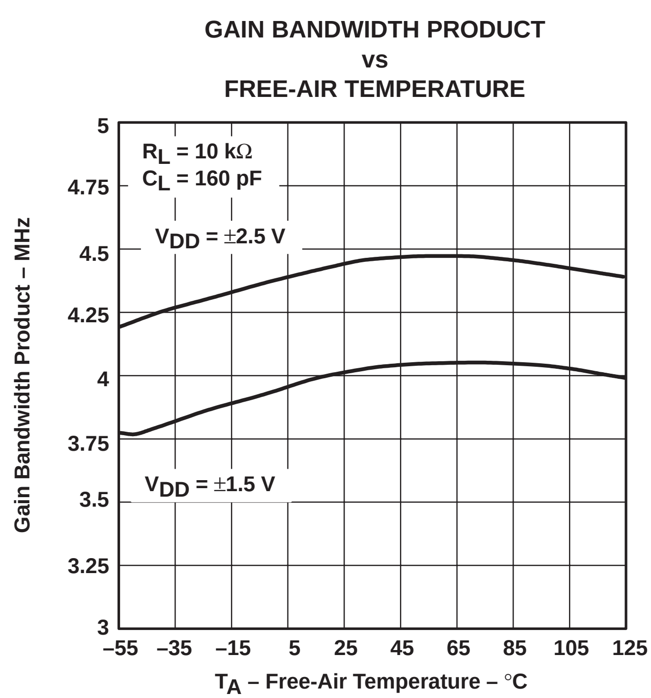


Figure 39

TYPICAL CHARACTERISTICS

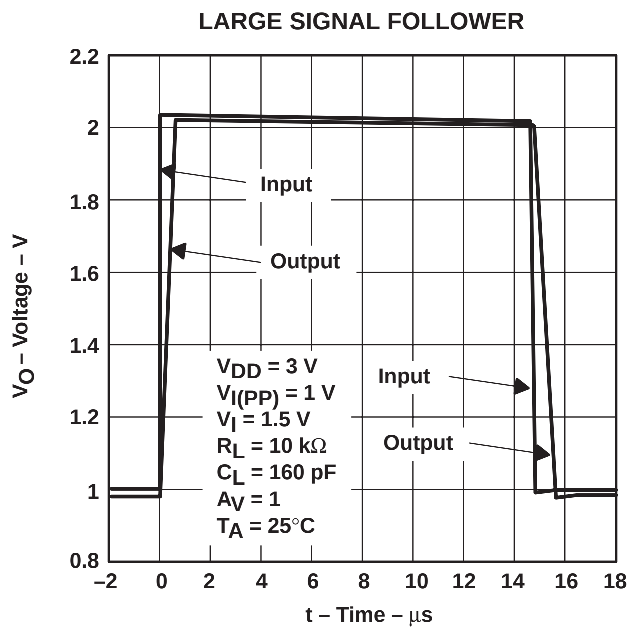


Figure 40

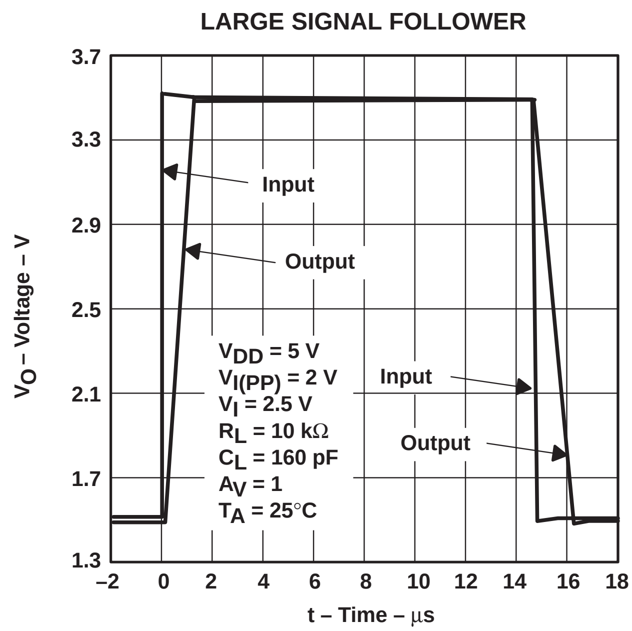


Figure 41

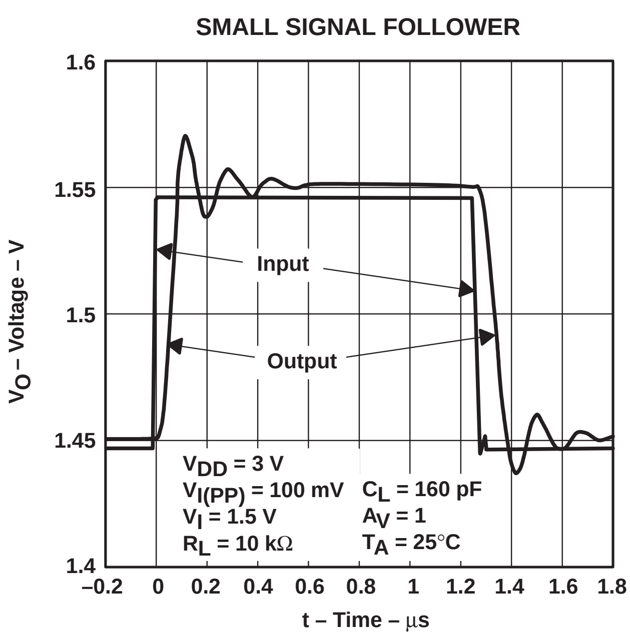


Figure 42

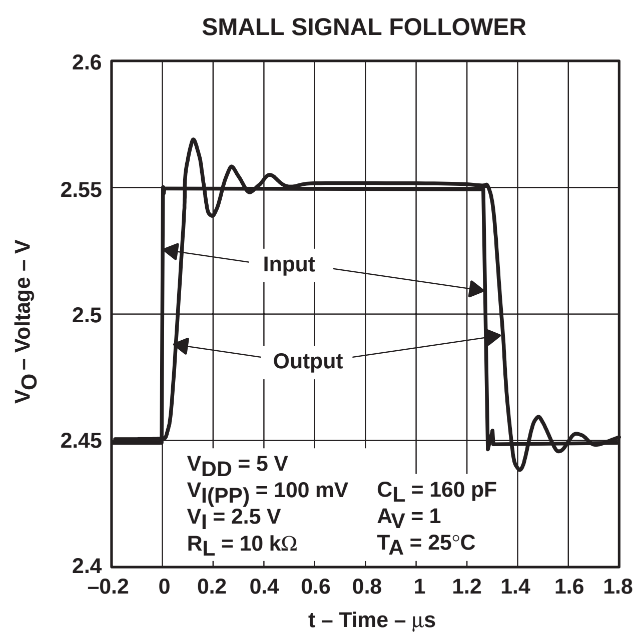


Figure 43

TYPICAL CHARACTERISTICS

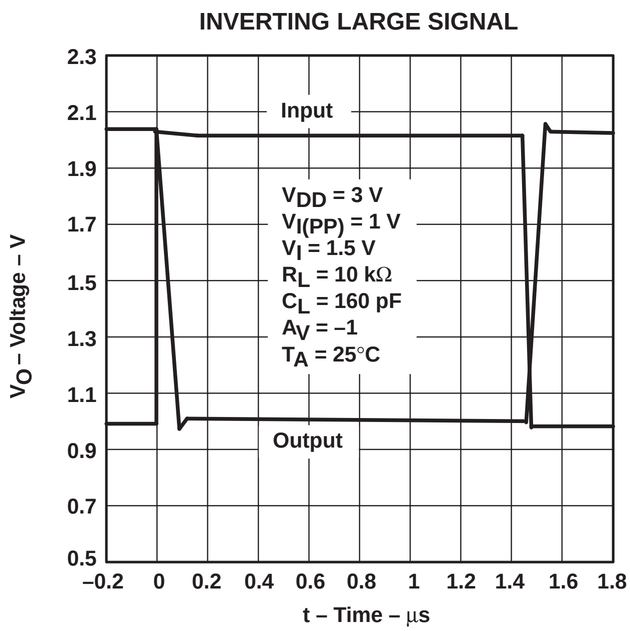


Figure 44

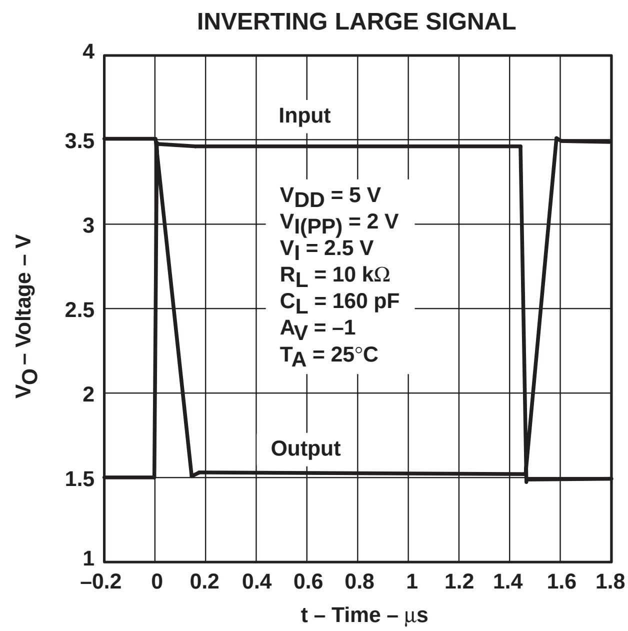


Figure 45

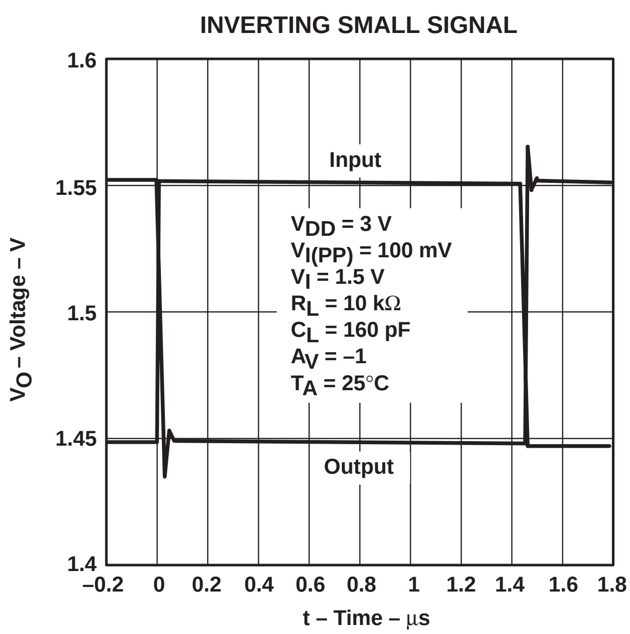


Figure 46

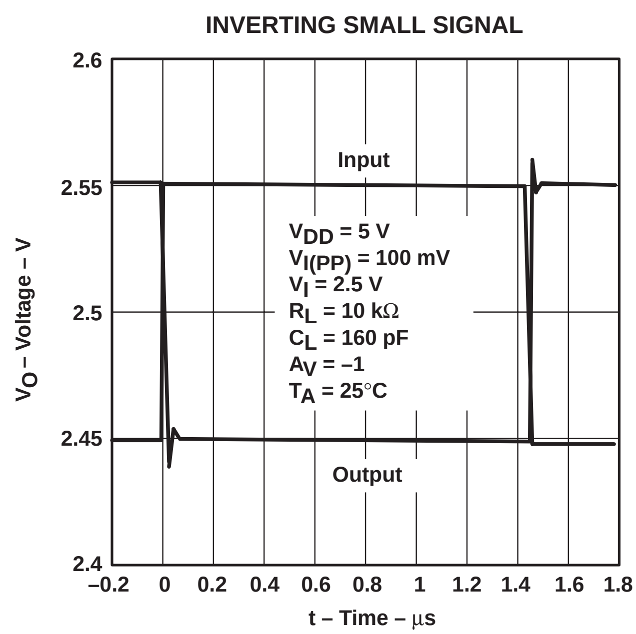


Figure 47

PARAMETER MEASUREMENT INFORMATION

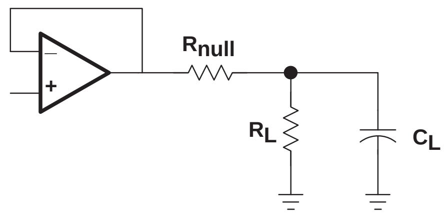


Figure 48

APPLICATION INFORMATION

driving a capacitive load

When the amplifier is configured in this manner, capacitive loading directly on the output will decrease the device’s phase margin leading to high frequency ringing or oscillations. Therefore, for capacitive loads of greater than 10 pF, it is recommended that a resistor be placed in series (R_{NULL}) with the output of the amplifier, as shown in Figure 49. A minimum value of 20 Ω should work well for most applications.

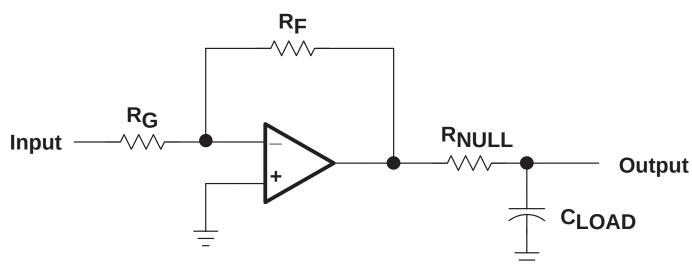
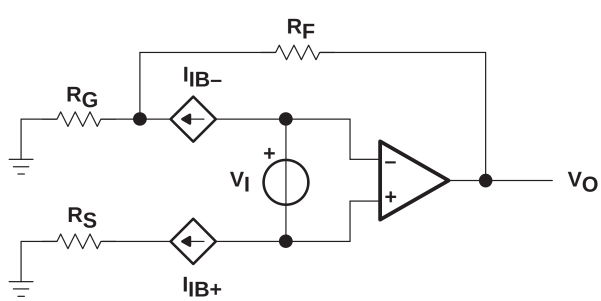


Figure 49. Driving a Capacitive Load

offset voltage

The output offset voltage, (V_{OO}) is the sum of the input offset voltage (V_{IO}) and both input bias currents (I_{IB}) times the corresponding gains. The following schematic and formula can be used to calculate the output offset voltage:



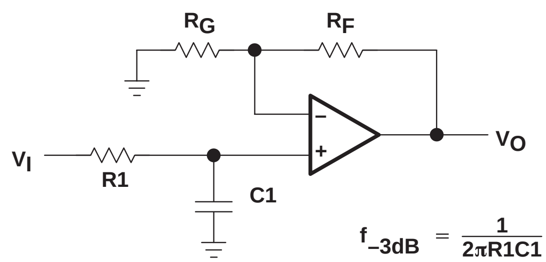
$$V_{OO} = V_{IO}\left(1 + \left(\frac{R_F}{R_G}\right)\right) \pm I_{IB+}\,R_S\left(1 + \left(\frac{R_F}{R_G}\right)\right) \pm I_{IB-}\,R_F$$

Figure 50. Output Offset Voltage Model

APPLICATION INFORMATION

general configurations

When receiving low-level signals, limiting the bandwidth of the incoming signals into the system is often required. The simplest way to accomplish this is to place an RC filter at the noninverting terminal of the amplifer (see Figure 51).

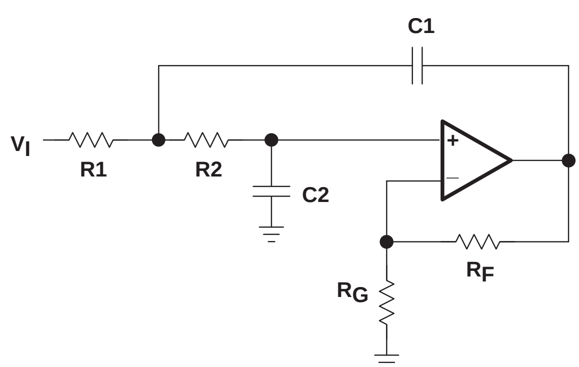


$$f_{-3dB} = \frac{1}{2\pi R1C1}$$

$$\frac{V_O}{V_I} = \left(1 + \frac{R_F}{R_G}\right)\left(\frac{1}{1 + sR1C1}\right)$$

Figure 51. Single-Pole Low-Pass Filter

If even more attenuation is needed, a multiple pole filter is required. The Sallen-Key filter can be used for this task. For best results, the amplifier should have a bandwidth that is 8 to 10 times the filter frequency bandwidth. Failure to do this can result in phase shift of the amplifier.



R1 = R2 = R
C1 = C2 = C
Q = Peaking Factor
(Butterworth Q = 0.707)

$$f_{-3dB} = \frac{1}{2\pi RC}$$

$$R_G = \frac{R_F}{\left(2 - \frac{1}{Q}\right)}$$

Figure 52. 2-Pole Low-Pass Sallen-Key Filter

APPLICATION INFORMATION

shutdown function

Three members of the TLV246x family (TLV2460/3/5) have a shutdown terminal for conserving battery life in portable applications. When the shutdown terminal is tied low, the supply current is reduced to 0.3 μA/channel, the amplifier is disabled, and the outputs are placed in a high impedance mode. To enable the amplifier, the shutdown terminal can either be left floating or pulled high. When the shutdown terminal is left floating, care should be taken to ensure that parasitic leakage current at the shutdown terminal does not inadvertently place the operational amplifier into shutdown. The shutdown terminal threshold is always referenced to $V_{DD}/2$. Therefore, when operating the device with split supply voltages (e.g. ±2.5 V), the shutdown terminal needs to be pulled to $V_{DD}–$ (not GND) to disable the operational amplifier.

The amplifier's output with a shutdown pulse is shown in Figures 22, 23, 24, and 25. The amplifier is powered with a single 5-V supply and configured as a noninverting configuration with a gain of 5. The amplifier turnon and turnoff times are measured from the 50% point of the shutdown pulse to the 50% point of the output waveform. The times for the single, dual, and quad are listed in the data tables.

circuit layout considerations

To achieve the levels of high performance of the TLV246x, follow proper printed-circuit board design techniques. A general set of guidelines is given in the following.

- Ground planes – It is highly recommended that a ground plane be used on the board to provide all components with a low inductive ground connection. However, in the areas of the amplifier inputs and output, the ground plane can be removed to minimize the stray capacitance.
- Proper power supply decoupling – Use a 6.8-μF tantalum capacitor in parallel with a 0.1-μF ceramic capacitor on each supply terminal. It may be possible to share the tantalum among several amplifiers depending on the application, but a 0.1-μF ceramic capacitor should always be used on the supply terminal of every amplifier. In addition, the 0.1-μF capacitor should be placed as close as possible to the supply terminal. As this distance increases, the inductance in the connecting trace makes the capacitor less effective. The designer should strive for distances of less than 0.1 inches between the device power terminals and the ceramic capacitors.
- Sockets – Sockets can be used but are not recommended. The additional lead inductance in the socket pins will often lead to stability problems. Surface-mount packages soldered directly to the printed-circuit board is the best implementation.
- Short trace runs/compact part placements – Optimum high performance is achieved when stray series inductance has been minimized. To realize this, the circuit layout should be made as compact as possible, thereby minimizing the length of all trace runs. Particular attention should be paid to the inverting input of the amplifier. Its length should be kept as short as possible. This will help to minimize stray capacitance at the input of the amplifier.
- Surface-mount passive components – Using surface-mount passive components is recommended for high performance amplifier circuits for several reasons. First, because of the extremely low lead inductance of surface-mount components, the problem with stray series inductance is greatly reduced. Second, the small size of surface-mount components naturally leads to a more compact layout thereby minimizing both stray inductance and capacitance. If leaded components are used, it is recommended that the lead lengths be kept as short as possible.

APPLICATION INFORMATION

general power dissipation considerations

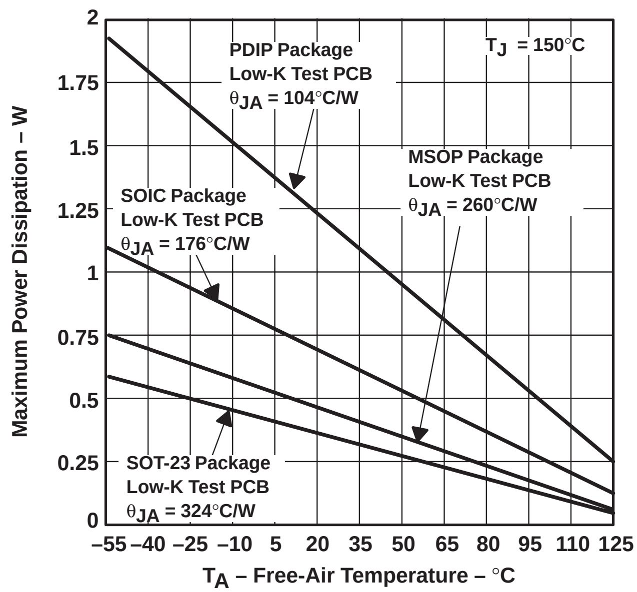
For a given θ_{JA}, the maximum power dissipation is shown in Figure 53 and is calculated by the following formula:

$$P_D = \left(\frac{T_{MAX} - T_A}{\theta_{JA}}\right)$$

Where:

P_D = Maximum power dissipation of THS246x IC (watts)
T_{MAX} = Absolute maximum junction temperature (150°C)
T_A = Free-ambient air temperature (°C)
$\theta_{JA} = \theta_{JC} + \theta_{CA}$
θ_{JC} = Thermal coefficient from junction to case
θ_{CA} = Thermal coefficient from case to ambient air (°C/W)

MAXIMUM POWER DISSIPATION
vs
FREE-AIR TEMPERATURE



NOTE A: Results are with no air flow and using JEDEC Standard Low-K test PCB.

Figure 53. Maximum Power Dissipation vs Free-Air Temperature

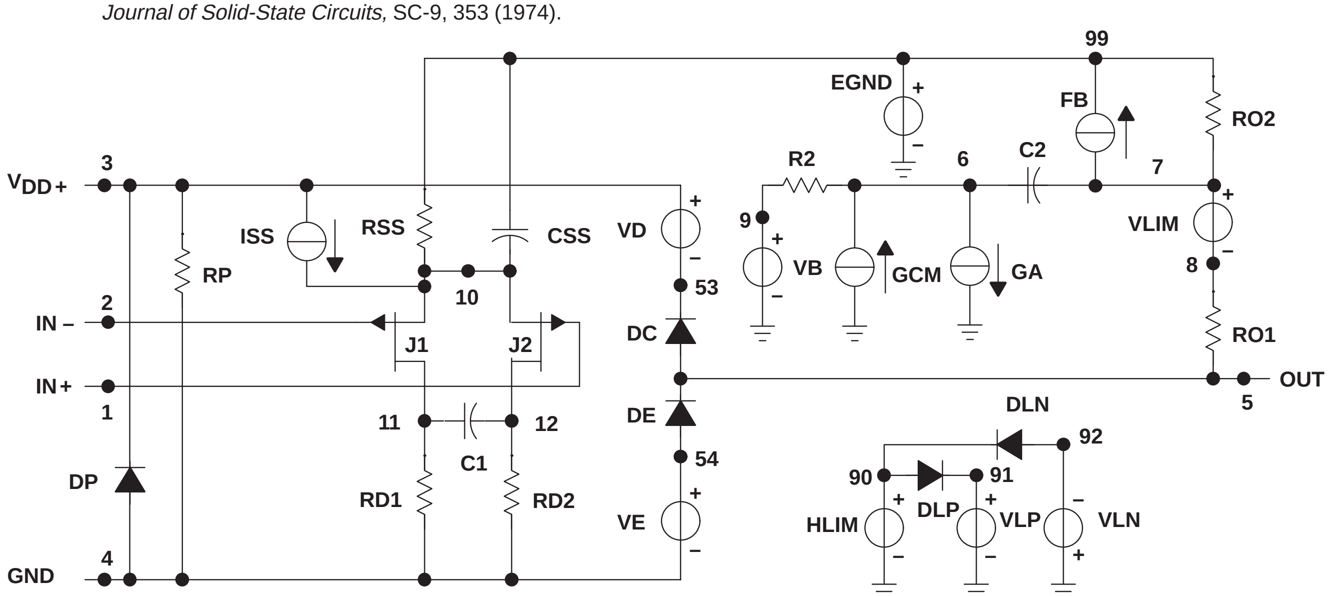
APPLICATION INFORMATION

macromodel information

Macromodel information provided was derived using Microsim *Parts*™ Release 8, the model generation software used with Microsim *PSpice*™. The Boyle macromodel (see Note 2) and subcircuit in Figure 54 are generated using the TLV246x typical electrical and operating characteristics at T_A = 25°C. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Unity-gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

NOTE 2: G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, “Macromodeling of Intergrated Circuit Operational Amplifiers”, *IEEE Journal of Solid-State Circuits,* SC-9, 353 (1974).




```
.SUBCKT TLV246X   1 2 3 4 5
    C1     11   12   2.46034E–12
    C2     6    7    10.0000E–12
    CSS    10   99   443.21E–15
    DC     5    53   DY
    DE     54   5    DY
    DLP    90   91   DX
    DLN    92   90   DX
    DP     4    3    DX
    EGND   99   0    POLY (2) (3,0) (4,0) 0 .5 .5
    FB     7    99   POLY (5) VB VC VE VLP
    + VLN 0 21.600E6 –1E3 1E3 22E6 –22E6
    GA     6    0    11     12 345.26E–6
    GCM    0    6    10     99 15.4226E–9
    ISS    10   4    DC 18.850E–6
    HLIM   90   0    VLIM 1K
    J1     11   2    10 JX1
    J2     12   1    10 JX2
    R2     6    9    100.00E3
RD1    3    11   2.8964E3
RD2    3    12   2.8964E3
R01    8    5    5.6000
R02    7    99   6.2000
RP     3    4    8.9127
RSS    10   99   10.610E6
VB     9    0    DC 0
VC     3    53   DC .7836
VE     54   4    DC .7436
VLIM   7    8    DC 0
VLP    91   0    DC 117
VLN    0    92   DC 117
.MODEL DX D (IS=800.00E–18)
.MODEL DY D (IS=800.00E–18 Rs = 1m Cjo=10p)
.MODEL JX1 NJF (IS=1.0000E–12 BETA=6.3239E–3
+ VTO=–1)
.MODEL JX2 NJF (IS=1.0000E–12 BETA=6.3239E–3
+ VTO=–1)
.ENDS
```

Figure 54. Boyle Macromodels and Subcircuit

PSpice and *Parts* are trademarks of MicroSim Corporation.

macromodel information (continued)

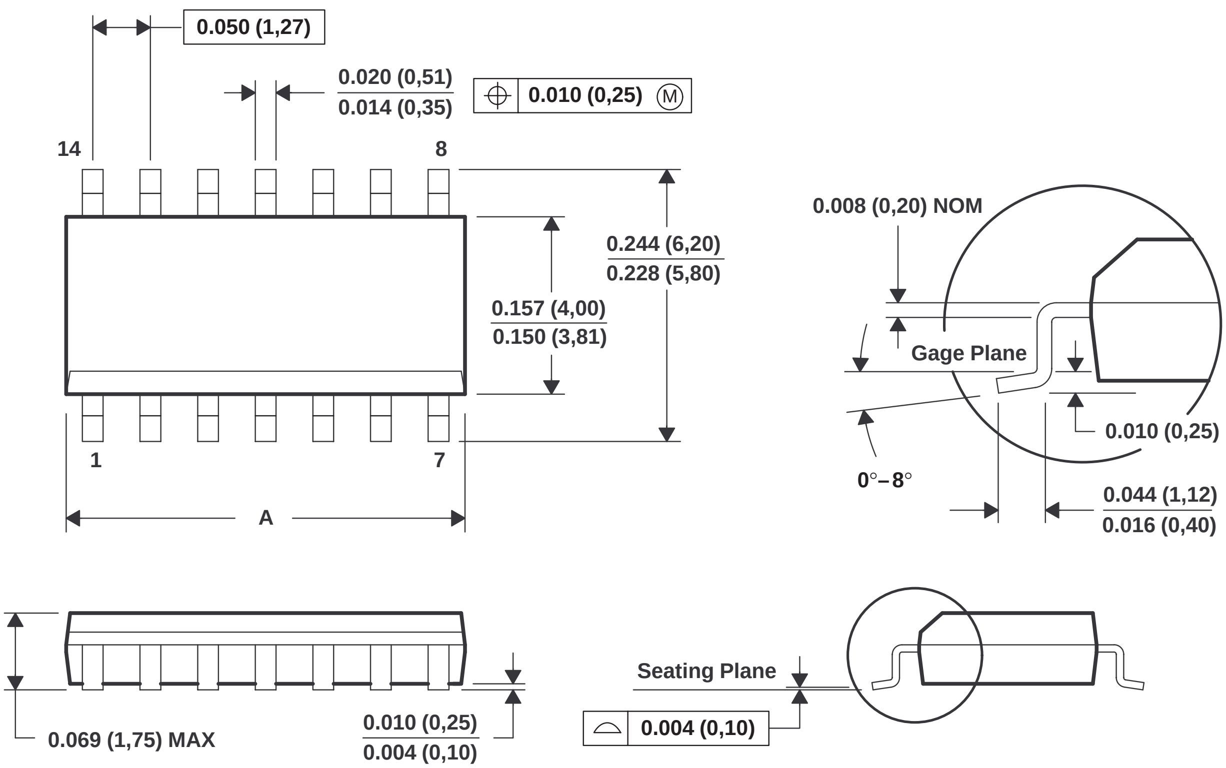
```
.subckt TLV_246Y 1 2 3 4 5 6
        c1      11      12      2.4603E–12
        c2      72      7       10.000E–12
        css     10      99      443.21E–15
        dc      70      53      dy
        de      54      70      dy
        dlp     90      91      dx
        dln     92      90      dx
        dp      4       3       dx
        egnd    99      0       poly(2) (3,0) (4,0) 0 .5 .5
        fb      7       99      poly(5) vb vc ve vlp vln 0
21.600E6 –1E3 1E3 22E6 –22E6
        ga      72      0       11 12 345.26E–6
        gcm     0       72      10 99 15.422E–9
        iss     74      4       dc 18.850E–6
        hlim    90      0       vlim 1K
        j1      11      2       10 jx1
        j2      12      1       10 jx2
        r2      72      9       100.00E3
        rd1     3       11      2.8964E3
        rd2     3       12      2.8964E3
        ro1     8       70      5.6000
        ro2     7       99      6.2000
        rp      3       71      8.9127
        rss     10      99      10.610E6
        rs1     6       4       1G
        rs2     6       4       1G
        rs3     6       4       1G
        rs4     6       4       1G
        s1      71      4       6  4  s1x
        s2      70      5       6  4  s1x
        s3      10      74      6  4  s1x
        s4      74      4       6  4  s2x
        vb      9       0       dc 0
        vc      3       53      dc .7836
        ve      54      4       dc .7436
        vlim    7       8       dc 0
        vlp     91      0       dc 117
        vln     0       92      dc 117
.model dx D(Is=800.00E–18)
.model dy D(Is=800.00E–18 Rs=1m Cjo=10p)
.model jx1 NJF(Is=1.0000E–12 Beta=6.3239E–3 Vto=–1)
.model jx2 NJF(Is=1.0000E–12 Beta=6.3239E–3 Vto=–1)
.model s1x VSWITCH(Roff=1E8 Ron=1.0 Voff=2.5 Von=0.0)
.model s2x  VSWITCH(Roff=1E8 Ron=1.0 Voff=0 Von=2.5)
.ends
```

Figure 54. Boyle Macromodels and Subcircuit (Continued)

MECHANICAL DATA

D (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PIN SHOWN



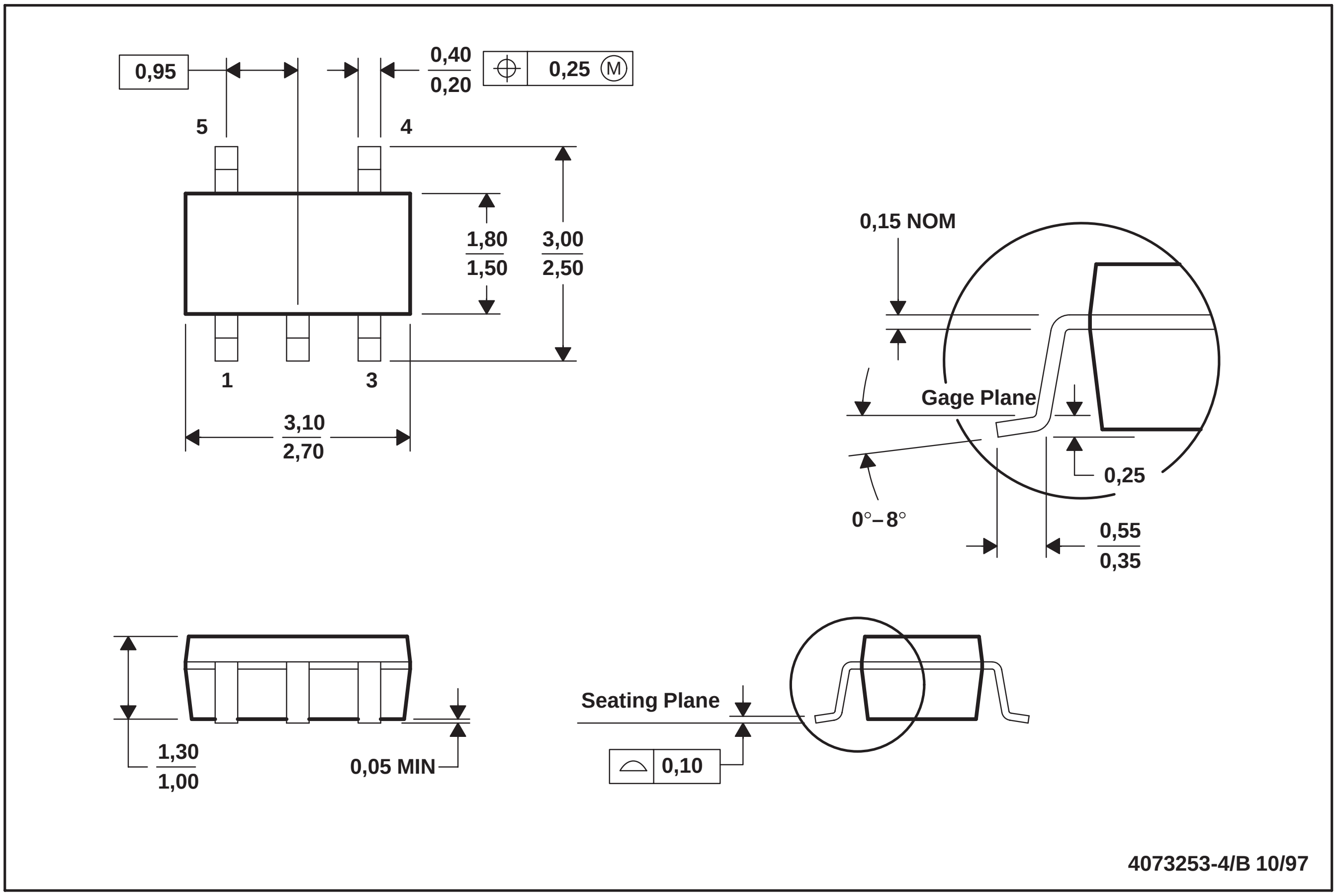
DIM \ PINS **	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

4040047/D 10/96

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-012

MECHANICAL DATA

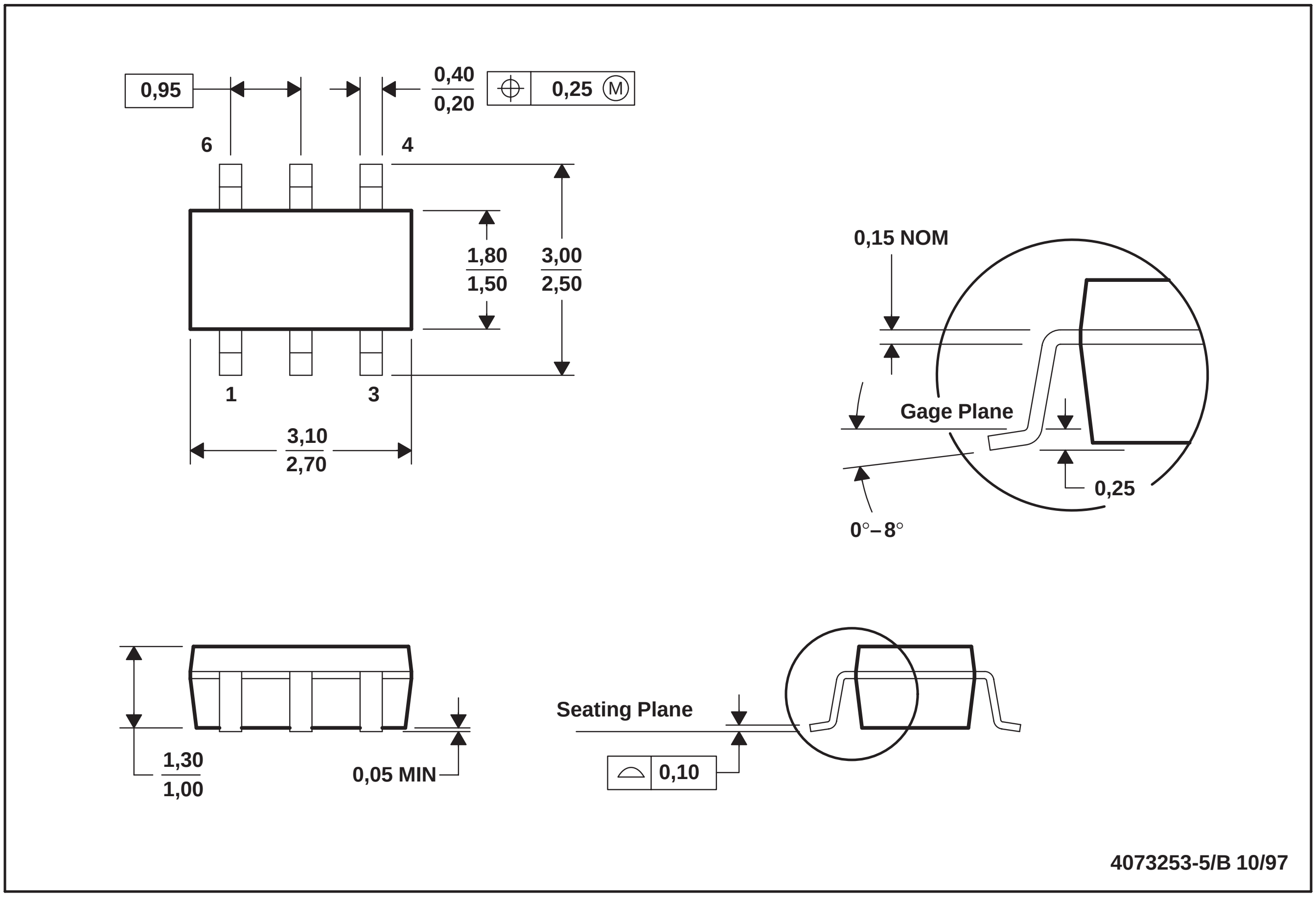
DBV (R-PDSO-G5) **PLASTIC SMALL-OUTLINE PACKAGE**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions include mold flash or protrusion.

MECHANICAL DATA

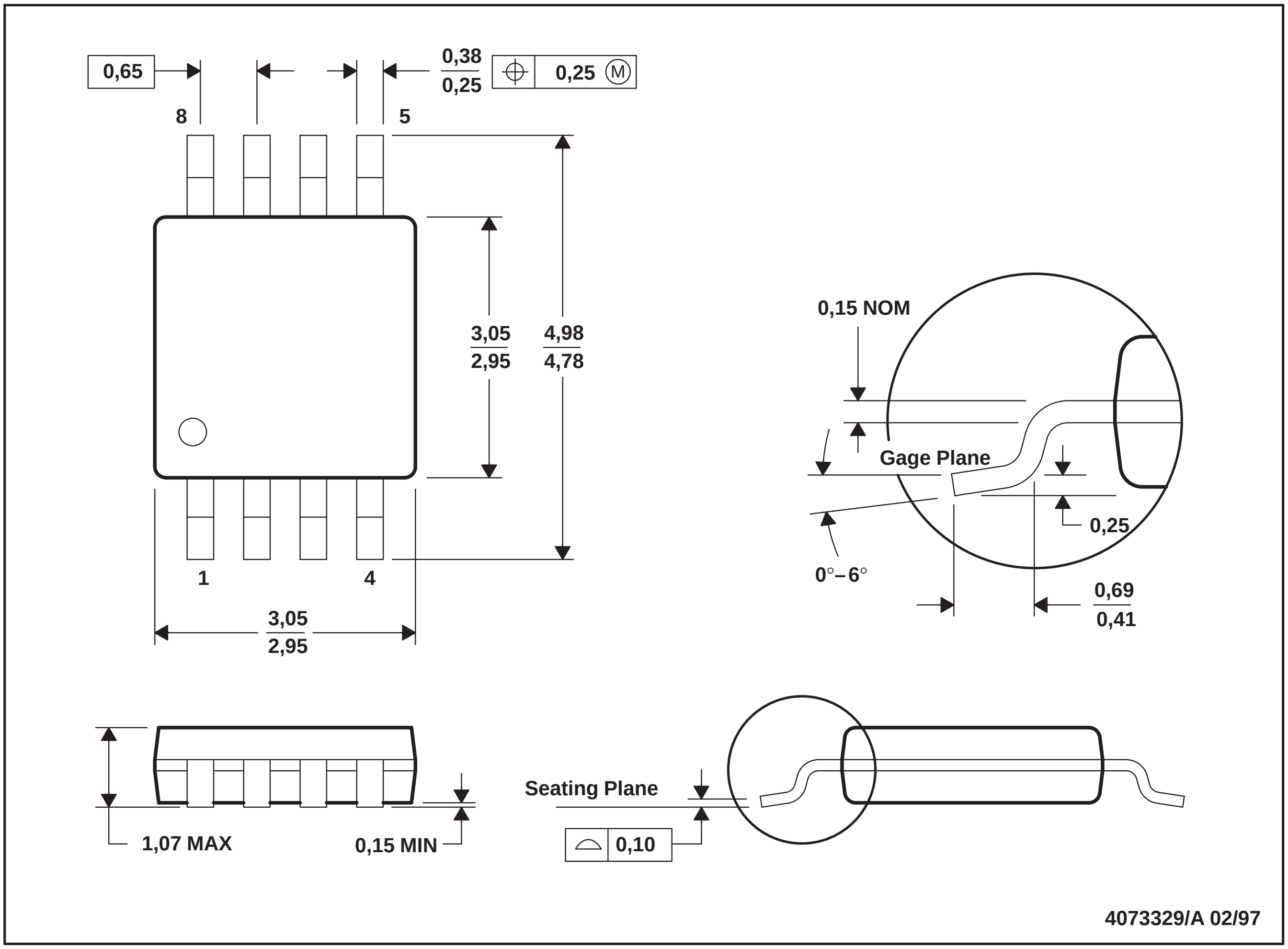
DBV (R-PDSO-G6) **PLASTIC SMALL-OUTLINE PACKAGE**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions include mold flash or protrusion.

MECHANICAL DATA

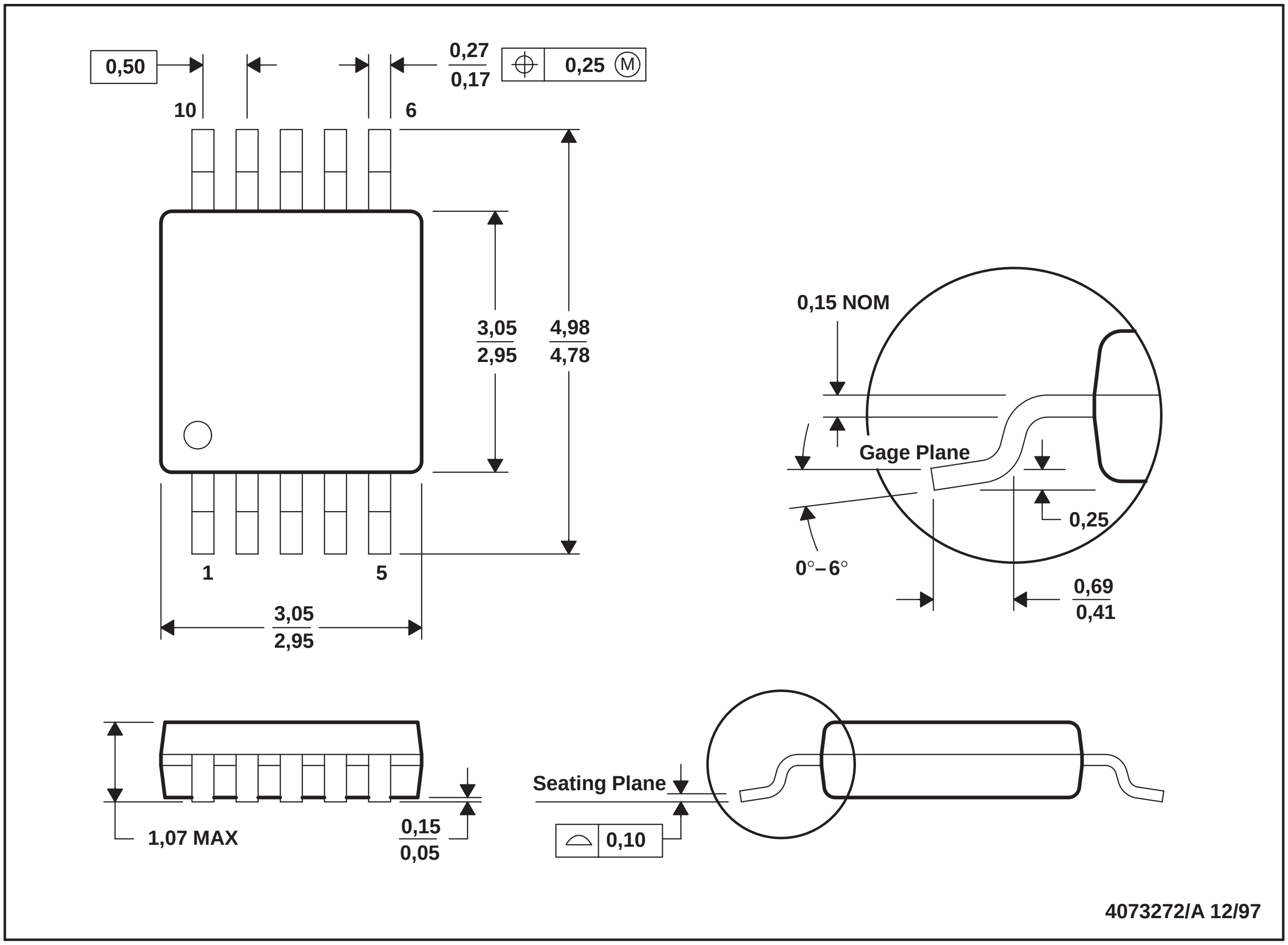
DGK (R-PDSO-G8) **PLASTIC SMALL-OUTLINE PACKAGE**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO-187

MECHANICAL DATA

DGS (S-PDSO-G10) **PLASTIC SMALL-OUTLINE PACKAGE**



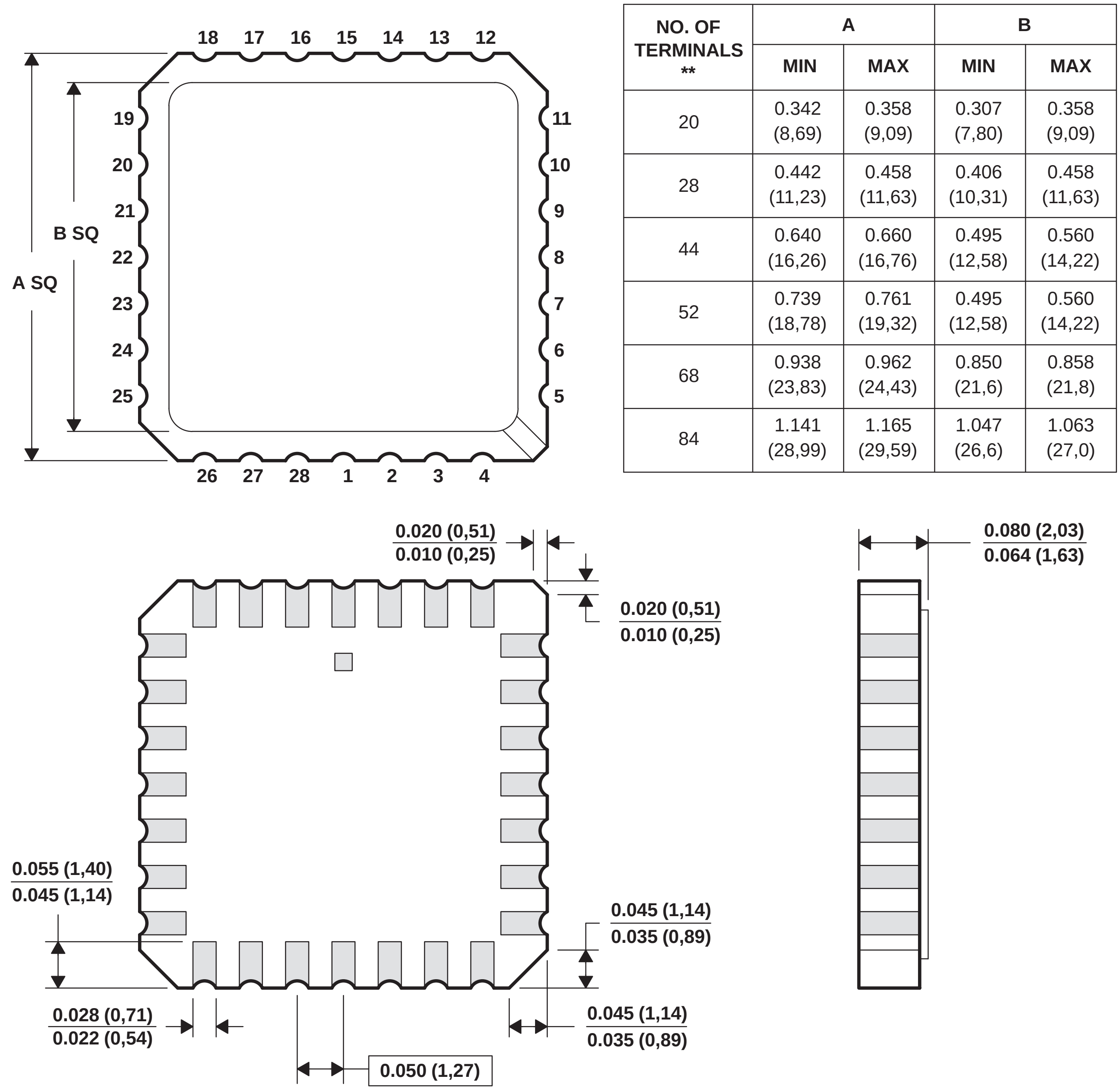
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.

MECHANICAL DATA

FK (S-CQCC-N)** — **LEADLESS CERAMIC CHIP CARRIER**

28 TERMINAL SHOWN

NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.739 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140 / D 10/96

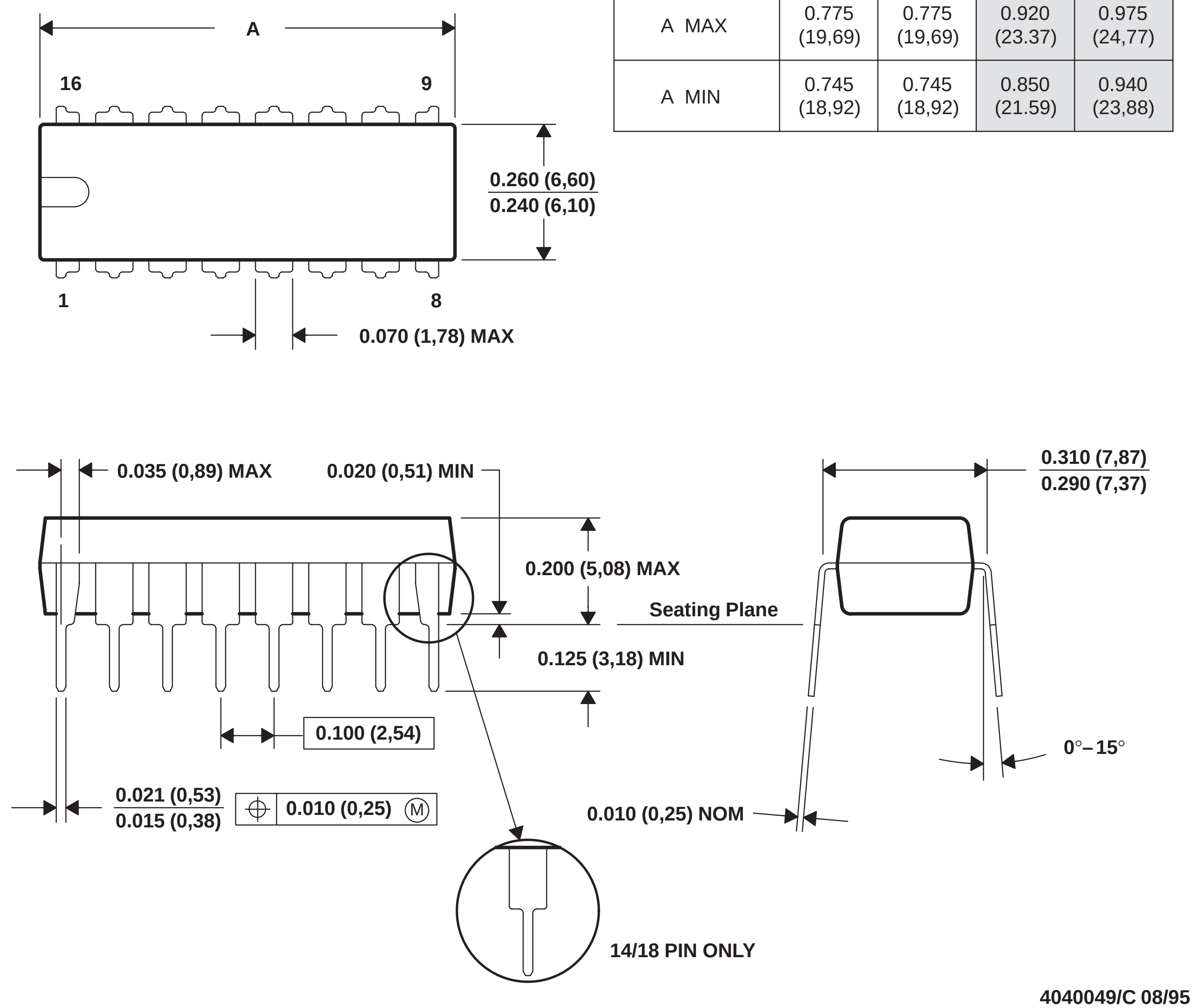
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. The terminals are gold plated.
E. Falls within JEDEC MS-004

MECHANICAL DATA

N (R-PDIP-T)** **PLASTIC DUAL-IN-LINE PACKAGE**

16 PIN SHOWN

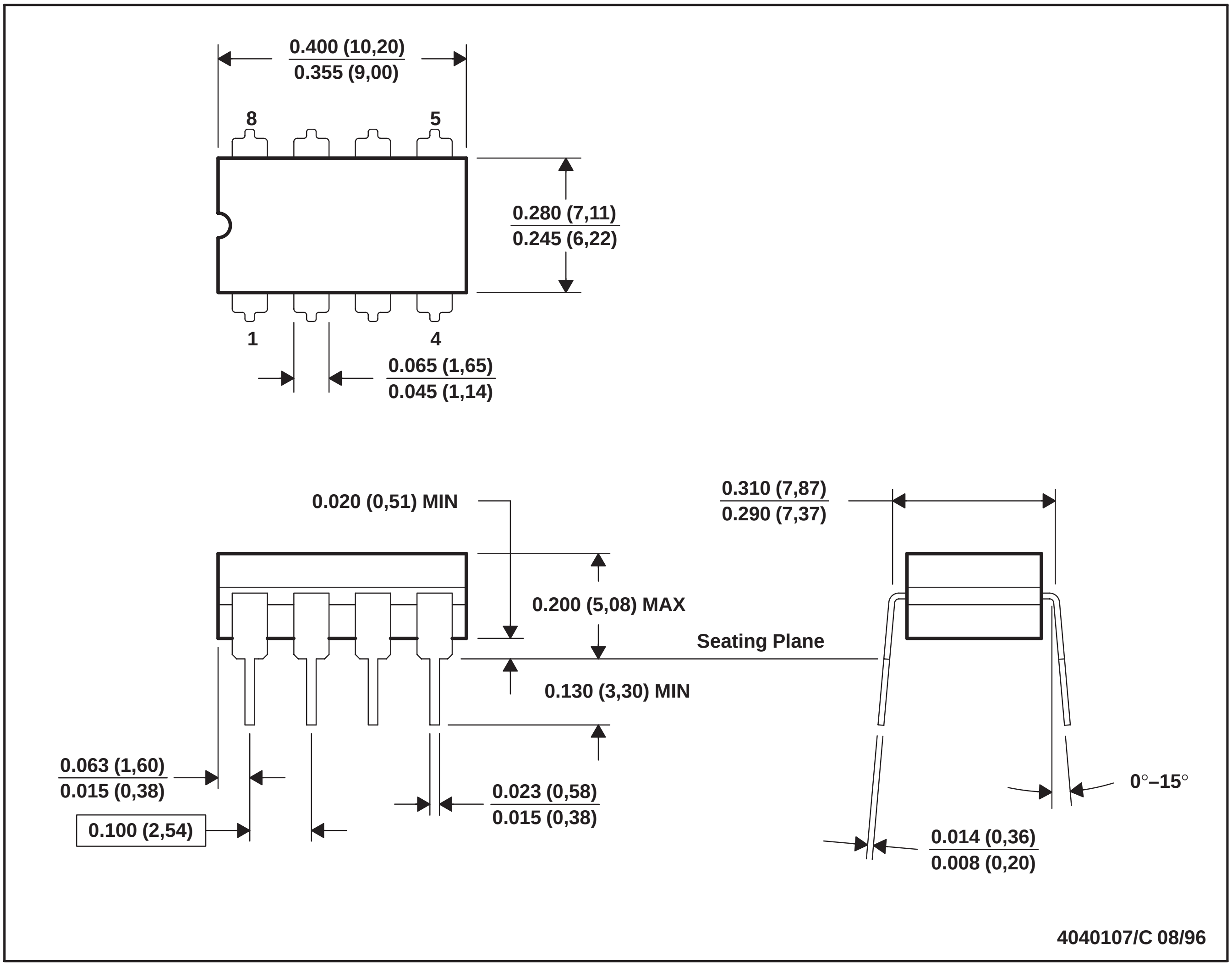
PINS ** / DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23.37)	0.975 (24,77)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21.59)	0.940 (23,88)



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001 (20 pin package is shorter then MS-001.)

MECHANICAL DATA

JG (R-GDIP-T8) **CERAMIC DUAL-IN-LINE PACKAGE**



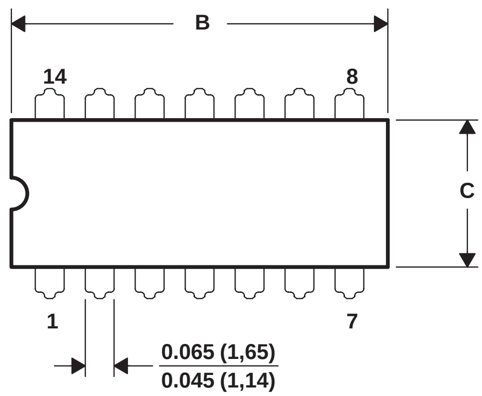
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL-STD-1835 GDIP1-T8

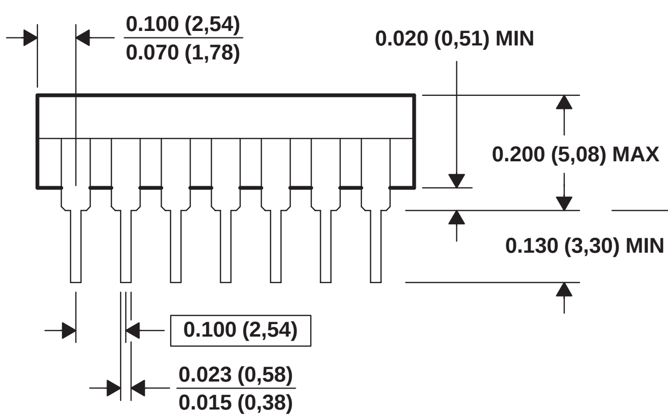
MECHANICAL DATA

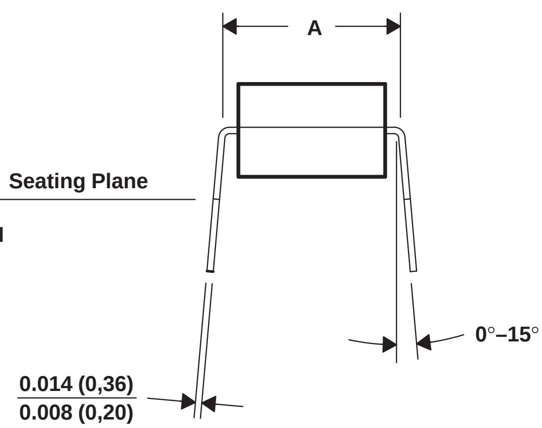
J (R-GDIP-T)** — **CERAMIC DUAL-IN-LINE PACKAGE**

14 PIN SHOWN

DIM \ PINS **	14	16	18	20
A MAX	0.310 (7,87)	0.310 (7,87)	0.310 (7,87)	0.310 (7,87)
A MIN	0.290 (7,37)	0.290 (7,37)	0.290 (7,37)	0.290 (7,37)
B MAX	0.785 (19,94)	0.785 (19,94)	0.910 (23,10)	0.975 (24,77)
B MIN	0.755 (19,18)	0.755 (19,18)	—	0.930 (23,62)
C MAX	0.300 (7,62)	0.300 (7,62)	0.300 (7,62)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.245 (6,22)	0.245 (6,22)





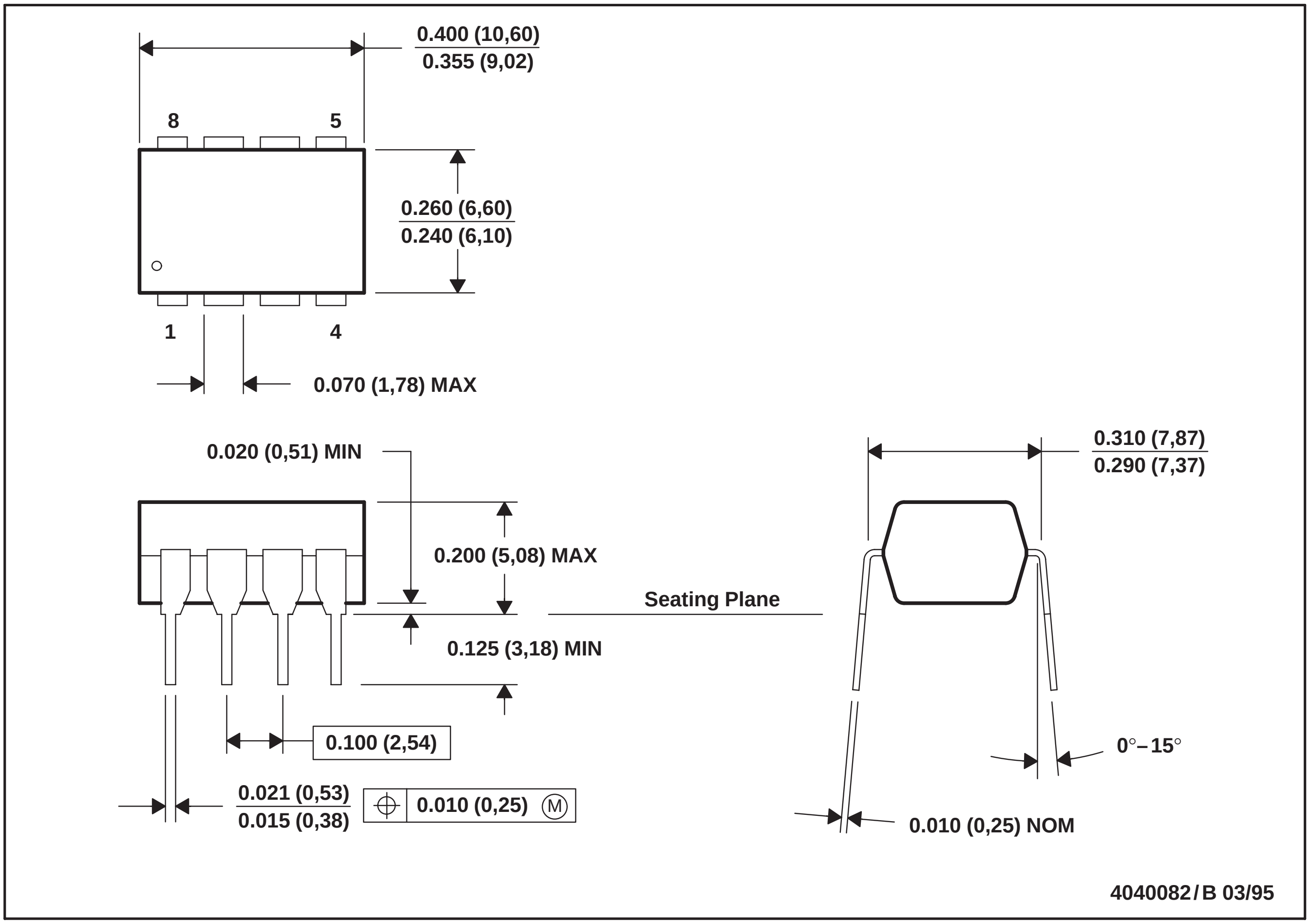


4040083/D 08/98

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18, GDIP1-T20, and GDIP1-T22.

MECHANICAL DATA

P (R-PDIP-T8) **PLASTIC DUAL-IN-LINE PACKAGE**

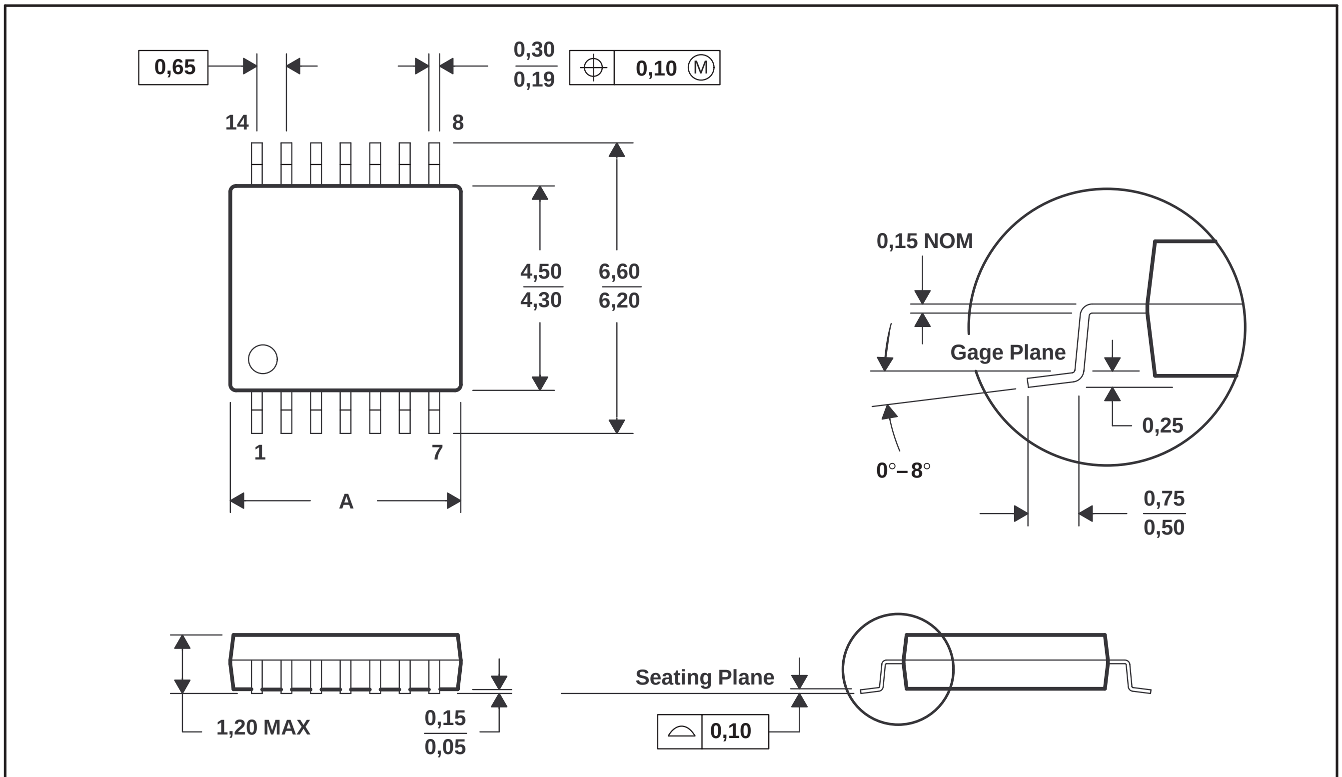


NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001

MECHANICAL DATA

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PIN SHOWN



PINS ** / DIM	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

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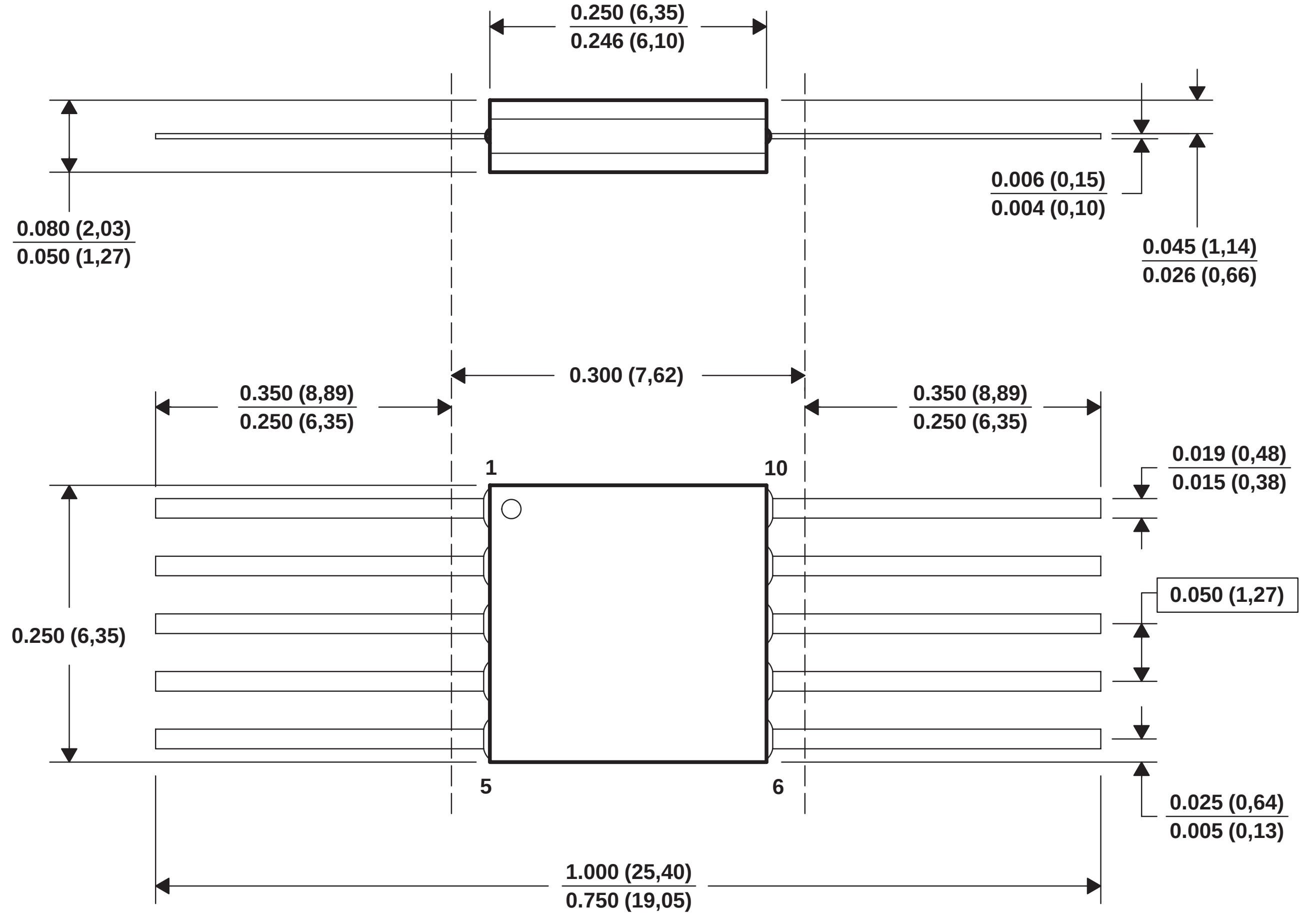
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

MECHANICAL DATA

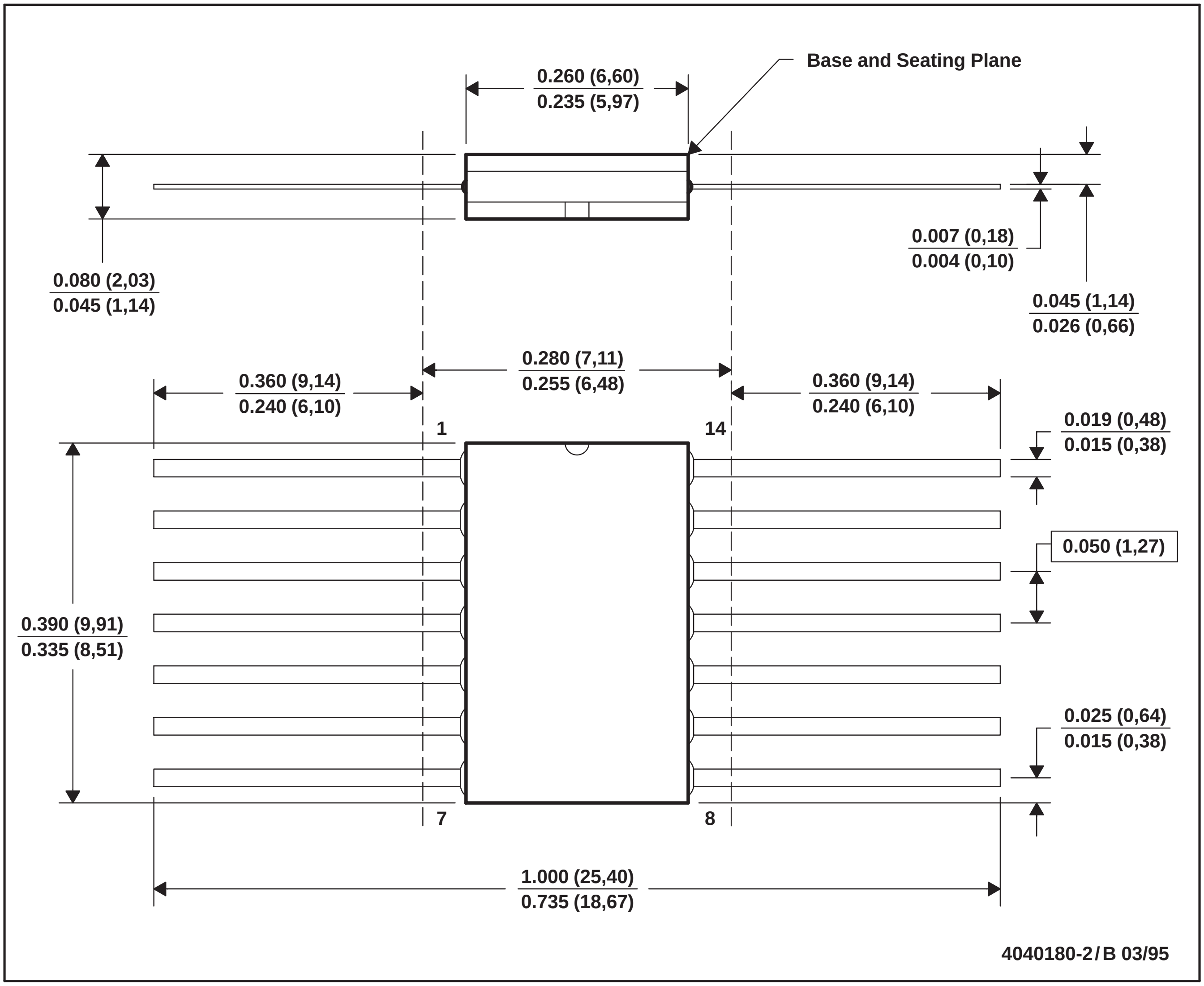
U (S-GDFP-F10) **CERAMIC DUAL FLATPACK**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP1-F10 and JEDEC MO-092AA

MECHANICAL INFORMATION

W (R-GDFP-F14) **CERAMIC DUAL FLATPACK**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP1-F14 and JEDEC MO-092AB

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