HIGH-SPEED, LOW NOISE, FULLY DIFFERENTIAL I/O AMPLIFIERS

SLOS318A – MAY 2000 – REVISED AUGUST 2000

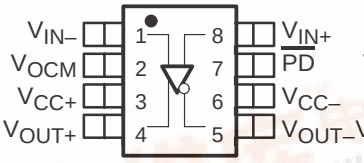
features

- **High Performance**
  - **150 MHz –3 dB Bandwidth (V_{CC} = ±15 V)**
  - **51 V/µs Slew Rate**
  - **–100 dB HD3 at 250 kHz**
- **Low Noise**
  - **1.3 nV/√Hz Input-Referred Noise**
- **Differential-Input/Differential-Output**
  - **Balanced Outputs Reject Common-Mode Noise**
  - **Differential Reduced Second Harmonic Distortion**
- **Wide Power Supply Range**
  - **V_{CC} = 5 V Single Supply to ±15 V**
- **Low-Power Shutdown Option**
  - **I_{CC} = 860 µA in Shutdown Mode (THS4130)**

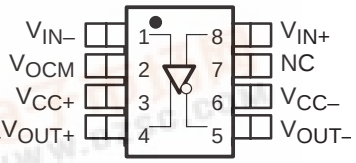
key applications

- **Simple Single-Ended To Differential Conversion**
- **Differential ADC Driver**
- **Differential Transmitter And Receiver**
- **Differential Antialiasing**
- **Output Level Shifter**

THS4130
D OR DGN PACKAGE
(TOP VIEW)



THS4131
D OR DGN PACKAGE
(TOP VIEW)



HIGH-SPEED DIFFERENTIAL I/O FAMILY

DEVICE	NUMBER OF CHANNELS	SHUTDOWN
THS4130	1	X
THS4131	1	–

description

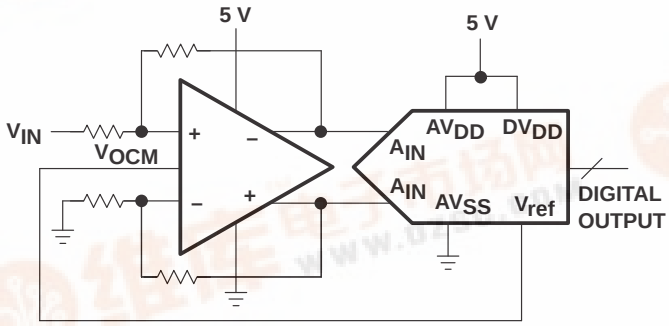
The THS413x is one in a family of fully differential input/differential output devices fabricated using Texas Instruments' state-of-the-art BiCom I complementary bipolar process.

The THS413x consists of a true fully differential signal path from input to output. This results in excellent common-mode noise rejection and improved total harmonic distortion. Not only does the device provide balanced, differential outputs, but internal feedback reduces the effects of parametric differences in gain-setting components between sides.

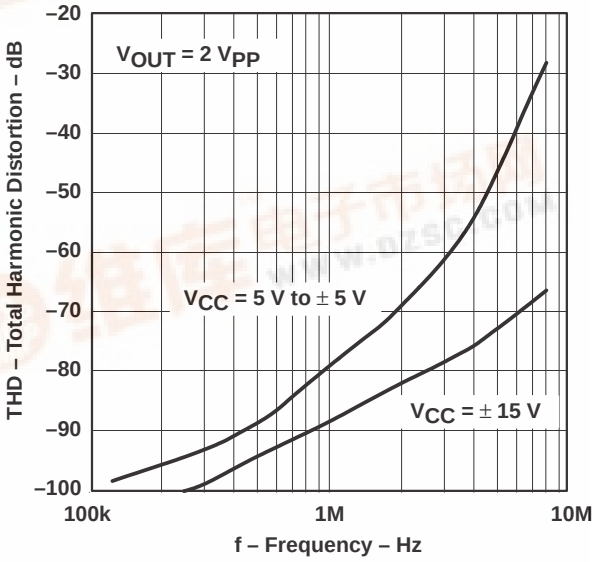
RELATED DEVICES

DEVICE	DESCRIPTION
THS412x	RRO, 3.3 V CMOS
THS414x	160 MHz, 450 V/µs, 6.5 nV/√Hz
THS415x	180 MHz, 850 V/µs, 9 nV/√Hz

typical A/D application circuit



TOTAL HARMONIC DISTORTION
vs
FREQUENCY



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

AVAILABLE OPTIONS

T_A	PACKAGED DEVICES		MSOP CODES	EVALUATION MODULES
	SMALL OUTLINE (D)	MSOP PowerPAD™ (DGN)		
0°C to 70°C	THS4130CD THS4131CD	THS4130CDGN THS4131CDGN	AOB AOD	THS4130/1EVM
–40°C to 85°C	THS4130ID THS4131ID	THS4130IDGN THS4131IDGN	AOC AOE	– –

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC}– to V_{CC}+ . . . . . ±33 V
Input voltage, V_I . . . . . ±V_{CC}
Output current, I_O (see Note 1) . . . . . 150 mA
Differential input voltage, V_{ID} . . . . . ±6 V
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature, T_A: C suffix . . . . . 0°C to 70°C
I suffix . . . . . –40°C to 85°C
Storage temperature, T_{stg} . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 Inch) from case for 10 seconds . . . . . 300°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The THS413x may incorporate a PowerPad™ on the underside of the chip. This acts as a heatsink and must be connected to a thermally dissipative plane for proper power dissipation. Failure to do so may result in exceeding the maximum junction temperature which could permanently damage the device. See TI technical brief SLMA002 and SLMA004 for more information about utilizing the PowerPad™ thermally enhanced package.

DISSIPATION RATING TABLE

PACKAGE	θ_{JA} (°C/W)	θ_{JC} (°C/W)	T_A = 25°C POWER RATING
D	167‡	38.3	740 mW
DGN§	58.4	4.7	2.14 W

‡ This data was taken using the JEDEC standard Low-K test PCB. For the JEDEC Proposed High-K test PCB, the θ_{JA} is 95°C/W with a power rating at T_A = 25°C of 1.32 W.

§ This data was taken using 2 oz. trace and copper pad that is soldered directly to a 3 in. × 3 in. PC.

recommended operating conditions

		MIN	TYP	MAX	UNIT
Supply voltage, V_{CC}+ to V_{CC}–	Dual supply	±2.5		±15	V
	Single supply	5		30	
Operating free-air temperature, T_A	C suffix	0		70	°C
	I suffix	–40		85	

PowerPAD is a trademark of Texas Instruments.

electrical characteristics, V_{CC} = ±5 V, R_L = 800 Ω, T_A = 25°C (unless otherwise noted)†

dynamic performance

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
BW	Small signal bandwidth (–3 dB) Single ended input, differential output V_I = 63 mV_{PP}	V_{CC} = 5	Gain = 1, R_f = 390 Ω		125		MHz
		V_{CC} = ±5	Gain = 1, R_f = 390 Ω		135		
		V_{CC} = ±15	Gain = 1, R_f = 390 Ω		150		
	Small signal bandwidth (–3 dB) Single ended input, differential output V_I = 63 mV_{PP}	V_{CC} = 5	Gain = 2, R_f = 750 Ω		80		
		V_{CC} = ±5	Gain = 2, R_f = 750 Ω		85		
		V_{CC} = ±15	Gain = 2, R_f = 750 Ω		90		
SR	Slew rate (see Note 2)	Gain = 1			52		V/µs
t_S	Settling time to 0.1%	Step voltage = 2 V,	Gain = 1		78		ns
	Settling time to 0.01%				213		ns

NOTE 2: Slew rate is measured from an output level range of 25% to 75%.
† The full range temperature is 0°C to 70°C for the C suffix, and –40°C to 85°C for the I suffix.

distortion performance

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
THD	Total harmonic distortion Differential input, differential output Gain = 1, R_f = 390 Ω, R_L = 800 Ω V_O = 2 V_{PP}	V_{CC} = 5	f= 250 kHz		–95		dBc
			f= 1 MHz		–81		
		V_{CC} = ±5	f= 250 kHz		–96		
			f= 1 MHz		–80		
		V_{CC} = ±15	f= 250 kHz		–97		
			f= 1 MHz		–80		
	V_O = 4 V_{PP}	V_{CC} = ±5	f= 250 kHz		–91		
			f= 1 MHz		–75		
		V_{CC} = ±15	f= 250 kHz		–91		
			f= 1 MHz		–75		
Spurious free dynamic range (SFDR) Differential input, differential output Gain = 1, R_f = 390 Ω, R_L = 800 Ω f= 250 kHz		V_O = 2 V_{pp}	V_{CC} = ±2.5		97		dB
			V_{CC} = ±5		98		
			V_{CC} = ±15		99		
		V_O = 4 V_{pp}	V_{CC} = ±5		93		
			V_{CC} = ±15		95		
Third intermodulation distortion		$V_{I(PP)}$ = 4 V, F2 = 3.5 MHz	G = 1, F1 = 3 MHz,		–53		dBc
Third order intercept		$V_{I(PP)}$ = 4 V, F2 = 3.5 MHz	G = 1, F1 = 3 MHz,		41.5		dB

† The full range temperature is 0°C to 70°C for the C suffix, and –40°C to 85°C for the I suffix.

electrical characteristics, V_{CC} = ±5 V, R_L = 800 Ω, T_A = 25°C (unless otherwise noted) (continued)†

noise performance

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_n	Input voltage noise	f = 10 kHz		1.3		nV/√Hz
I_n	Input current noise	f = 10 kHz		0.4		pA/√Hz

† The full range temperature is 0°C to 70°C for the C suffix, and –40°C to 85°C for the I suffix.

dc performance

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Open loop gain		T_A = 25°C	71	78		dB
		T_A = full range	69			
$V_{(OS)}$	Input offset voltage	T_A = 25°C		0.2	2	mV
		T_A = full range			3	
	Common mode input offset voltage, referred to V_{OCM}	T_A = 25°C		0.2	3.5	
	Input offset voltage drift	T_A = full range		4.5		µV/°C
I_{IB}	Input bias current	T_A = full range		2	6	µA
I_{OS}	Input offset current	T_A = full range		100	500	nA
	Offset drift			2		nA/°C

† The full range temperature is 0°C to 70°C for the C suffix, and –40°C to 85°C for the I suffix.

input characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CMRR	Common-mode rejection ratio	T_A = full range	80	95		dB
V_{ICR}	Common-mode input voltage range		–3.77 to 4.3	–4 to 4.5		V
R_I	Input resistance	Measured into each input terminal		34		MΩ
C_I	Input capacitance, closed loop			4		pF
r_o	Output resistance	Open loop		41		Ω

† The full range temperature is 0°C to 70°C for the C suffix, and –40°C to 85°C for the I suffix.

output characteristics

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Output voltage swing	V_{CC} = 5 V	T_A = 25°C	1.2 to 3.8	0.9 to 4.1		V
		T_A = full range	1.3 to 3.7			
	V_{CC} = ±5 V	T_A = 25°C	3.7	4		
		T_A = full range	3.6			
	V_{CC} = ±15 V	T_A = 25°C	10.5	12.4		
		T_A = full range	10.2			
I_O Output current	V_{CC} = 5 V, R_L = 7 Ω	T_A = 25°C	25	45		mA
		T_A = full range	20			
	V_{CC} = ±5 V, R_L = 7 Ω	T_A = 25°C	30	55		
		T_A = full range	28			
	V_{CC} = ±15 V, R_L = 7 Ω	T_A = 25°C	60	85		
		T_A = full range	50			

† The full range temperature is 0°C to 70°C for the C suffix, and –40°C to 85°C for the I suffix.

electrical characteristics, V_{CC} = ±5 V, R_L = 800 Ω, T_A = 25°C (unless otherwise noted) (continued)†

power supply

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage range	Single supply		4		33	V
		Split supply		±2		±16.5	
I_{CC}	Quiescent current	V_{CC} = ±5 V	T_A = 25°C		12.3	15	mA
			T_A = full range			16	
		V_{CC} = ±15 V	T_A = 25°C		14		
$I_{CC(SD)}$	Quiescent current (shutdown) (THS4130 only)	V_{PD} = –5 V	T_A = 25°C		0.86	1.4	mA
			T_A = full range			1.5	
PSRR	Power supply rejection ratio		T_A = 25°C	73	98		dB
			T_A = full range	70			

† The full range temperature is 0°C to 70°C for the C suffix, and –40°C to 85°C for the I suffix.

TYPICAL CHARACTERISTICS

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	Small signal frequency response		1
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	Small signal frequency response (various C_F)		4
	Small signal frequency response (various C_L)		5
	Large signal transient response (differential in/single out)		6
	Small signal frequency response		7
CMMR	Common mode rejection ratio	vs Frequency	8
I_{CC}	Supply current	vs Free-air temperature	9
		vs Free-air temperature (shutdown state)	10
I_{IB}	Input bias current	vs Free-air temperature	11
	Settling time		12
PSRR	Power supply rejection ratio	vs Frequency (differential out)	13
	Large signal transient response		14
THD	Total harmonic distortion	vs Frequency	15
	Second harmonic distortion	vs Frequency	16, 17
		vs Output voltage	18, 19
	Third harmonic distortion	vs Frequency	20, 21
		vs Output voltage	22, 23
V_n	Voltage noise	vs Frequency	24
I_n	Current noise	vs Frequency	25
$V_{(OS)}$	Input offset voltage	vs Common-mode output voltage	26
V_O	Output voltage	vs Differential load resistance	27
z_o	Output impedance	vs Frequency	28

TYPICAL CHARACTERISTICS

SMALL SIGNAL FREQUENCY RESPONSE

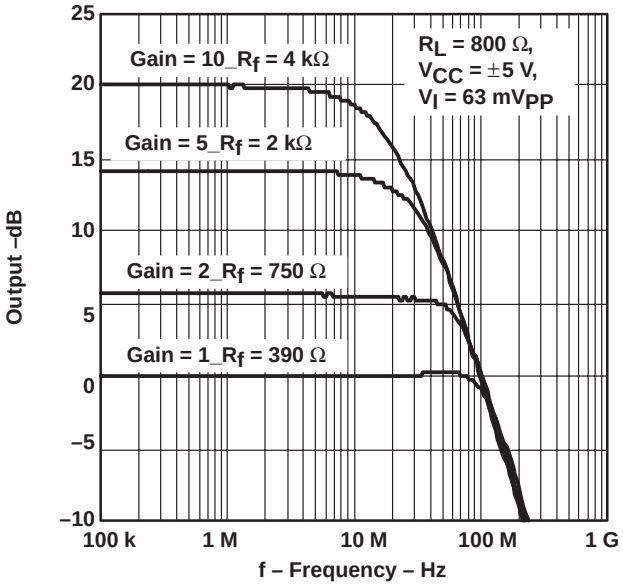


Figure 1

SMALL SIGNAL FREQUENCY RESPONSE

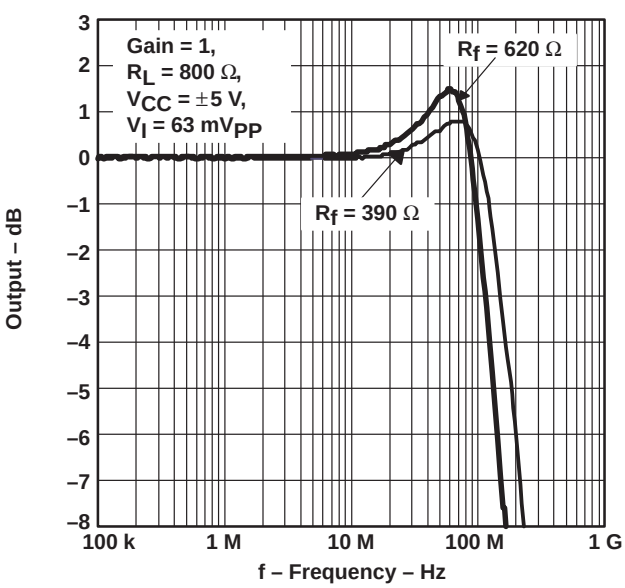


Figure 2

SMALL SIGNAL FREQUENCY RESPONSE
(VARIOUS SUPPLY)

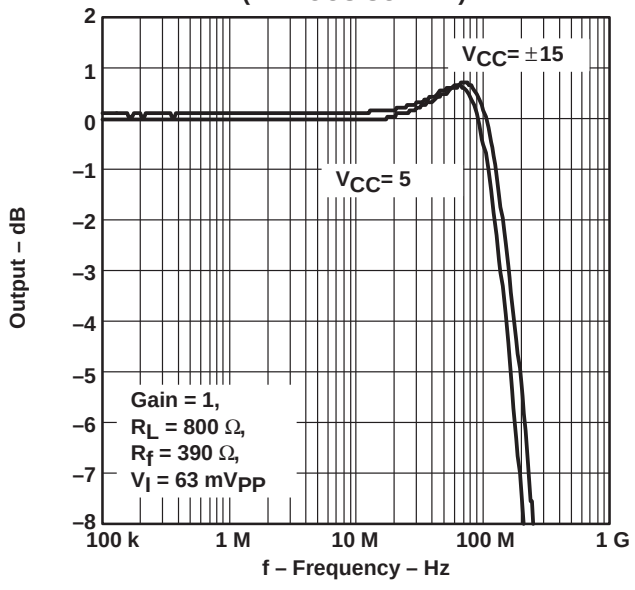


Figure 3

SMALL SIGNAL FREQUENCY RESPONSE
(VARIOUS C_F)

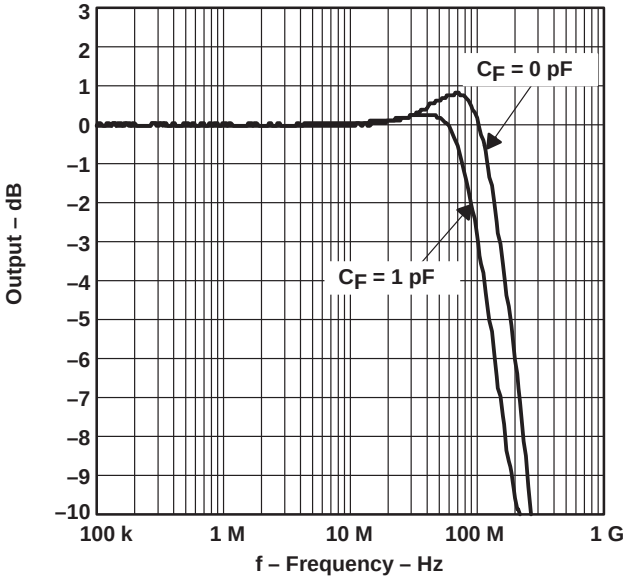


Figure 4

TYPICAL CHARACTERISTICS

SMALL SIGNAL FREQUENCY RESPONSE
(VARIOUS C_L)

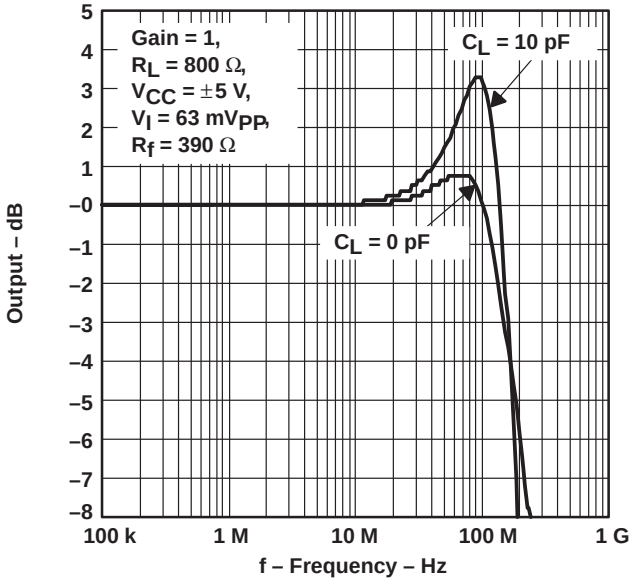


Figure 5

LARGE SIGNAL TRANSIENT RESPONSE
(DIFFERENTIAL IN/SINGLE OUT)

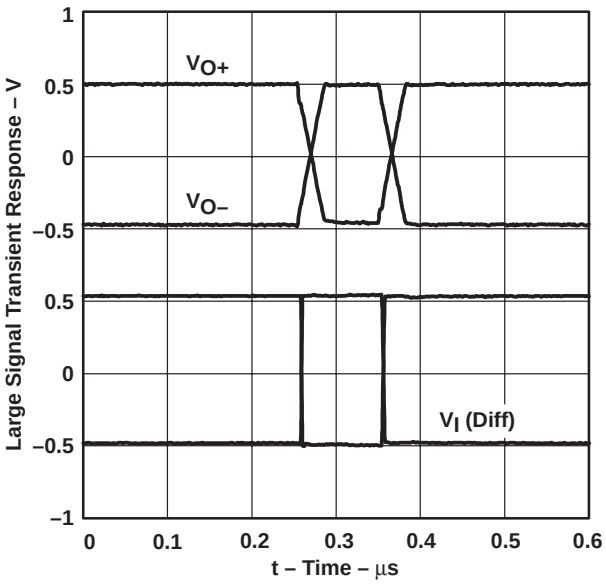


Figure 6

SMALL SIGNAL FREQUENCY RESPONSE

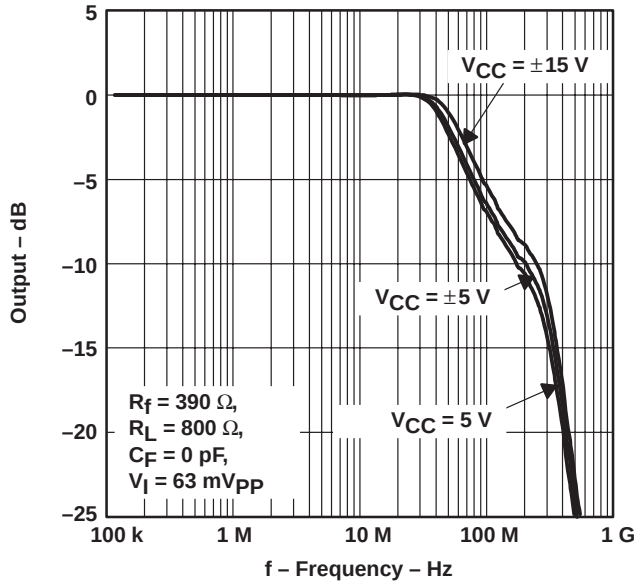


Figure 7

COMMON MODE REJECTION RATIO
vs
FREQUENCY

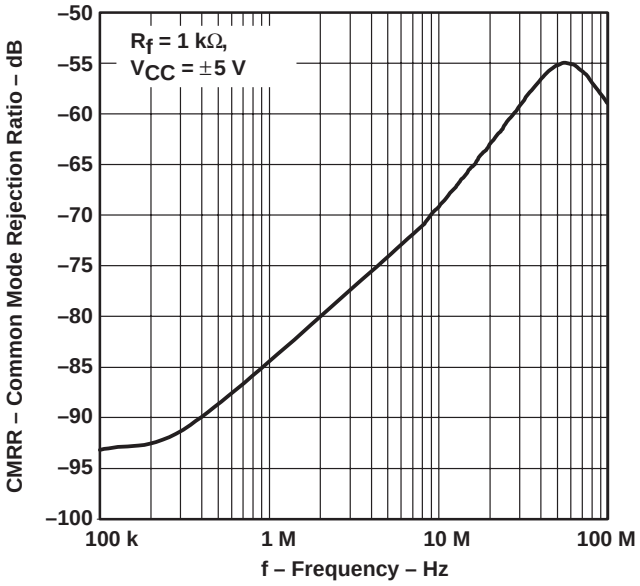


Figure 8

TYPICAL CHARACTERISTICS

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

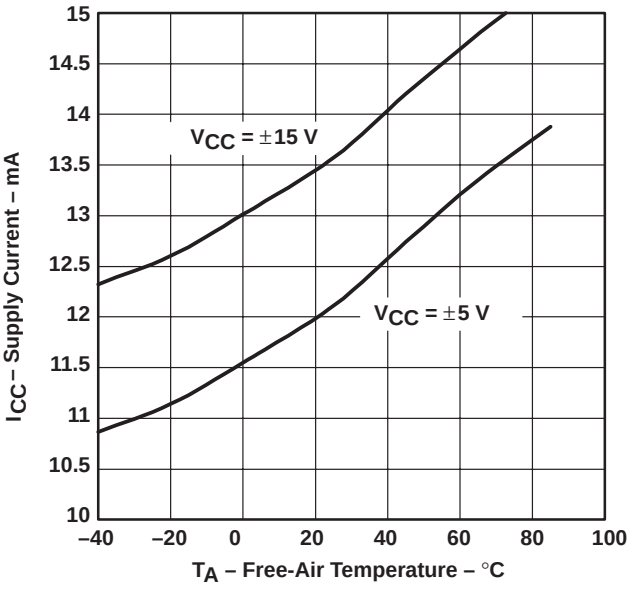


Figure 9

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE
(SHUTDOWN STATE)

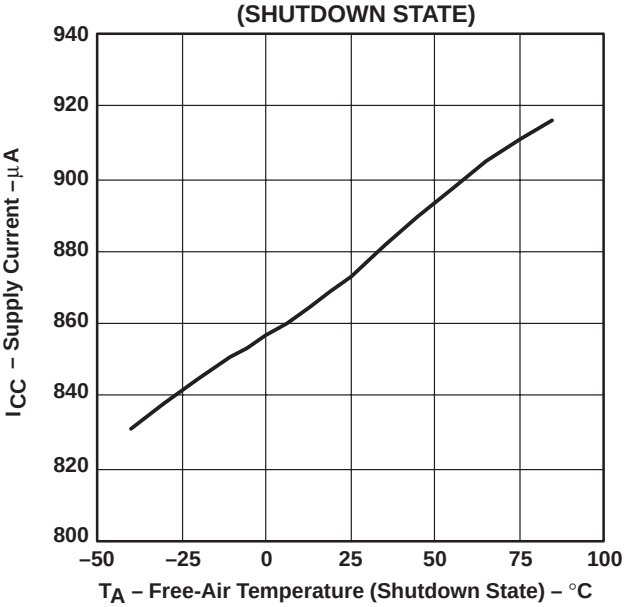


Figure 10

INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE

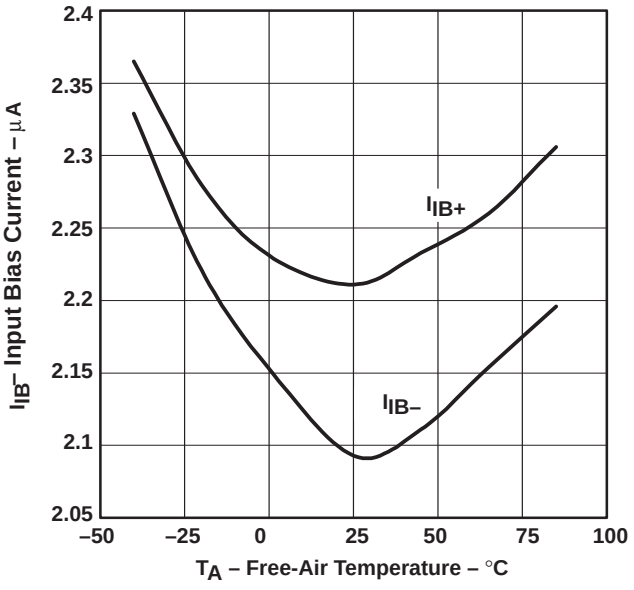


Figure 11

SETTLING TIME

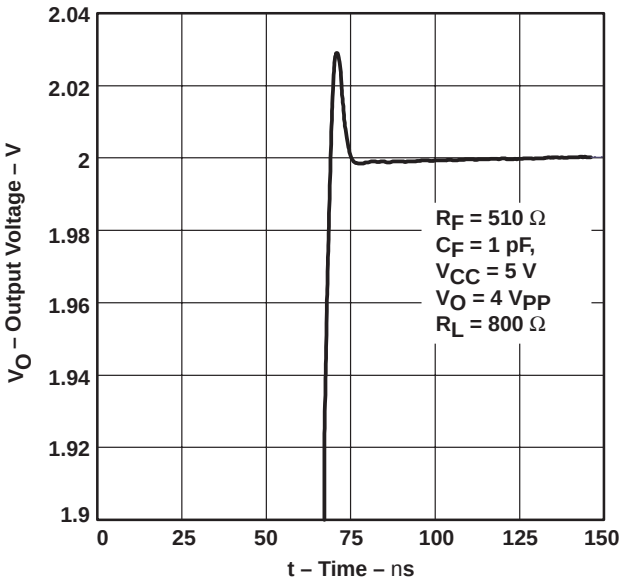


Figure 12

TYPICAL CHARACTERISTICS

POWER SUPPLY REJECTION RATIO vs FREQUENCY (DIFFERENTIAL OUT)

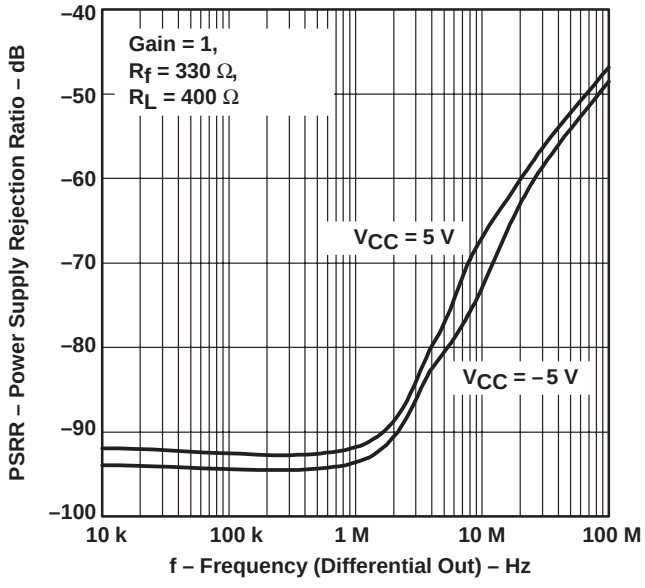


Figure 13

LARGE SIGNAL TRANSIENT RESPONSE

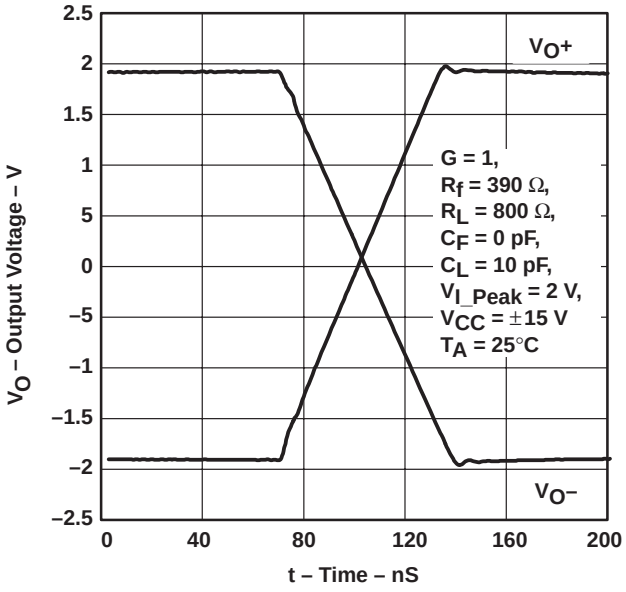


Figure 14

TOTAL HARMONIC DISTORTION vs FREQUENCY

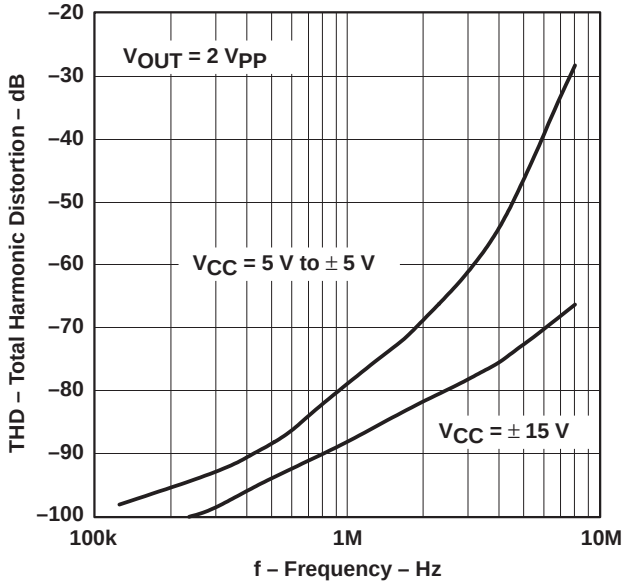


Figure 15

TYPICAL CHARACTERISTICS

SECOND HARMONIC DISTORTION vs FREQUENCY

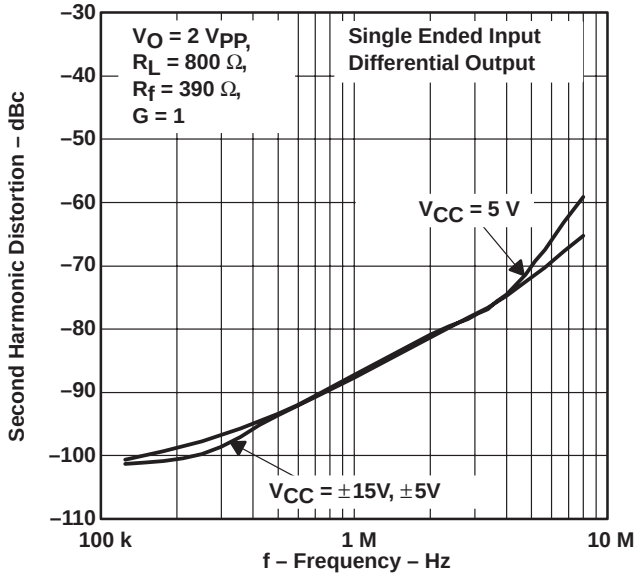


Figure 16

SECOND HARMONIC DISTORTION vs FREQUENCY

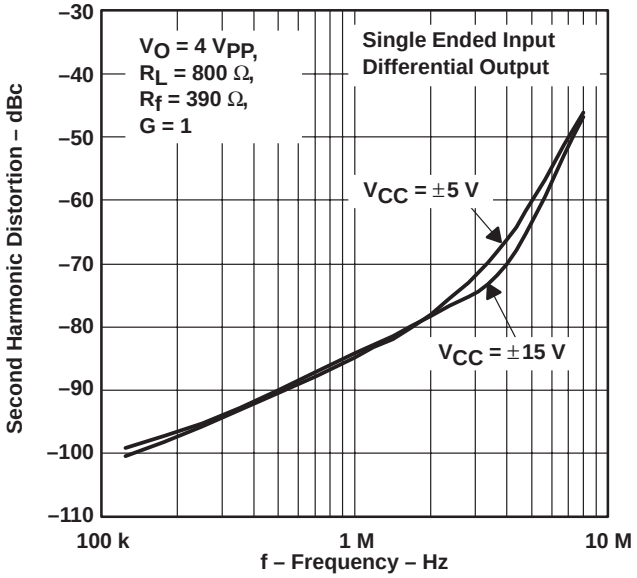


Figure 17

SECOND HARMONIC DISTORTION vs OUTPUT VOLTAGE

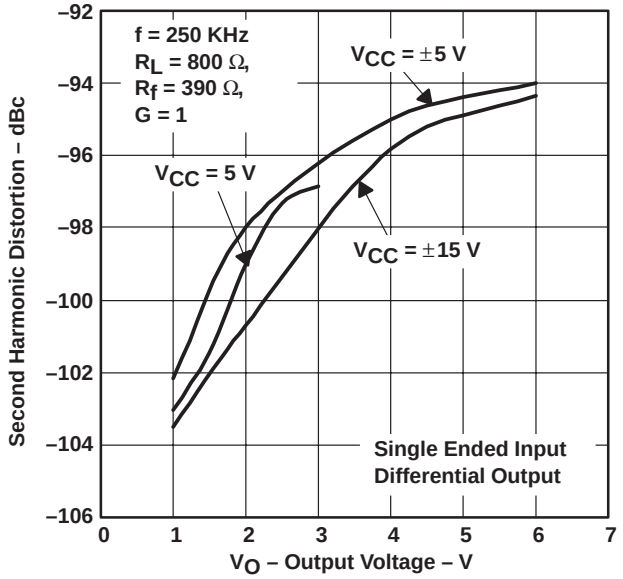


Figure 18

SECOND HARMONIC DISTORTION vs OUTPUT VOLTAGE

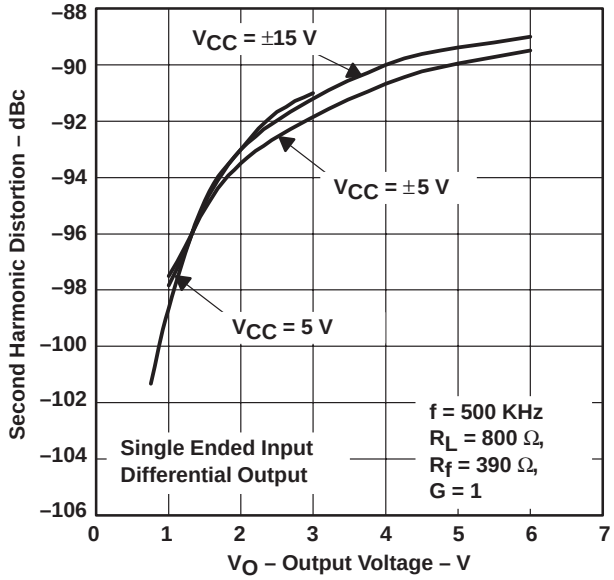


Figure 19

TYPICAL CHARACTERISTICS

THIRD HARMONIC DISTORTION
vs
FREQUENCY

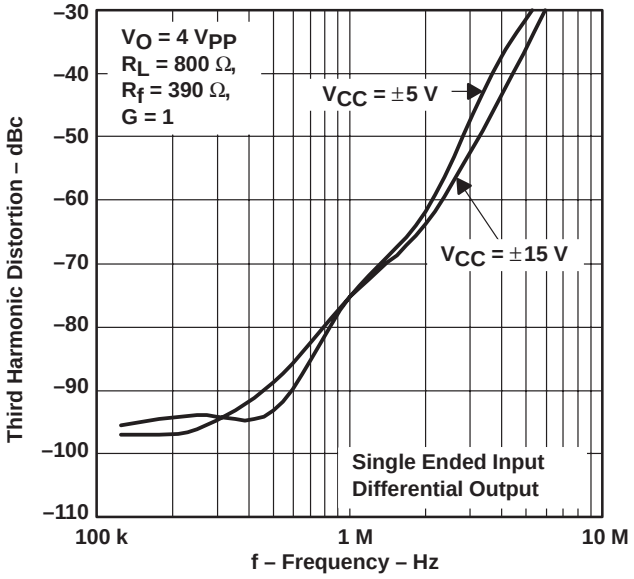


Figure 20

THIRD HARMONIC DISTORTION
vs
FREQUENCY

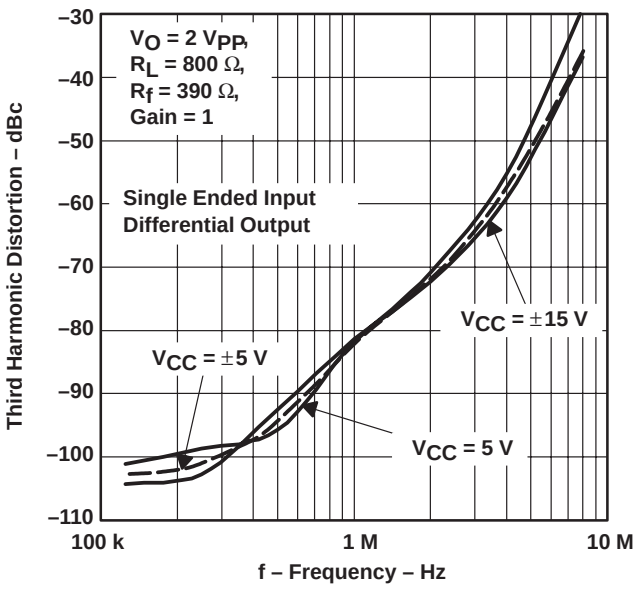


Figure 21

THIRD HARMONIC DISTORTION
vs
OUTPUT VOLTAGE

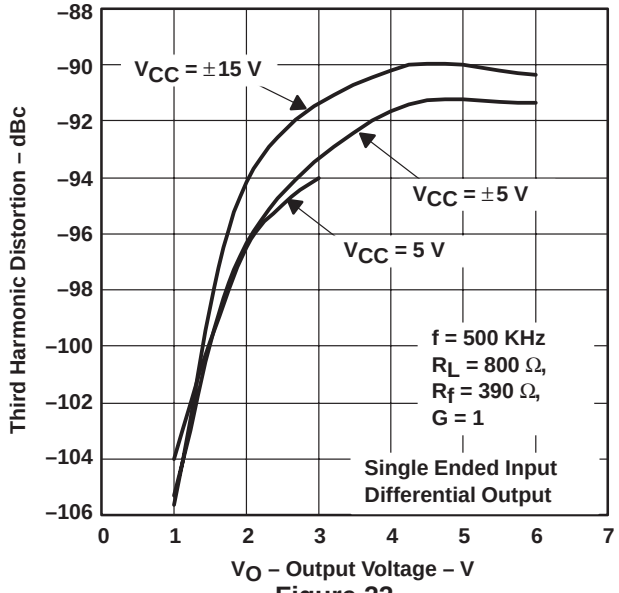


Figure 22

THIRD HARMONIC DISTORTION
vs
OUTPUT VOLTAGE

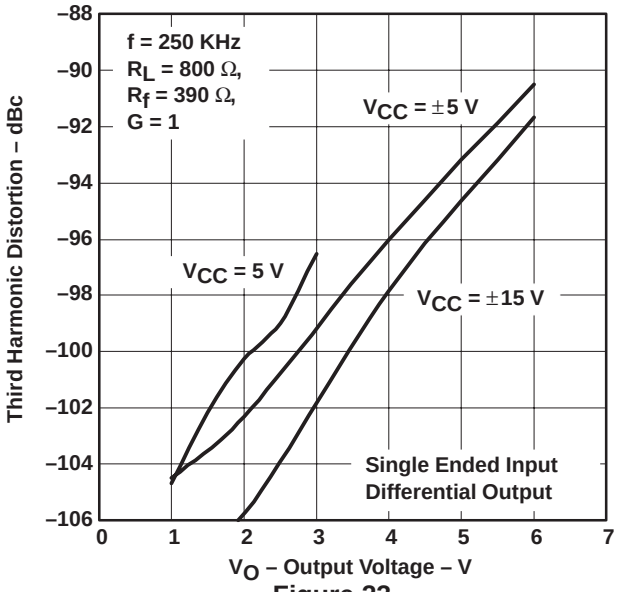


Figure 23

TYPICAL CHARACTERISTICS

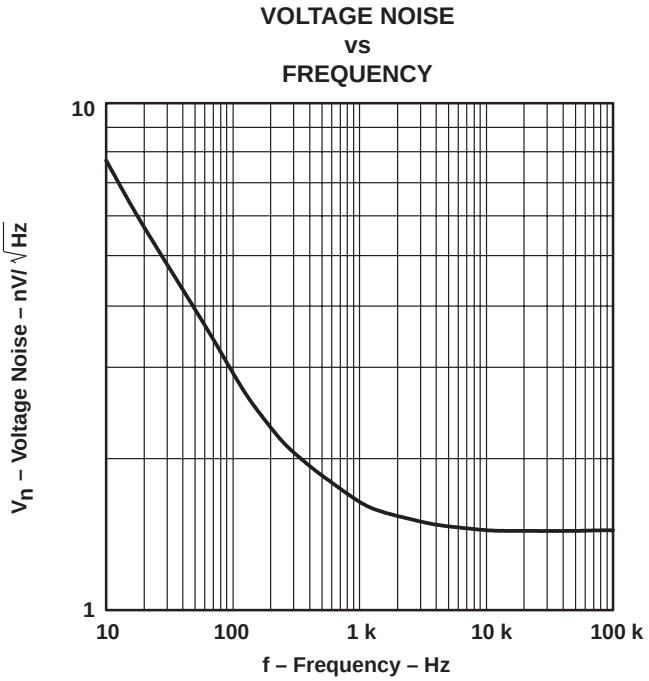


Figure 24

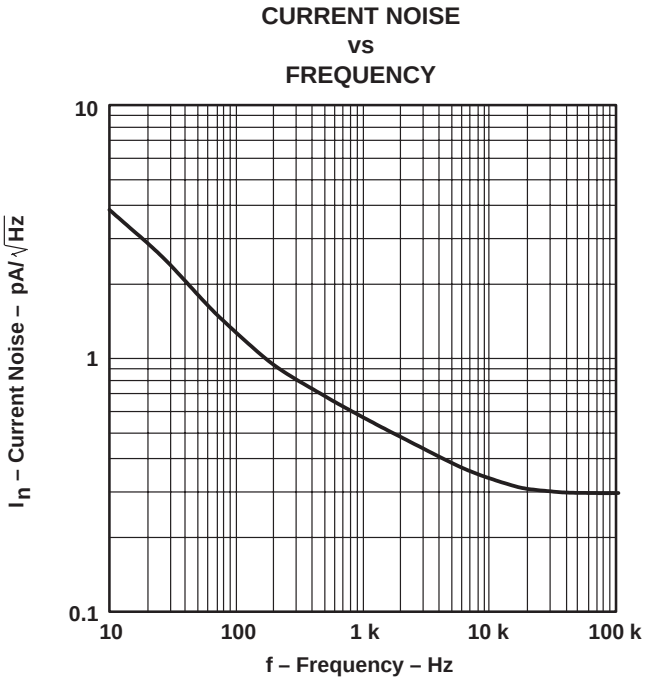


Figure 25

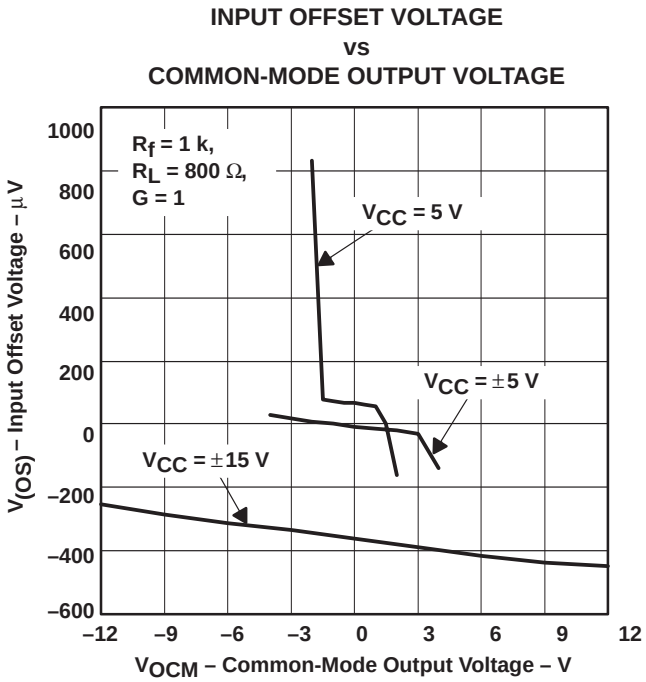


Figure 26

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE vs DIFFERENTIAL LOAD RESISTANCE

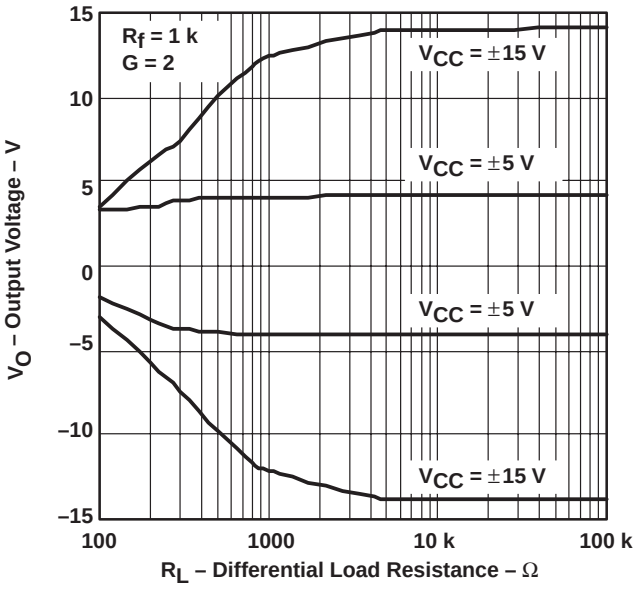


Figure 27

OUTPUT IMPEDANCE vs FREQUENCY

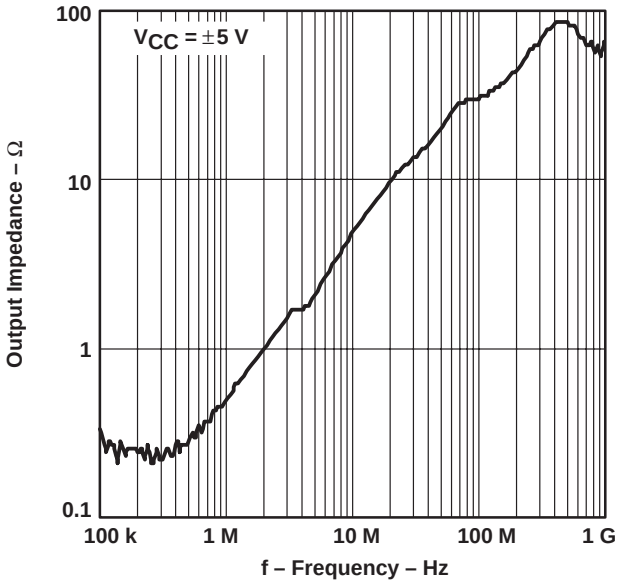


Figure 28

APPLICATION INFORMATION

resistor matching

Resistor matching is important in fully differential amplifiers. The balance of the output on the reference voltage depends on matched ratios of the resistor. CMRR, PSRR, and cancellation of the second harmonic distortion will diminish if resistor mismatch occurs. Therefore, it is recommended to use 0.1% tolerance resistors or better to keep the performance optimized.

V_{OCM} sets the dc level of the output signals. If no voltage is applied to the V_{OCM} pin, it will be set to the midrail voltage internally defined as:

$$\frac{\left(V_{CC+}\right) + \left(V_{CC-}\right)}{2}$$

In the differential mode, the V_{OCM} on the two outputs cancel each other. Therefore, the output in the differential mode is the same as the input in the gain of 1. V_{OCM} has a high bandwidth capability up to the typical operation range of the amplifier. For the prevention of noise going through the device, use a 0.1 μf capacitor on the V_{OCM} pin as a bypass capacitor. The following graph shows the simplified diagram of the THS413x.

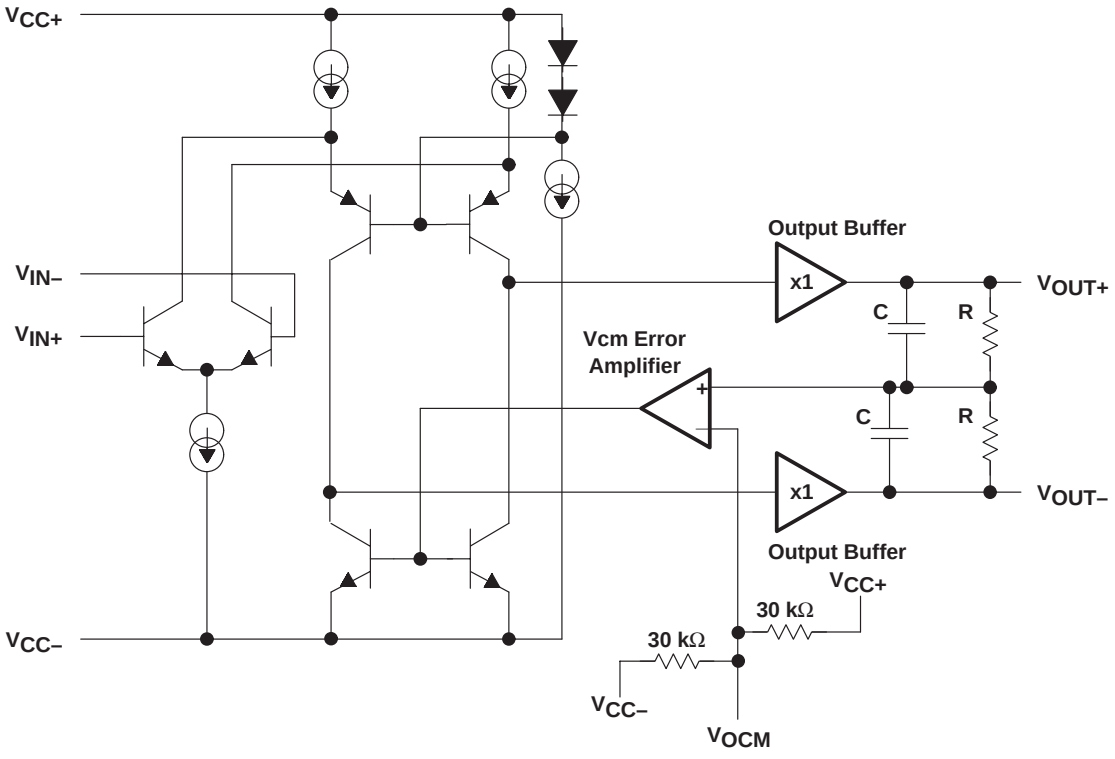


Figure 29. THS413x Simplified Diagram

APPLICATION INFORMATION

data converters

Data converters are one of the most popular applications for the fully differential amplifiers. The following schematic shows a typical configuration of a fully differential amplifier attached to a differential ADC.

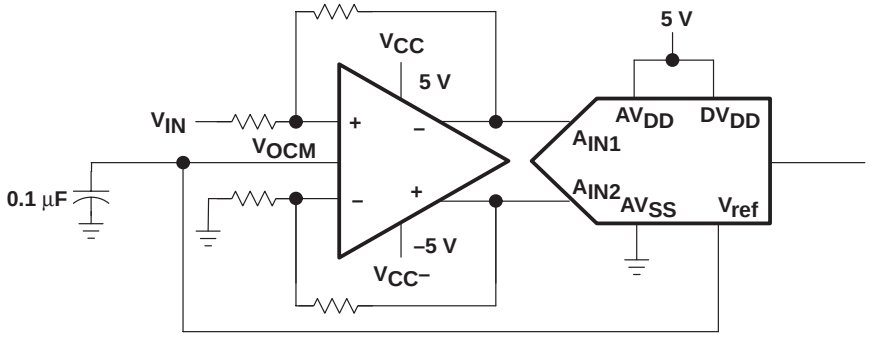


Figure 30. Fully Differential Amplifier Attached to a Differential ADC

Fully differential amplifiers can operate with a single supply. V_{OCM} defaults to the midrail voltage, $V_{CC}/2$. The differential output may be fed into a data converter. This method eliminates the use of a transformer in the circuit. If the ADC has a reference voltage output (V_{ref}), then it is recommended to connect it directly to the V_{OCM} of the amplifier using a bypass capacitor for stability.

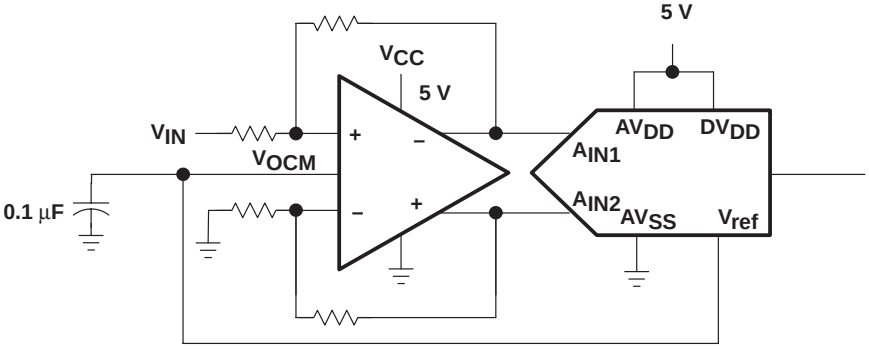


Figure 31. Differential Amplifier Using a Single Supply

APPLICATION INFORMATION

driving a capacitive load

Driving capacitive loads with high performance amplifiers is not a problem as long as certain precautions are taken. The first is to realize that the THS413x has been internally compensated to maximize its bandwidth and slew rate performance. When the amplifier is compensated in this manner, capacitive loading directly on the output will decrease the device's phase margin leading to high frequency ringing or oscillations. Therefore, for capacitive loads of greater than 10 pF, it is recommended that a resistor be placed in series with the output of the amplifier, as shown in Figure 32. A minimum value of 20 Ω should work well for most applications. For example, in 50-Ω transmission systems, setting the series resistor value to 50 Ω both isolates any capacitance loading and provides the proper line impedance matching at the source end.

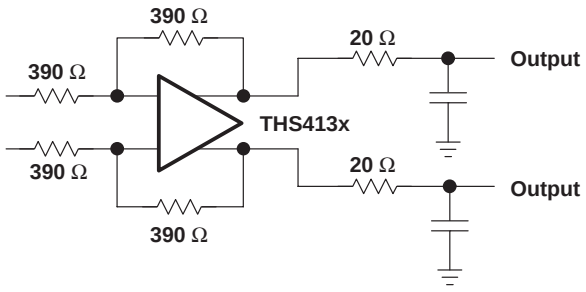


Figure 32. Driving a Capacitive Load

circuit layout considerations

To achieve the levels of high frequency performance of the THS413x, follow proper printed-circuit board high frequency design techniques. A general set of guidelines is given below. In addition, a THS413x evaluation board is available to use as a guide for layout or for evaluating the device performance.

- Ground planes – It is highly recommended that a ground plane be used on the board to provide all components with a low inductive ground connection. However, in the areas of the amplifier inputs and output, the ground plane can be removed to minimize the stray capacitance.
- Proper power supply decoupling – Use a 6.8-μF tantalum capacitor in parallel with a 0.1-μF ceramic capacitor on each supply terminal. It may be possible to share the tantalum among several amplifiers depending on the application, but a 0.1-μF ceramic capacitor should always be used on the supply terminal of every amplifier. In addition, the 0.1-μF capacitor should be placed as close as possible to the supply terminal. As this distance increases, the inductance in the connecting trace makes the capacitor less effective. The designer should strive for distances of less than 0.1 inches between the device power terminals and the ceramic capacitors.
- Sockets – Sockets are not recommended for high-speed operational amplifiers. The additional lead inductance in the socket pins will often lead to stability problems. Surface-mount packages soldered directly to the printed-circuit board is the best implementation.
- Short trace runs/compact part placements – Optimum high frequency performance is achieved when stray series inductance has been minimized. To realize this, the circuit layout should be made as compact as possible, thereby minimizing the length of all trace runs. Particular attention should be paid to the inverting input of the amplifier. Its length should be kept as short as possible. This will help to minimize stray capacitance at the input of the amplifier.

APPLICATION INFORMATION

circuit layout considerations (continued)

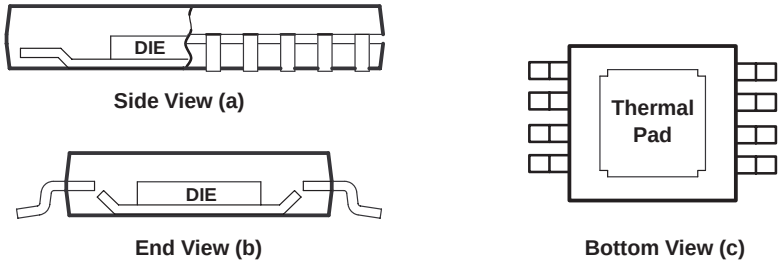
- Surface-mount passive components – Using surface-mount passive components is recommended for high frequency amplifier circuits for several reasons. First, because of the extremely low lead inductance of surface-mount components, the problem with stray series inductance is greatly reduced. Second, the small size of surface-mount components naturally leads to a more compact layout thereby minimizing both stray inductance and capacitance. If leaded components are used, it is recommended that the lead lengths be kept as short as possible.

general PowerPAD™ design considerations

The THS413x is available packaged in a thermally-enhanced DGN package, which is a member of the PowerPAD™ family of packages. This package is constructed using a downset leadframe upon which the die is mounted [see Figure 33(a) and Figure 33(b)]. This arrangement results in the lead frame being exposed as a thermal pad on the underside of the package [see Figure 33(c)]. Because this thermal pad has direct thermal contact with the die, excellent thermal performance can be achieved by providing a good thermal path away from the thermal pad.

The PowerPAD™ package allows for both assembly and thermal management in one manufacturing operation. During the surface-mount solder operation (when the leads are being soldered), the thermal pad can also be soldered to a copper area underneath the package. Through the use of thermal paths within this copper area, heat can be conducted away from the package into either a ground plane or other heat dissipating device.

The PowerPAD™ package represents a breakthrough in combining the small area and ease of assembly of the surface mount with the, heretofore, awkward mechanical methods of heatsinking.



NOTE A: The thermal pad is electrically isolated from all terminals in the package.

Figure 33. Views of Thermally Enhanced DGN Package

APPLICATION INFORMATION

general PowerPAD™ design considerations (continued)

Although there are many ways to properly heatsink this device, the following steps illustrate the recommended approach.

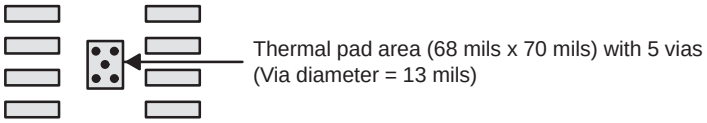


Figure 34. PowerPAD™ PCB Etch and Via Pattern

1. Prepare the PCB with a top side etch pattern as shown in Figure 34. There should be etch for the leads as well as etch for the thermal pad.
2. Place five holes in the area of the thermal pad. These holes should be 13 mils in diameter. Keep them small so that solder wicking through the holes is not a problem during reflow.
3. Additional vias may be placed anywhere along the thermal plane outside of the thermal pad area. This helps dissipate the heat generated by the THS413xDGN IC. These additional vias may be larger than the 13-mil diameter vias directly under the thermal pad. They can be larger because they are not in the thermal pad area to be soldered so that wicking is not a problem.
4. Connect all holes to the internal ground plane.
5. When connecting these holes to the ground plane, *do not* use the typical web or spoke via connection methodology. Web connections have a high thermal resistance connection that is useful for slowing the heat transfer during soldering operations. This makes the soldering of vias that have plane connections easier. In this application, however, low thermal resistance is desired for the most efficient heat transfer. Therefore, the holes under the THS413xDGN package should make their connection to the internal ground plane with a complete connection around the entire circumference of the plated-through hole.
6. The top-side solder mask should leave the terminals of the package and the thermal pad area with its five holes exposed. The bottom-side solder mask should cover the five holes of the thermal pad area. This prevents solder from being pulled away from the thermal pad area during the reflow process.
7. Apply solder paste to the exposed thermal pad area and all of the IC terminals.
8. With these preparatory steps in place, the THS413xDGN IC is simply placed in position and run through the solder reflow operation as any standard surface-mount component. This results in a part that is properly installed.

APPLICATION INFORMATION

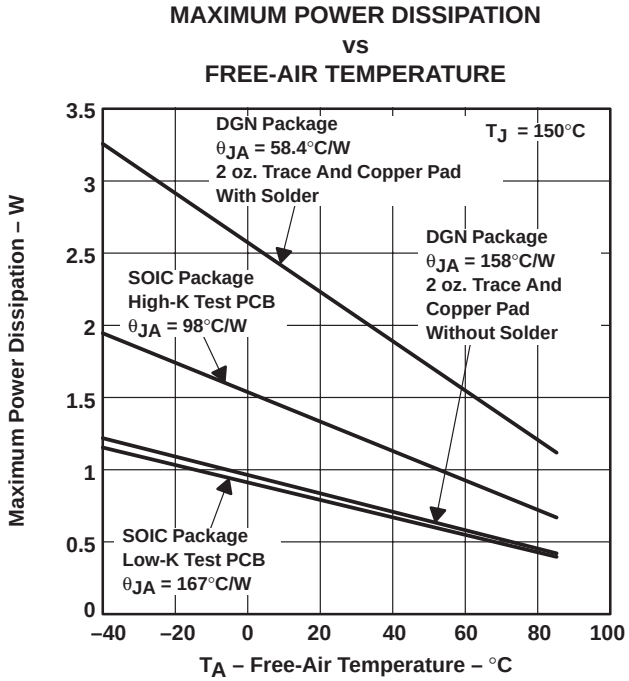
general PowerPAD™ design considerations (continued)

The actual thermal performance achieved with the THS413xDGN in its PowerPAD™ package depends on the application. In the example above, if the size of the internal ground plane is approximately 3 inches × 3 inches, then the expected thermal coefficient, θ_{JA}, is about 58.4°C/W. For comparison, the non-PowerPAD™ version of the THS413x IC (SOIC) is shown. For a given θ_{JA}, the maximum power dissipation is shown in Figure 35 and is calculated by the following formula:

$$P_D = \left(\frac{T_{MAX} - T_A}{\theta_{JA}} \right)$$

Where:

P_D = Maximum power dissipation of THS413x IC (watts)
T_{MAX} = Absolute maximum junction temperature (150°C)
T_A = Free-ambient air temperature (°C)
$\theta_{JA} = \theta_{JC} + \theta_{CA}$
θ_{JC} = Thermal coefficient from junction to case (°C/W)
θ_{CA} = Thermal coefficient from case to ambient air (°C/W)



NOTE A: Results are with no air flow and PCB size = 3"× 3"

Figure 35. Maximum Power Dissipation vs Free-Air Temperature

More complete details of the PowerPAD™ installation process and thermal management techniques can be found in the Texas Instruments Technical Brief, *PowerPAD™ Thermally Enhanced Package.* This document can be found at the TI web site (www.ti.com) by searching on the key word PowerPAD™. The document can also be ordered through your local TI sales office. Refer to literature number SLMA002 when ordering.

APPLICATION INFORMATION

general PowerPAD™ design considerations (continued)

The next consideration is the package constraints. The two sources of heat within an amplifier are quiescent power and output power. The designer should never forget about the quiescent heat generated within the device, especially devices with multiple amplifiers or output stages. Because these devices have linear output stages (Class A-B), most of the heat dissipation is at low output voltages with high output currents. Figure 36 to Figure 37 show this effect, along with the quiescent heat, with an ambient air temperature of 50°C. Obviously, as the ambient temperature increases, the limit lines shown will drop accordingly. The area under each respective limit line is considered the safe operating area. Any condition above this line will exceed the amplifier's limits and failure may result. When using V_{CC} = ±5 V, there is generally not a heat problem, even with SOIC packages. But, when using V_{CC} = ±15 V, the SOIC package is severely limited in the amount of heat it can dissipate. The other key factor when looking at these graphs is how the devices are mounted on the PCB. The PowerPAD™ devices are extremely useful for heat dissipation. But, the device should always be soldered to a copper plane to fully utilize the heat dissipation properties of the PowerPAD™. The SOIC package, on the other hand, is highly dependent on how it is mounted on the PCB. As more trace and copper area is placed around the device, θ_{JA} decreases and the heat dissipation capability increases. The currents and voltages shown in these graphs are for the total package. The sum of the RMS output currents and voltages should be used to choose the proper package. The graphs shown assume that both of the amplifier's outputs are symmetrical.

MAXIMUM RMS OUTPUT CURRENT vs RMS OUTPUT VOLTAGE DUE TO THERMAL LIMITS

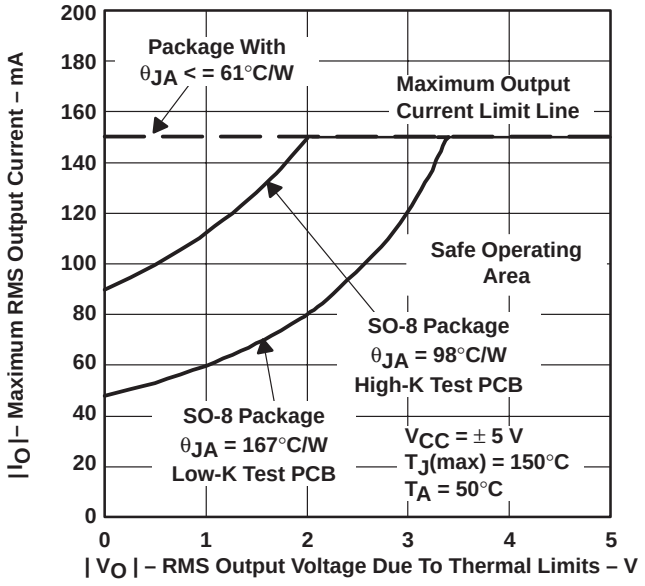


Figure 36

MAXIMUM RMS OUTPUT CURRENT vs RMS OUTPUT VOLTAGE DUE TO THERMAL LIMITS

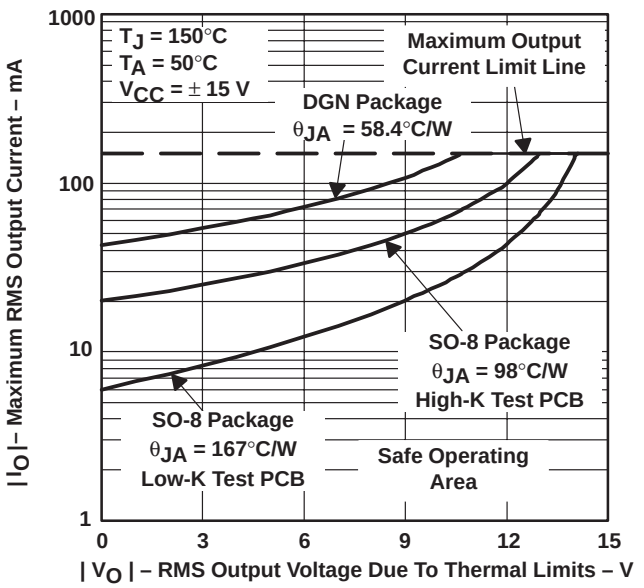


Figure 37

APPLICATION INFORMATION

Active antialias filtering

For signal conditioning in ADC applications, it is important to limit the input frequency to the ADC. Low-pass filters can prevent the aliasing of the high frequency noise with the frequency of operation. The following figure presents a method by which the noise may be filtered in the THS413x.

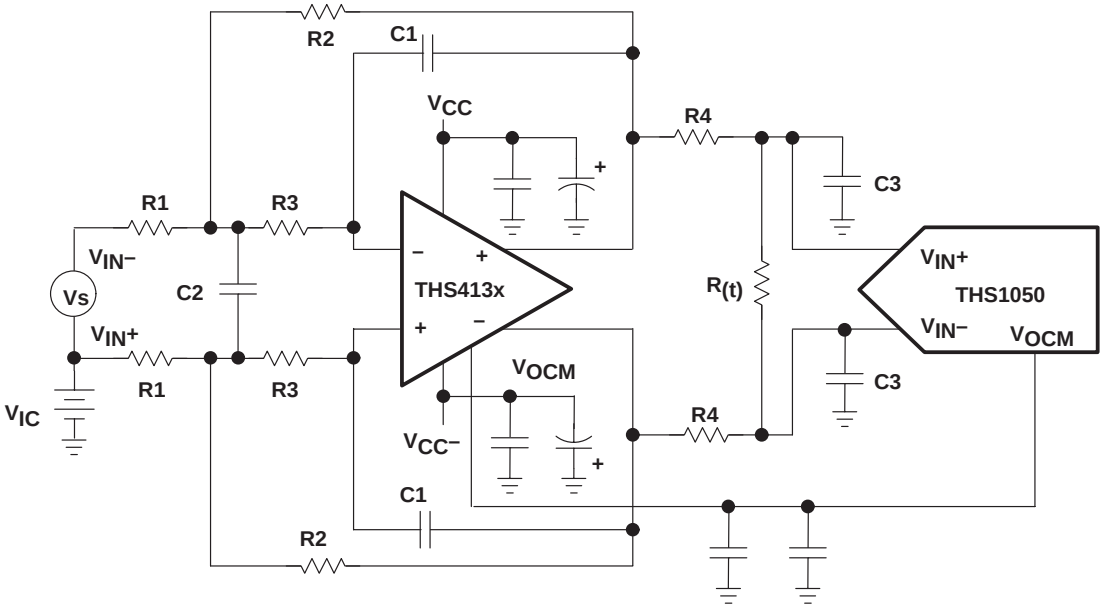


Figure 38. Antialias Filtering

PRINCIPLES OF OPERATION

theory of operation

The THS413x is a fully differential amplifier. Differential amplifiers are typically *differential in/single out*, whereas fully differential amplifiers are *differential in/differential out*.

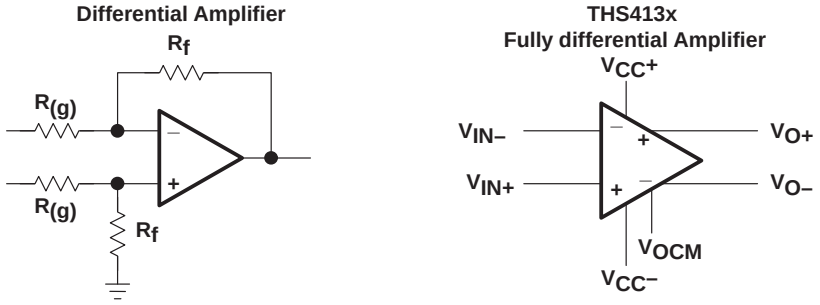


Figure 39. Differential Amplifier Versus a Fully Differential Amplifier

To understand the THS413x fully differential amplifiers, the definition for the pinouts of the amplifier are provided.

Input voltage definition $V_{ID} = (V_I+) - (V_I-)$ $V_{IC} = \frac{(V_I+) - (V_I-)}{2}$

Output voltage definition $V_{OD} = (V_O+) - (V_O-)$ $V_{OC} = \frac{(V_O+) - (V_O-)}{2}$

Transfer function $V_{OD} = V_{ID} \times A_{(f)}$

Output common mode voltage $V_{OC} = V_{OCM}$

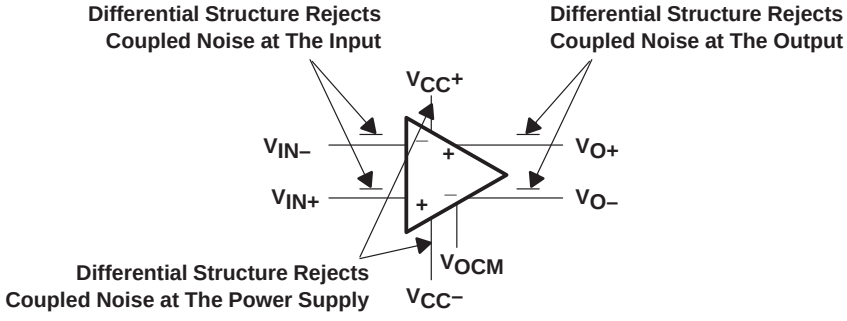


Figure 40. Definition of the Fully Differential Amplifier

PRINCIPLES OF OPERATION

The following schematics depict the differences between the operation of the THS413x, fully differential amplifier, in two different modes. Fully differential amplifiers can work with differential input or can be implemented as single in/differential out.

Note: For proper operation, maintain symmetry by setting
$R_f1 = R_f2 = R_f$ and $R_{(g)}1 = R_{(g)}2 = R_{(g)}$
$\Rightarrow A = R_f/R_{(g)}$

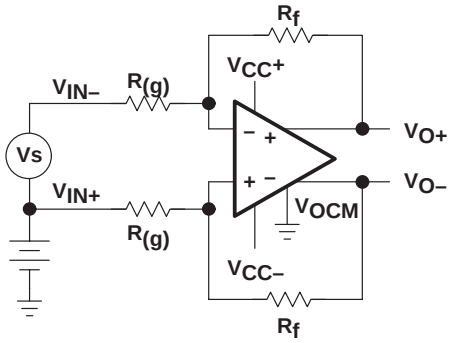


Figure 41. Amplifying Differential Signals

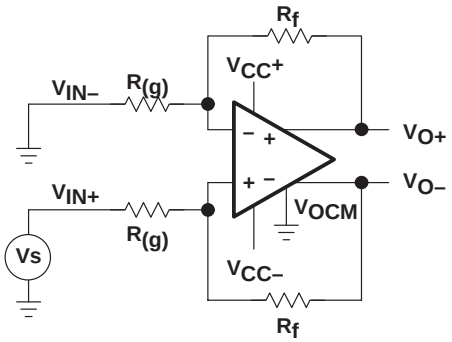


Figure 42. Single In With Differential Out

If each output is measured independently, each output is one-half of the input signal when gain is 1. The following equations express the transfer function for each output:

$$V_O = \frac{1}{2} V_I$$

The second output is equal and opposite in sign:

$$V_O = -\frac{1}{2} V_I$$

Fully differential amplifiers may be viewed as two inverting amplifiers. In this case, the equation of an inverting amplifier holds true for gain calculations. One advantage of fully differential amplifiers is that they offer twice as much dynamic range compared to single-ended amplifiers. For example, a 1-V_{PP} ADC can only support an input signal of 1 V_{PP}. If the output of the amplifier is 2 V_{PP}, then it will not be practical to feed a 2-V_{PP} signal into the targeted ADC. Using a fully differential amplifier enables the user to break down the output into two 1-V_{PP} signals with opposite signs and feed them into the differential input nodes of the ADC. In practice, the designer has been able to feed a 2-V peak-to-peak signal into a 1-V differential ADC with the help of a fully differential amplifier. The final result indicates twice as much dynamic range. Figure 43 illustrates the increase in dynamic range. The gain factor should be considered in this scenario. The THS413x fully differential amplifier offers an improved CMRR and PSRR due to its symmetrical input and output. Furthermore, second harmonic distortion is improved. Second harmonics tend to cancel because of the symmetrical output.

PRINCIPLES OF OPERATION

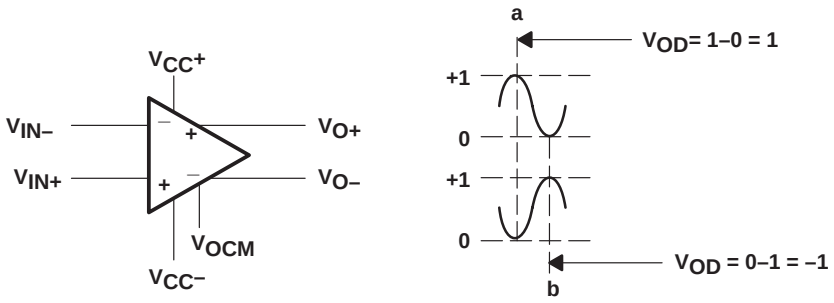


Figure 43. Fully Differential Amplifier With Two 1-V_{PP} Signals

Similar to the standard inverting amplifier configuration, input impedance of a fully differential amplifier is selected by the input resistor, $R_{(g)}$. If input impedance is a constraint in design, the designer may choose to implement the differential amplifier as an instrumentation amplifier. This configuration improves the input impedance of the fully differential amplifier. The following schematic depicts the general format of instrumentation amplifiers.

The general transfer function for this circuit is:

$$\frac{V_{OD}}{V_{IN1} - V_{IN2}} = \frac{R_f}{R_{(g)}} \left(1 + \frac{2R2}{R1}\right)$$

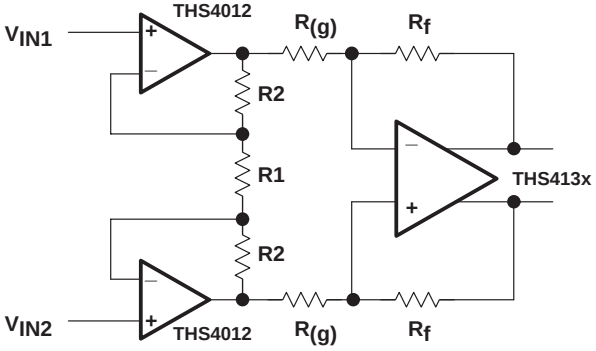


Figure 44. Instrumentation Amplifier

PRINCIPLES OF OPERATION

power-down mode

The power-down mode is used when power saving is required. The power-down terminal ($\overline{PD}$) found on the THS413x is an active low terminal. If it is left as a no-connect terminal, the device will always stay on due to an internal 50 kΩ resistor to V_{CC}. The threshold voltage for this terminal is approximately 1.4 V above V_{CC}–. This means that if the $\overline{PD}$ terminal is 1.4 V above V_{CC}–, the device is active. If the $\overline{PD}$ terminal is less than 1.4 V above V_{CC}–, the device is off. For example, if V_{CC}– = –5 V, then the device is on when PD reaches -3.6 V, (-5 V + 1.4 V = –3.6 V). By the same calculation, the device is off below –3.6 V. It is recommended to pull the terminal to V_{CC}– in order to turn the device off. The following graph shows the simplified version of the power-down circuit. While in the power-down state, the amplifier goes into a high impedance state. The amplifier output impedance is typically greater than 1 MΩ in the power-down state.

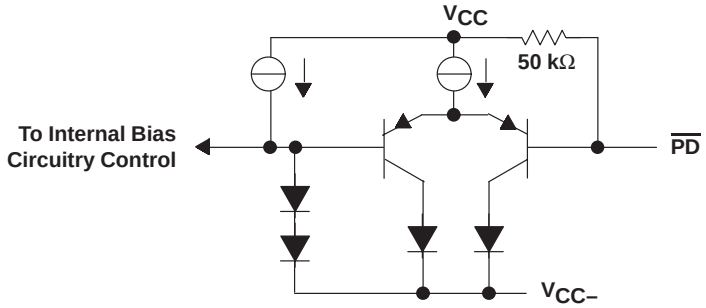


Figure 45. Simplified Power-Down Circuit

PRINCIPLES OF OPERATION

Due to the similarity of the standard inverting amplifier configuration, the output impedance appears to be very low while in the power-down state. This is because the feedback resistor (R_f) and the gain resistor ($R_{(g)}$) are still connected to the circuit. Therefore, a current path is allowed between the input of the amplifier and the output of the amplifier. An example of the closed loop output impedance is shown in Figure 46.

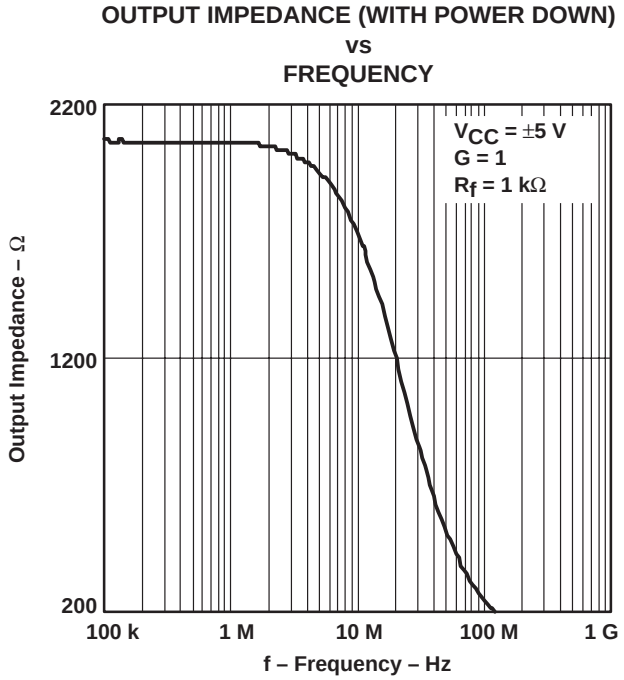


Figure 46

resistor values

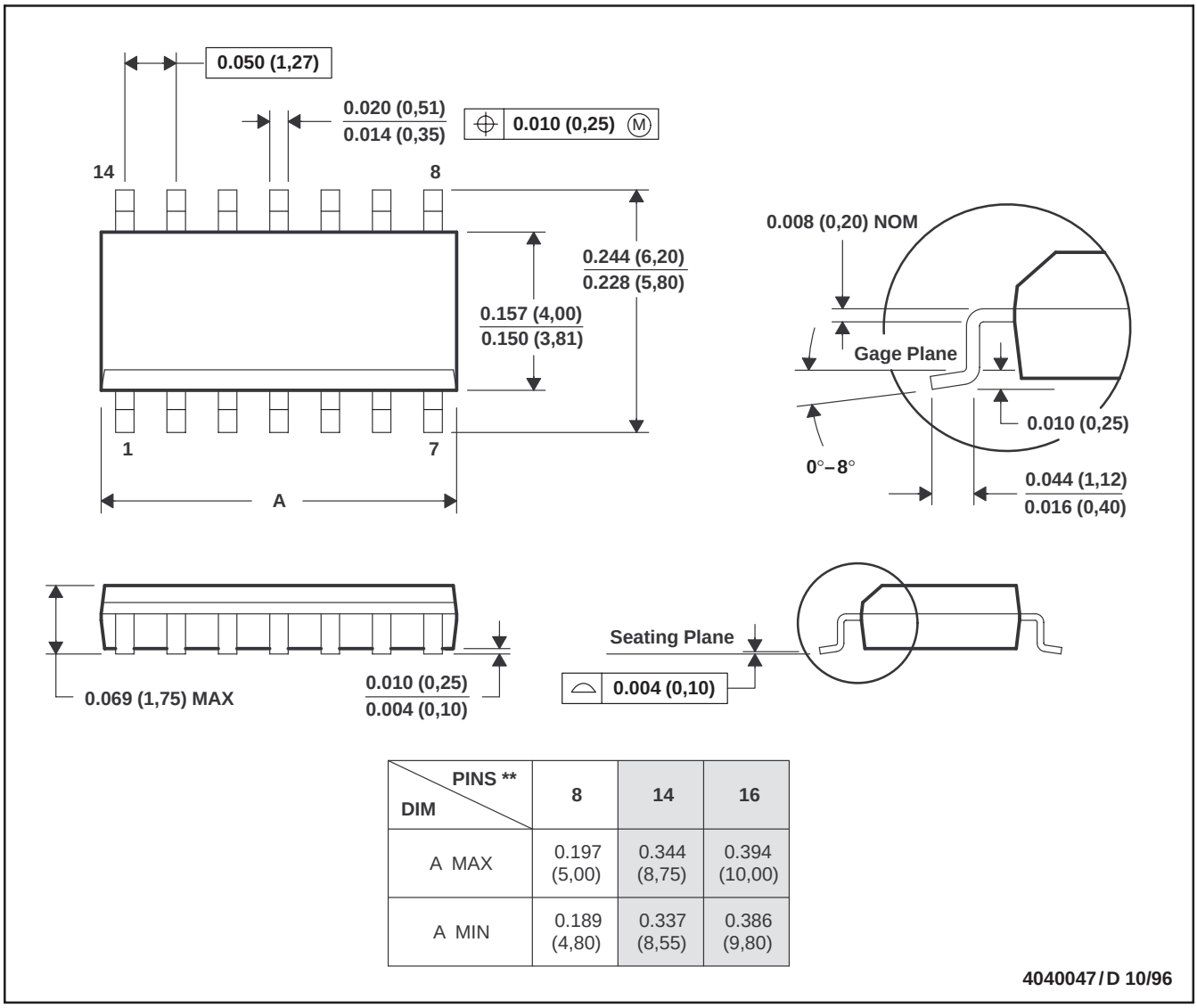
Suggested resistor values for various gains.

GAIN	$R_{(g)}$ Ω	R_f Ω
1	390	390
2	374	750
5	402	2010
10	402	4020

MECHANICAL DATA

D (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



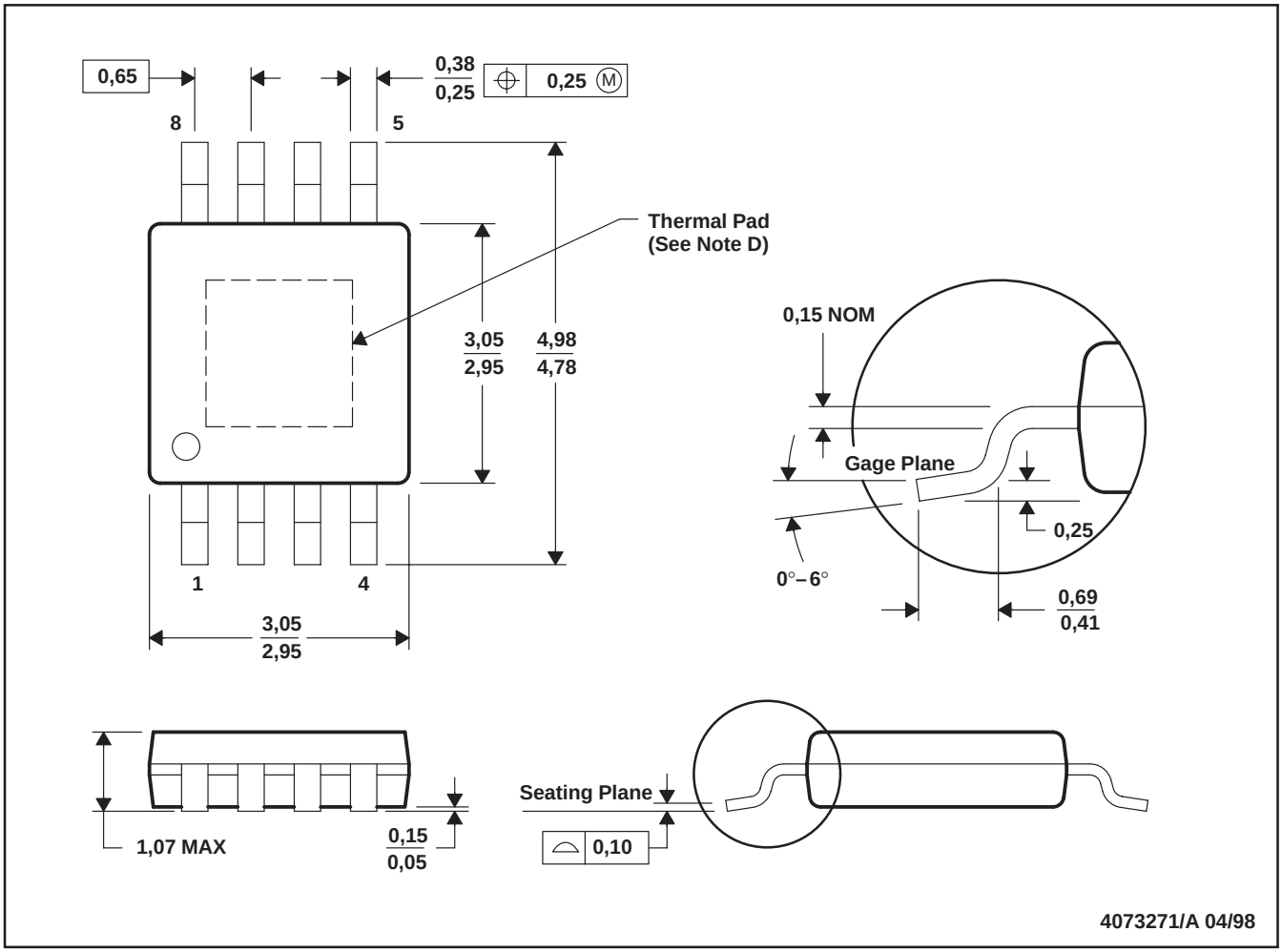
DIM \ PINS **	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

4040047/D 10/96

NOTES: B. All linear dimensions are in inches (millimeters).
C. This drawing is subject to change without notice.
D. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
E. Falls within JEDEC MS-012

MECHANICAL DATA

DGN (S-PDSO-G8) **PowerPAD™ PLASTIC SMALL-OUTLINE PACKAGE**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions include mold flash or protrusions.
D. The package thermal performance may be enhanced by attaching an external heat sink to the thermal pad. This pad is electrically and thermally connected to the backside of the die and possibly selected leads.
E. Falls within JEDEC MO-187

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