

# MOS FIELD EFFECT TRANSISTOR

2SK2512

## SWITCHING N-CHANNEL POWER MOS FET INDUSTRIAL USE

#### **DESCRIPTION**

The 2SK2512 is N-Channel MOS Field Effect Transistor designed for high current switching applications.

#### **FEATURES**

· Low On-Resistance

RDS (on)1 = 15 m $\Omega$  (VGS = 10 V, ID = 23 A) RDS (on)2 = 23 m $\Omega$  (VGS = 4 V, ID = 23 A)

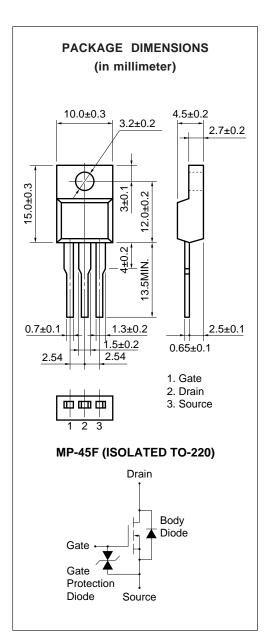
- Low Ciss Ciss = 2 100 pF TYP.
- Built-in G-S Protection Diode

#### ABSOLUTE MAXIMUM RATINGS $(T_A = 25 \degree C)$

Drain to Source Voltage	Voss	60	V
Gate to Source Voltage	Vgss	±20	V
Drain Current (DC)	$I_{D(DC)}$	±45	Α
Drain Current (pulse)*	ID(pulse	e) ±180	Α
Total Power Dissipation (Tc = 25 °C)	P <sub>T1</sub>	35	W
Total Power Dissipation (T <sub>A</sub> = 25 °C)	$P_{T2}$	2.0	W
Channel Temperature	$T_ch$	150	°C
Storage Temperature	$T_{stg}$	-55 to +150	°C

\* PW  $\leq$  10  $\mu$ s, Duty Cycle  $\leq$  1 %

The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device is actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

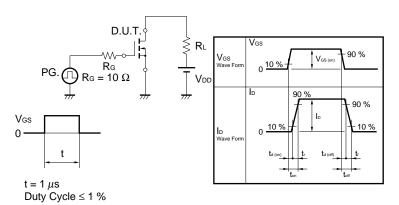




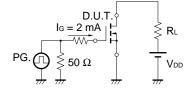
# ELECTRICAL CHARACTERISTICS (TA = 25 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Drain to Source On-Resistance	RDS (on)1		11	15	mΩ	Vgs = 10 V, ID = 23 A
Drain to Source On-Resistance	RDS (on)2		16	23	mΩ	Vgs = 4 V, Ip = 23 A
Gate to Source Cutoff Voltage	VGS (off)	1.0	1.5	2.0	V	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1 mA
Forward Transfer Admittance	yfs	15	20		S	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 23 A
Drain Leakage Current	IDSS			10	μΑ	V <sub>DS</sub> = V <sub>DSS</sub> , V <sub>GS</sub> = 0
Gate to Source Leakage Current	Igss			±10	μΑ	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0$
Input Capacitance	Ciss		2 100		pF	V <sub>DS</sub> = 10 V
Output Capacitance	Coss		1 100		pF	V <sub>G</sub> S = 0
Reverse Transfer Capacitance	Crss		500		pF	f = 1 MHz
Turn-On Delay Time	td (on)		45		ns	ID = 23 A
Rise Time	tr		380		ns	VGS (on) = 10 V
Turn-Off Delay Time	td (off)		320		ns	V <sub>DD</sub> = 30 V
Fall Time	<b>t</b> f		320		ns	R <sub>G</sub> = 10 Ω
Total Gate Charge	Q <sub>G</sub>		101		nC	ID = 45 A
Gate to Source Charge	Qgs		7		nC	V <sub>DD</sub> = 48 V
Gate to Drain Charge	Q <sub>GD</sub>		40		nC	V <sub>GS</sub> = 10 V
Body Diode Forward Voltage	V <sub>F</sub> (S-D)		1.0		V	IF = 45 A, VGS = 0
Reverse Recovery Time	trr		100		ns	IF = 45 A, VGS = 0
Reverse Recovery Charge	Qrr		180		nC	di/dt = 100 A/μs

### **Test Circuit 1 Switching Time**

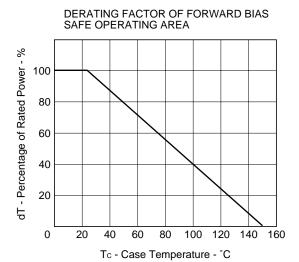


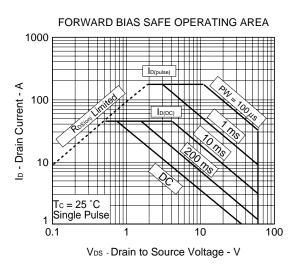
# Test Circuit 2 Gate Charge

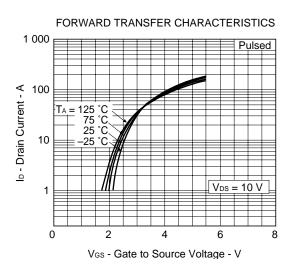


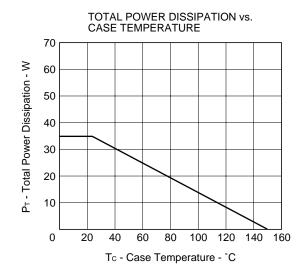
The application circuits and their parameters are for references only and are not intended for use in actual design-in's.

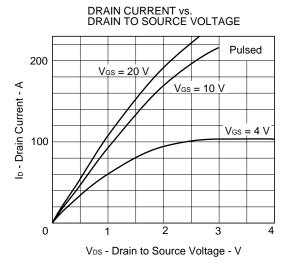
#### TYPICAL CHARACTERISTICS (TA = 25 °C)





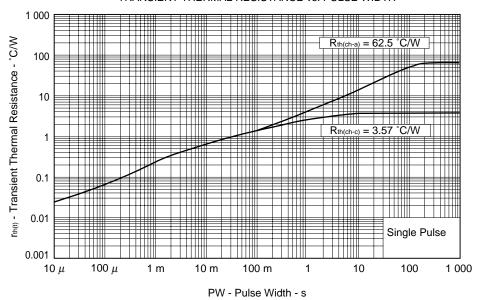




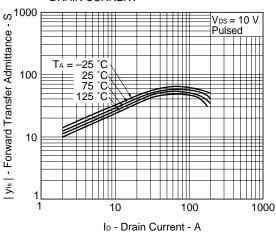


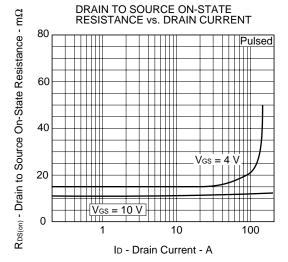
# **NEC**

#### TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH

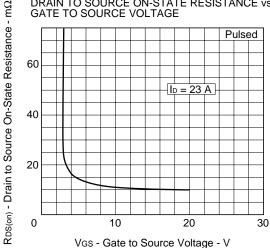




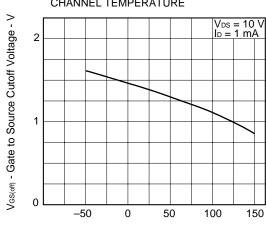




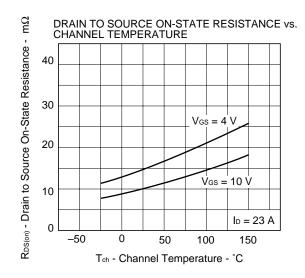
# DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

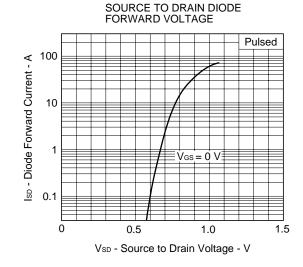


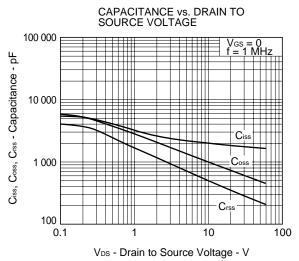
#### GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE

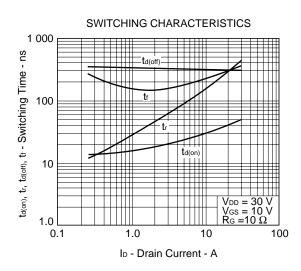


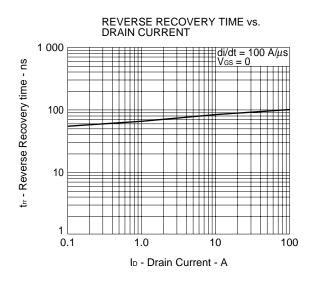
Tch - Channel Temperature - °C

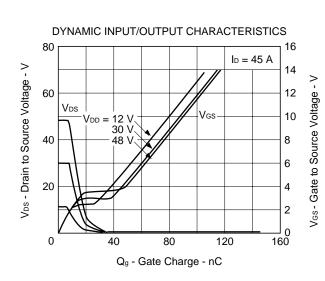














# REFERENCE

Document Name	Document No.
NEC semiconductor device reliability/quality control system.	TEI-1202
Quality grade on NEC semiconductor devices.	IEI-1209
Semiconductor device mounting technology manual.	IEI-1207
Semiconductor device package manual.	IEI-1213
Guide to quality assurance for semiconductor devices.	MEI-1202
Semiconductor selection guide.	MF-1134
Power MOS FET features and application switching power supply.	TEA-1034
Application circuits using Power MOS FET.	TEA-1035
Safe operating area of Power MOS FET.	TEA-1037

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Anti-radioactive design is not implemented in this product.

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