NEC

DATA SHEET

MOS FIELD EFFECT TRANSISTOR

# 2SK2513, 2SK2513-Z

## SWITCHING
## N-CHANNEL POWER MOS FET
## INDUSTRIAL USE

### DESCRIPTION

The 2SK2513, 2SK2513-Z is N-Channel MOS Field Effect Transistor designed for high current switching applications.

### FEATURES

- Low On-Resistance
  $R_{DS(on)1}$ = 15 mΩ ($V_{GS}$ = 10 V, $I_D$ = 23 A)
  $R_{DS(on)2}$ = 23 mΩ ($V_{GS}$ = 4 V, $I_D$ = 23 A)
- Low $C_{iss}$ $C_{iss}$ = 2 100 pF TYP.
- Built-in G-S Protection Diode

### ABSOLUTE MAXIMUM RATINGS ($T_A$ = 25 °C)

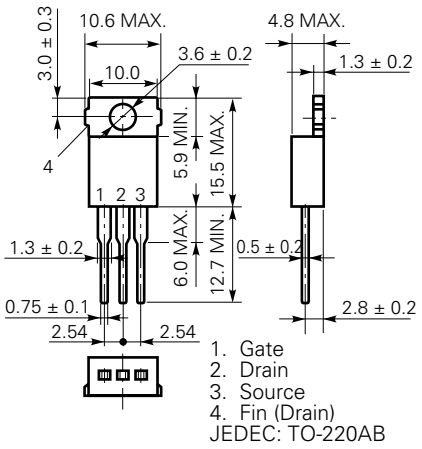
| | | | |
|---|---|---|---|
| Drain to Source Voltage | $V_{DSS}$ | 60 | V |
| Gate to Source Voltage | $V_{GSS}$ | ±20 | V |
| Drain Current (DC) | $I_{D(DC)}$ | ±45 | A |
| Drain Current (pulse)* | $I_{D(pulse)}$ | ±180 | A |
| Total Power Dissipation ($T_c$ = 25 °C) | $P_{T1}$ | 75 | W |
| Total Power Dissipation ($T_A$ = 25 °C) | $P_{T2}$ | 1.5 | W |
| Channel Temperature | $T_{ch}$ | 150 | °C |
| Storage Temperature | $T_{stg}$ | –55 to +150 | °C |

* PW ≤ 10 μs, Duty Cycle ≤ 1 %

The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device is actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

### PACKAGE DIMENSIONS

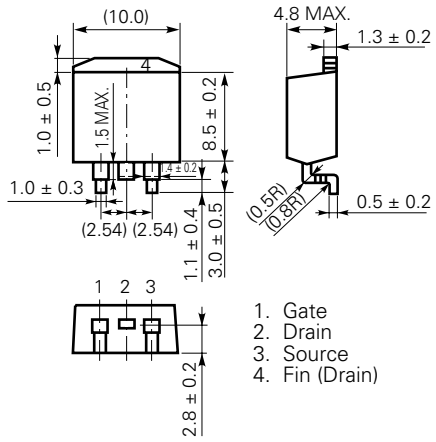
(in millimeters)




1. Gate
2. Drain
3. Source
4. Fin (Drain)

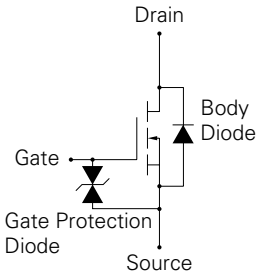
JEDEC: TO-220AB

**MP-25 (TO-220)**




1. Gate
2. Drain
3. Source
4. Fin (Drain)

**MP-25Z (SURFACE MOUNT TYPE)**

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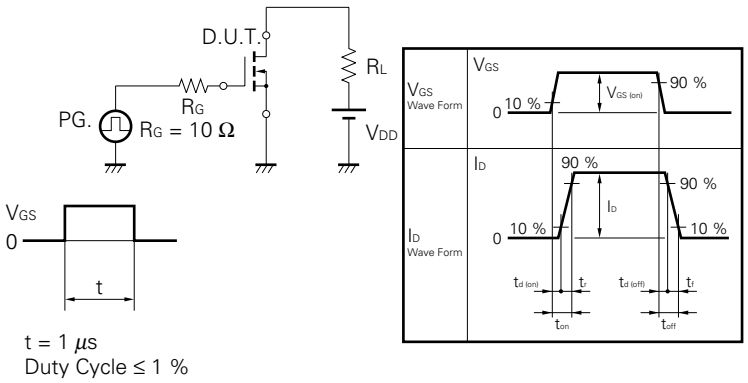
## ELECTRICAL CHARACTERISTICS ($T_A$ = 25 °C)

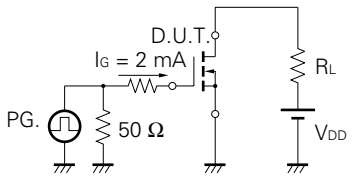
| CHARACTERISTIC | SYMBOL | MIN. | TYP. | MAX. | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|
| Drain to Source On-State Resistance | $R_{DS(on)1}$ | | 11 | 15 | mΩ | $V_{GS}$ = 10 V, $I_D$ = 23 A |
| Drain to Source On-State Resistance | $R_{DS(on)2}$ | | 16 | 23 | mΩ | $V_{GS}$ = 4 V, $I_D$ = 23 A |
| Gate to Source Cutoff Voltage | $V_{GS(off)}$ | 1.0 | 1.5 | 2.0 | V | $V_{DS}$ = 10 V, $I_D$ = 1 mA |
| Forward Transfer Admittance | $\|y_{fs}\|$ | 15 | 20 | | S | $V_{DS}$ = 10 V, $I_D$ = 23 A |
| Drain Leakage Current | $I_{DSS}$ | | | 10 | μA | $V_{DS}$ = $V_{DSS}$, $V_{GS}$ = 0 |
| Gate to Source Leakage Current | $I_{GSS}$ | | | ±10 | μA | $V_{GS}$ = ±20 V, $V_{DS}$ = 0 |
| Input Capacitance | $C_{iss}$ | | 2 100 | | pF | $V_{DS}$ = 10 V |
| Output Capacitance | $C_{oss}$ | | 1 100 | | pF | $V_{GS}$ = 0 |
| Reverse Transfer Capacitance | $C_{rss}$ | | 500 | | pF | f = 1 MHz |
| Turn-On Delay Time | $t_{d(on)}$ | | 45 | | ns | $I_D$ = 23 A |
| Rise Time | $t_r$ | | 380 | | ns | $V_{GS(on)}$ = 10 V |
| Turn-Off Delay Time | $t_{d(off)}$ | | 320 | | ns | $V_{DD}$ = 30 V |
| Fall Time | $t_f$ | | 320 | | ns | $R_G$ = 10 Ω |
| Total Gate Charge | $Q_G$ | | 100 | | nC | $I_D$ = 45 A |
| Gate to Source Charge | $Q_{GS}$ | | 7 | | nC | $V_{DD}$ = 48 V |
| Gate to Drain Charge | $Q_{GD}$ | | 40 | | nC | $V_{GS}$ = 10 V |
| Body Diode Forward Voltage | $V_{F(S-D)}$ | | 1.0 | | V | $I_F$ = 45 A, $V_{GS}$ = 0 |
| Reverse Recovery Time | $t_{rr}$ | | 100 | | ns | $I_F$ = 45 A, $V_{GS}$ = 0 |
| Reverse Recovery Charge | $Q_{rr}$ | | 180 | | nC | di/dt = 100 A/μs |

**Test Circuit 1 Switching Time**




t = 1 μs
Duty Cycle ≤ 1 %

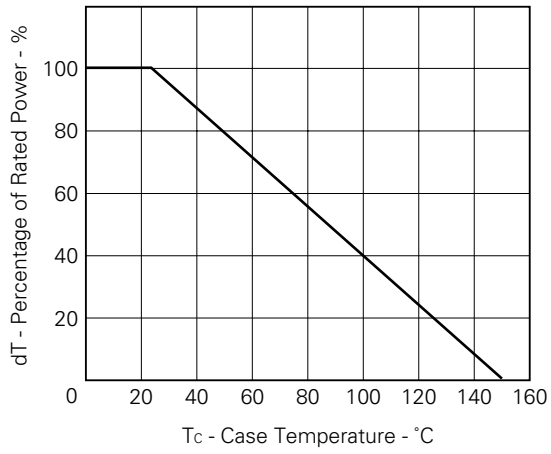
**Test Circuit 2 Gate Charge**



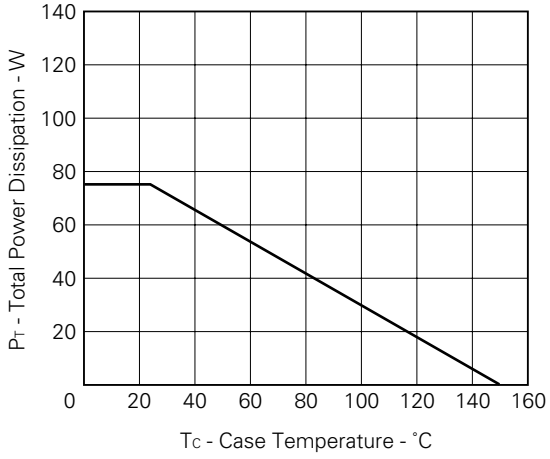

The application circuits and their parameters are for references only and are not intended for use in actual design-in's.

## TYPICAL CHARACTERISTICS ($T_A$ = 25 ˚C)

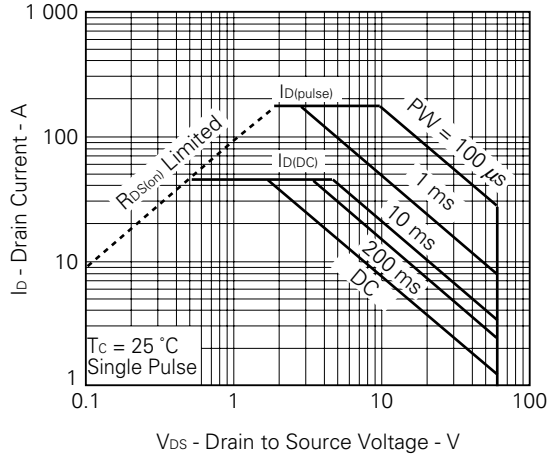
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



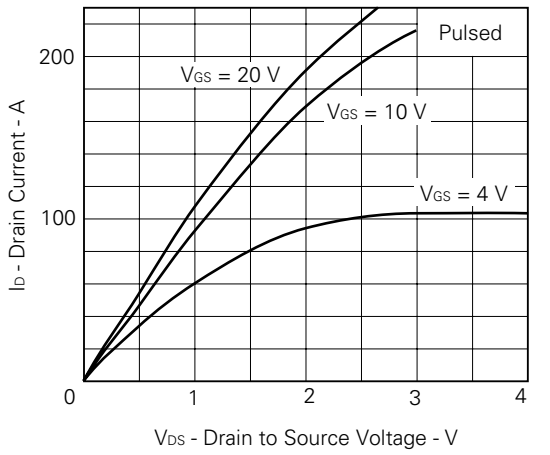

TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



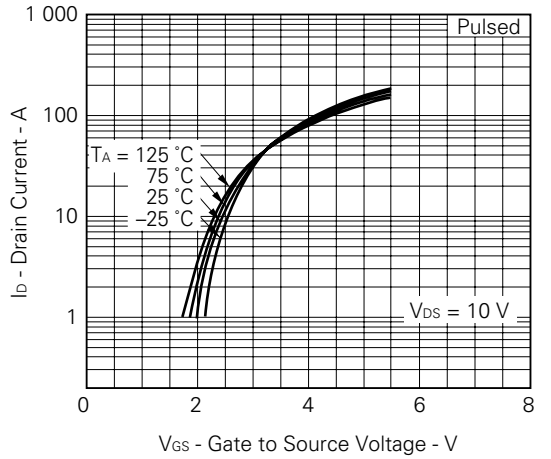

FORWARD BIAS SAFE OPERATING AREA



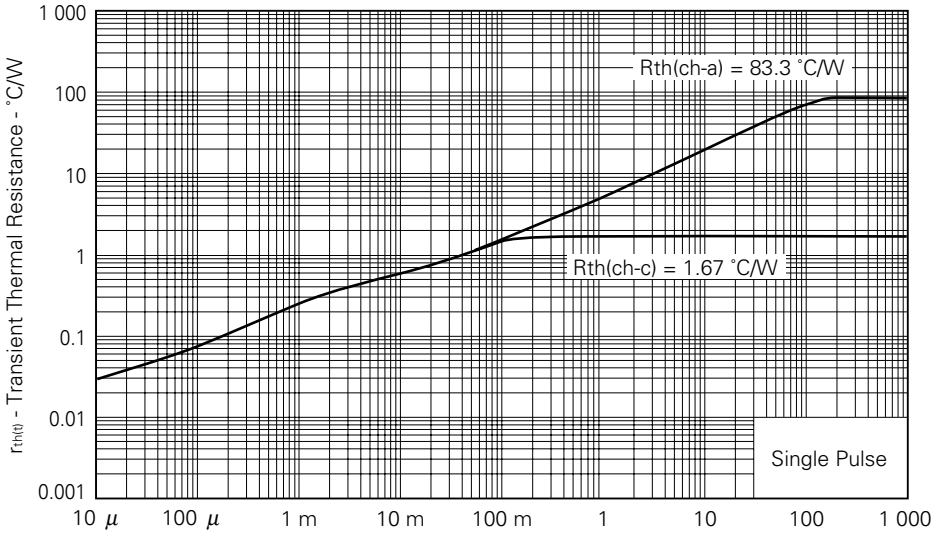

DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



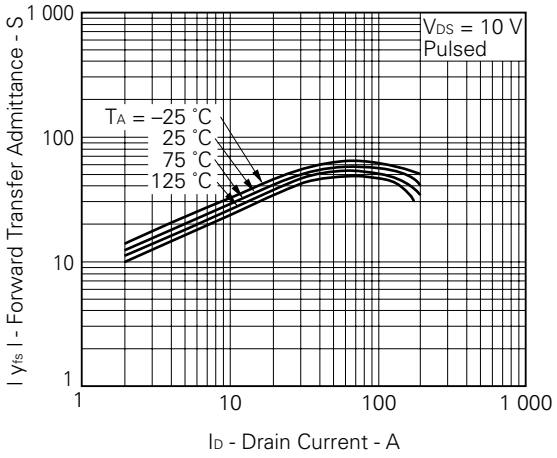

FORWARD TRANSFER CHARACTERISTICS



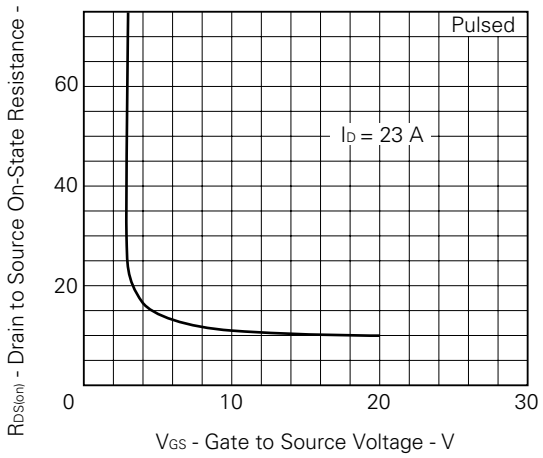
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



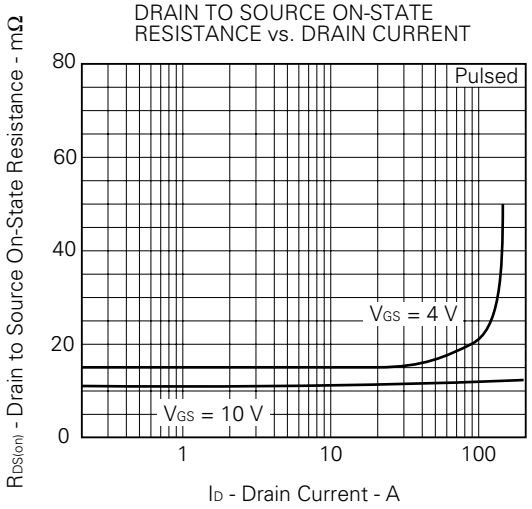

FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



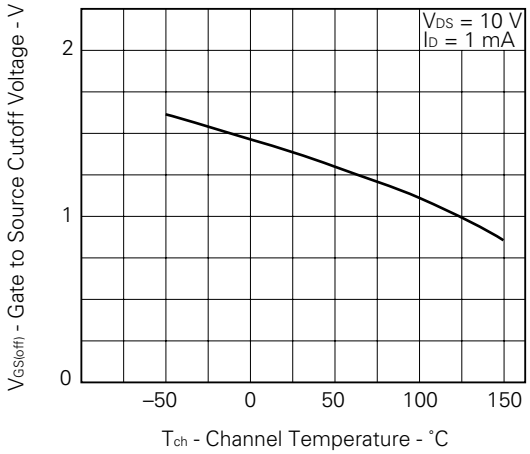

DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



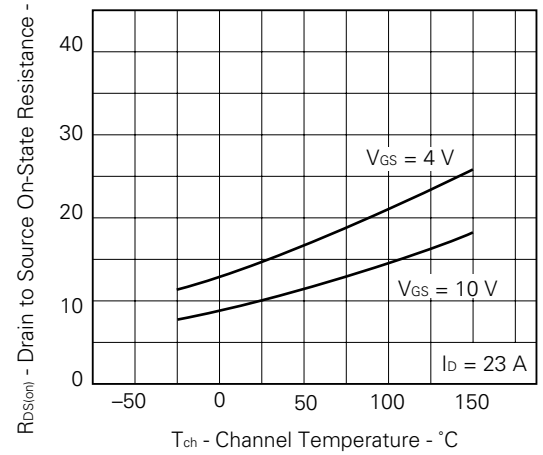

DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



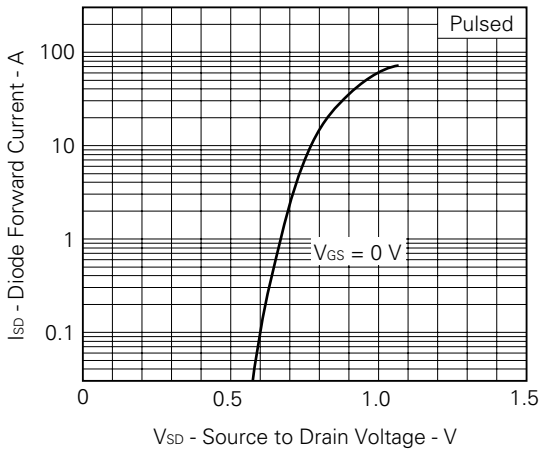

GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE



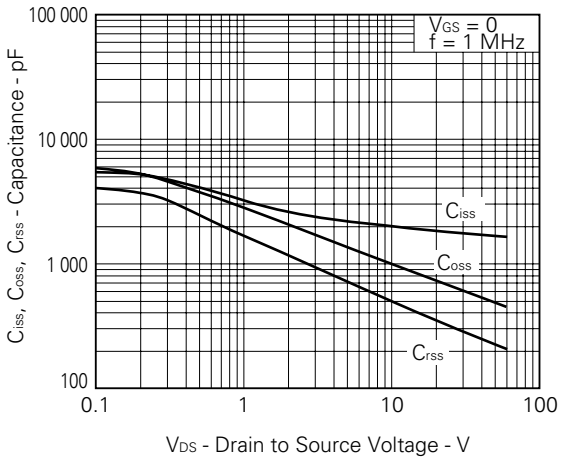
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



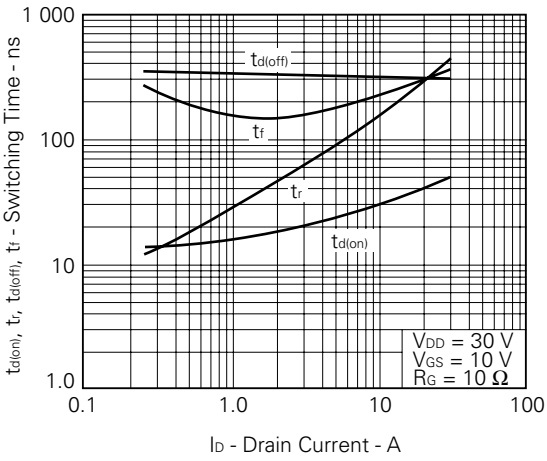

SOURCE TO DRAIN DIODE FORWARD VOLTAGE



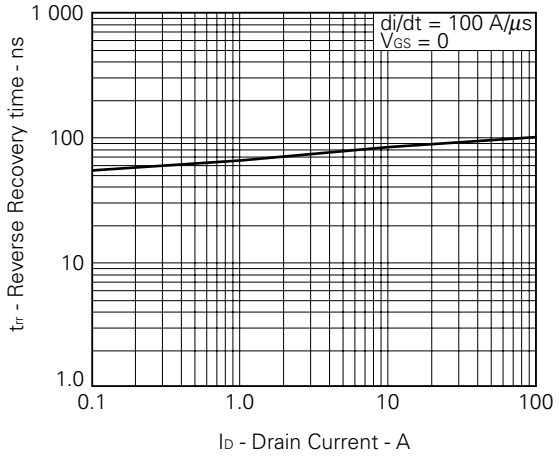

CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



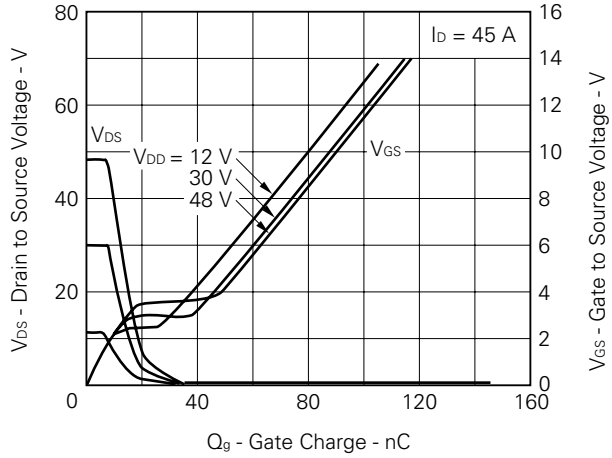

SWITCHING CHARACTERISTICS




REVERSE RECOVERY TIME vs. DRAIN CURRENT




DYNAMIC INPUT/OUTPUT CHARACTERISTICS



## REFERENCE

| Document Name | Document No. |
|---|---|
| NEC semiconductor device reliability/quality control system. | TEI-1202 |
| Quality grade on NEC semiconductor devices. | IEI-1209 |
| Semiconductor device mounting technology manual. | IEI-1207 |
| Semiconductor device package manual. | IEI-1213 |
| Guide to quality assurance for semiconductor devices. | MEI-1202 |
| Semiconductor selection guide. | MF-1134 |
| Power MOS FET features and application switching power supply. | TEA-1034 |
| Application circuits using Power MOS FET. | TEA-1035 |
| Safe operating area of Power MOS FET. | TEA-1037 |

[MEMO]